Silicon Integrated Nanophotonics: Road from Scientific Explorations to Practical Applications

Dr. Yurii A. Vlasov,
Manager, Silicon Integrated Nanophotonics

Si Photonics

1989

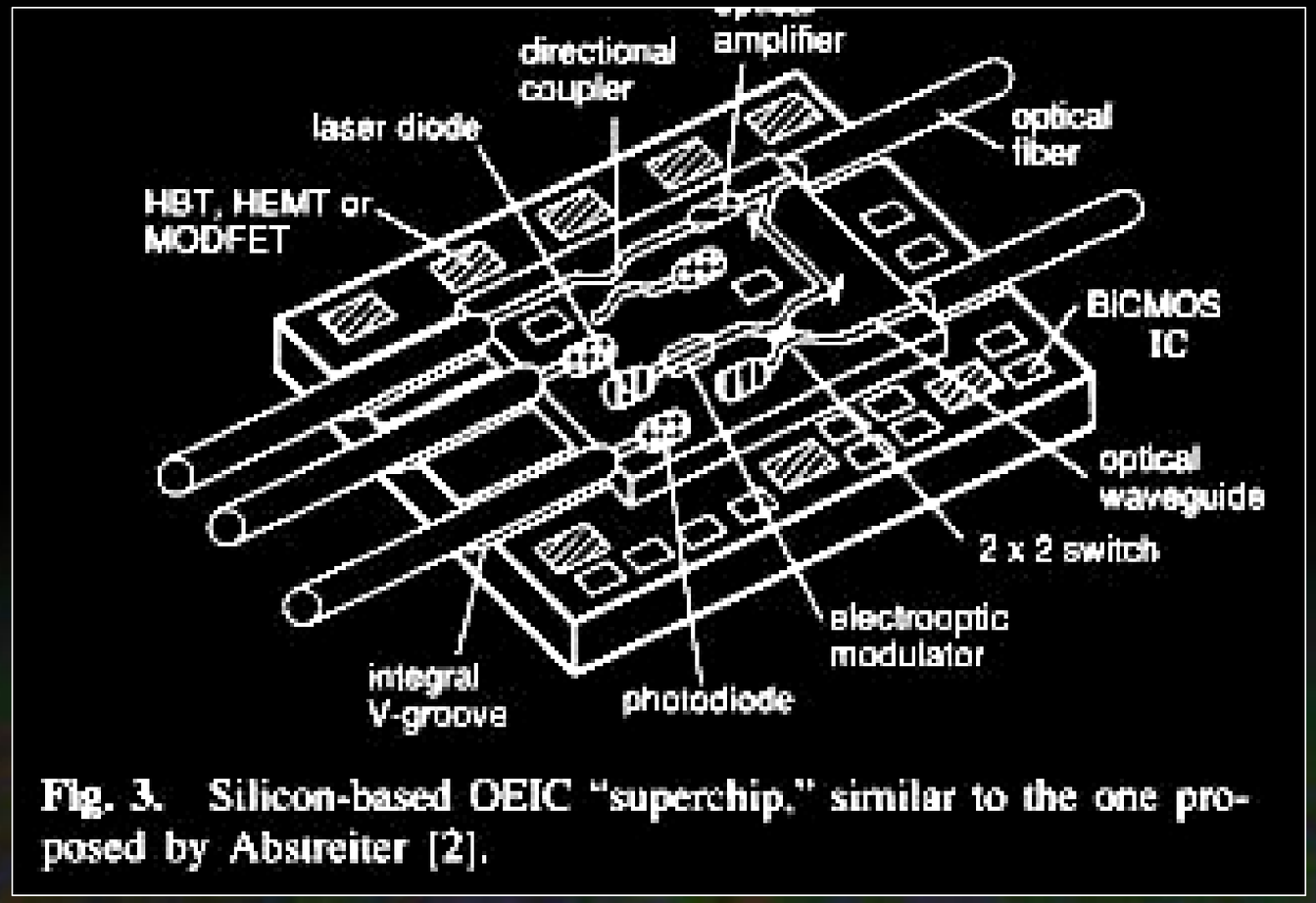


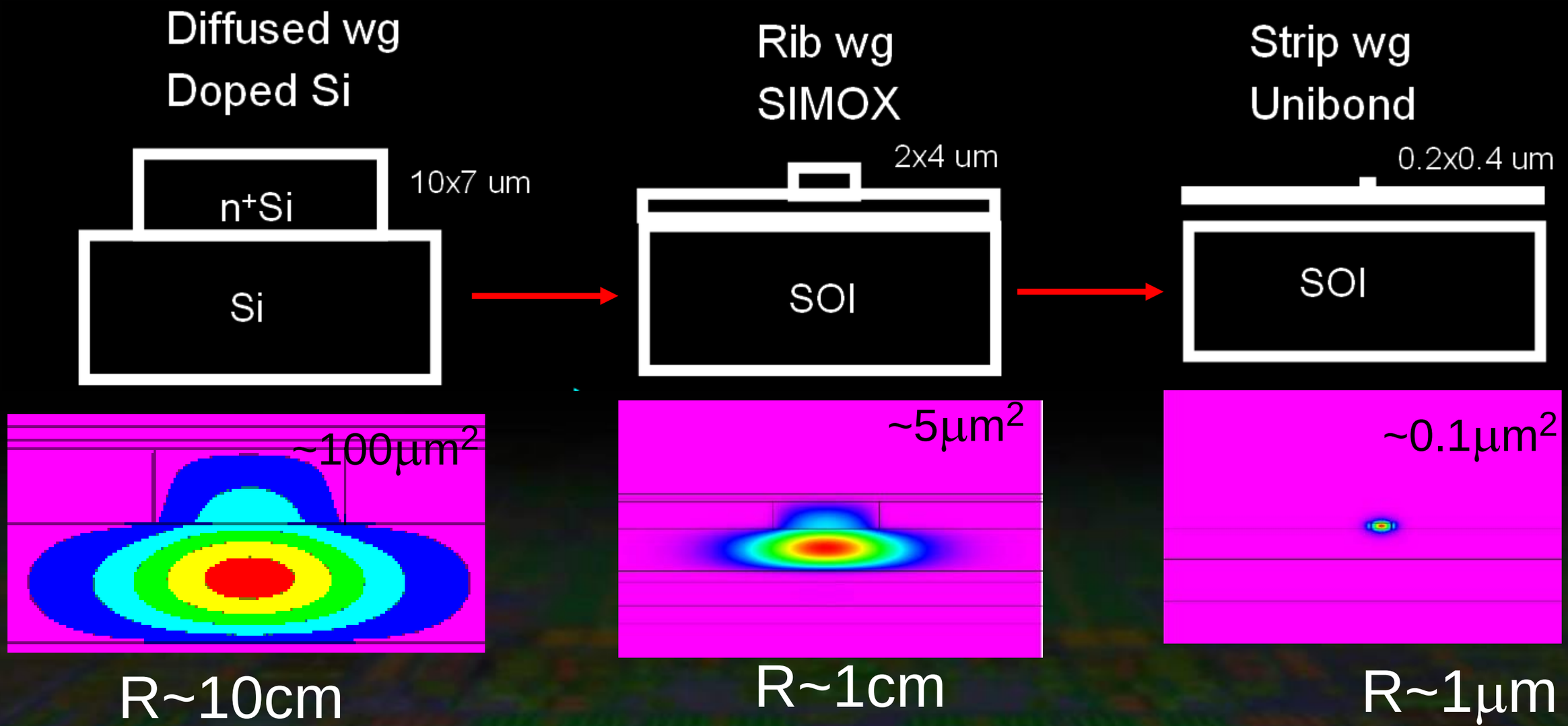
Fig. 3. Silicon-based OEIC "superchip," similar to the one proposed by Absreiter [2].

Concept:

1. Deep scaling of optics
2. CMOS compatible
   - Materials
   - Processing

R. Soref et al

Si Photonics scaling in 2 decades: 1985 - 2005

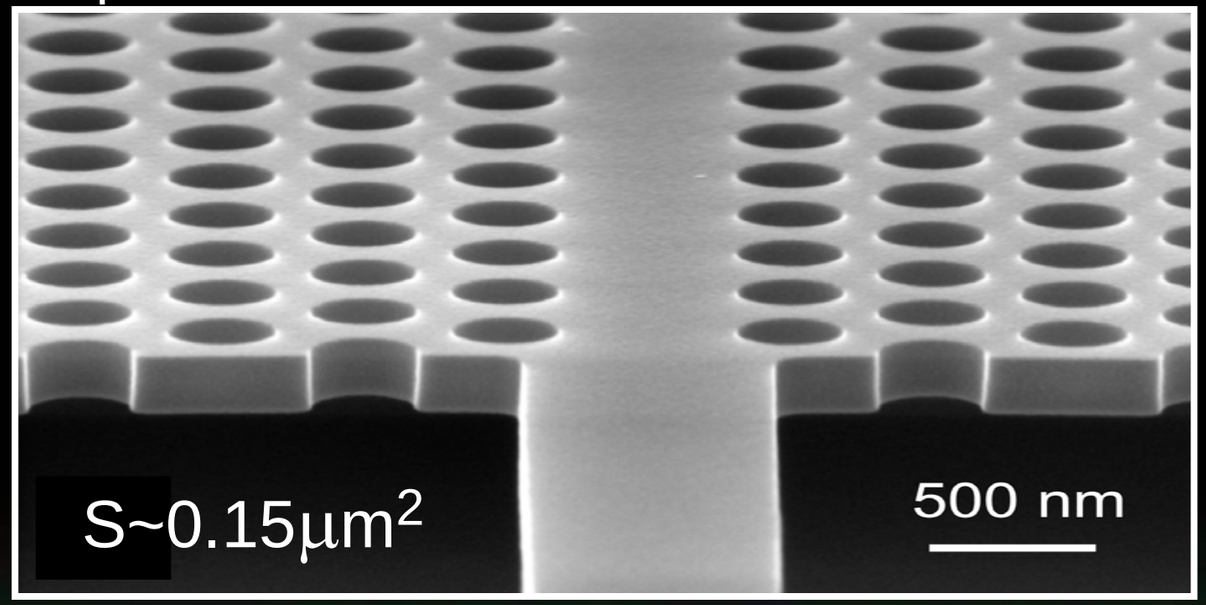


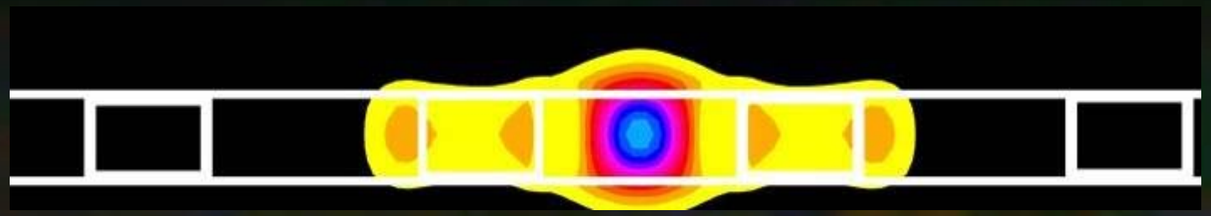
Higher refractive index contrast=smaller bending radius=higher integration density

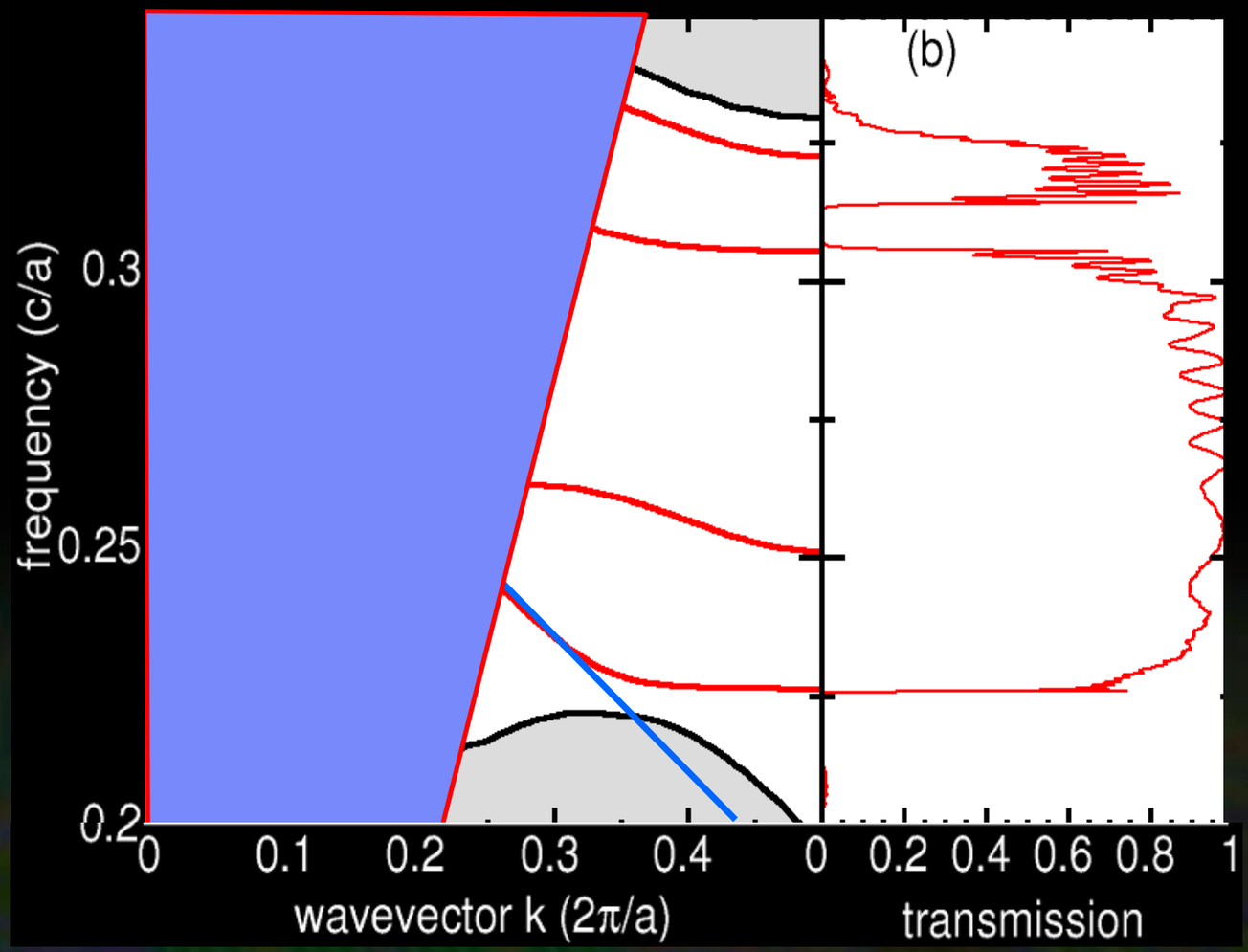
Planar SOI photonic crystals

holes 300nm

pitch 450nm





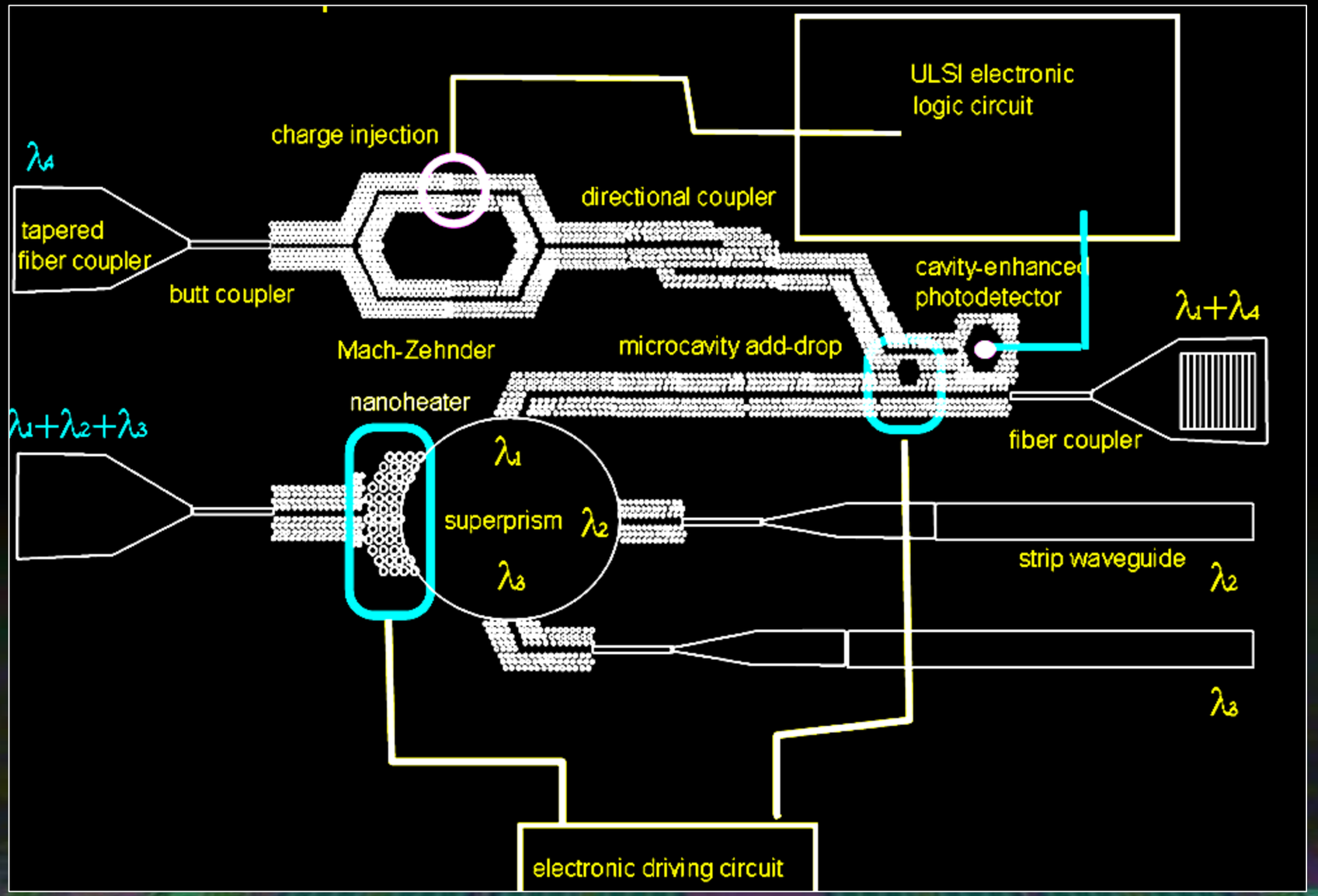


Very slow group velocities

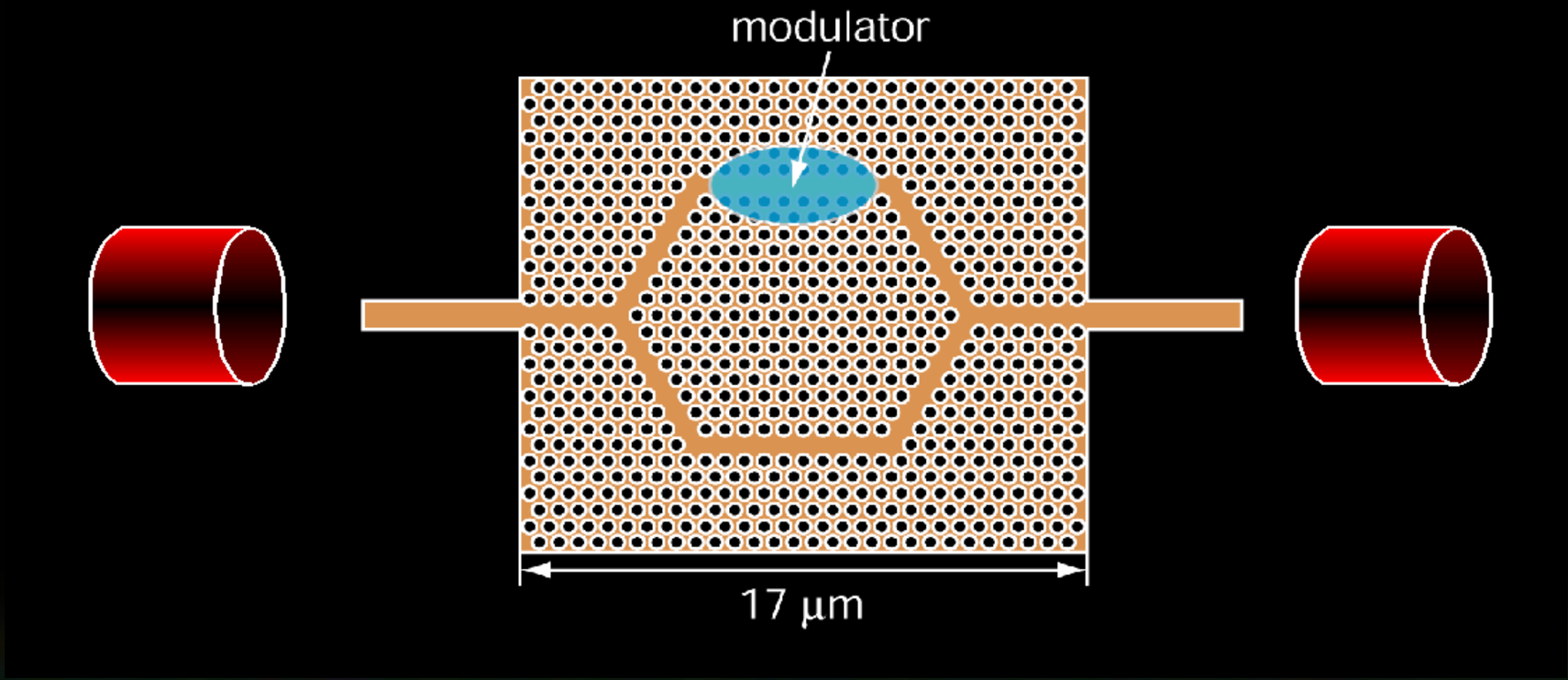
Mode is strongly confined to the center of wg

S.McNab et al, OE, April 2003

Nanophotonics Toolbox (circa 2002)



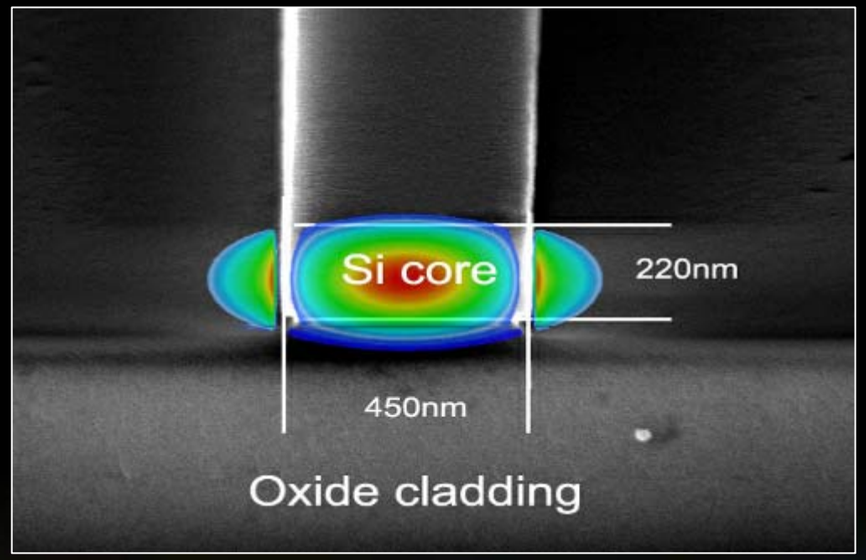
Design of PhC based MZI



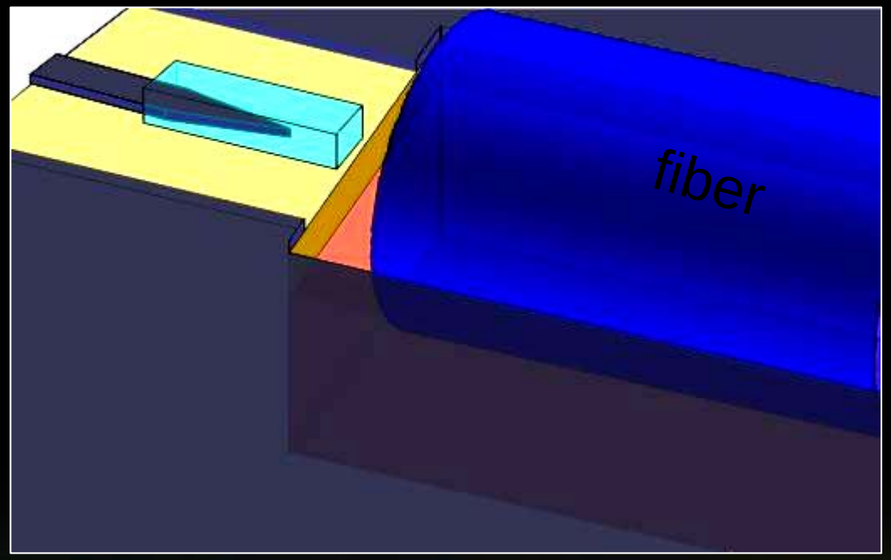
- fiber-to-strip coupler 2
- access strip waveguide 2
- strip-to-PhC couplers 2
- splitter/combiner 2
- sharp bend 4
- phase shifter 1

Single-mode SOI photonic wires

SOI photonic wire



Inverted Taper fiber coupler

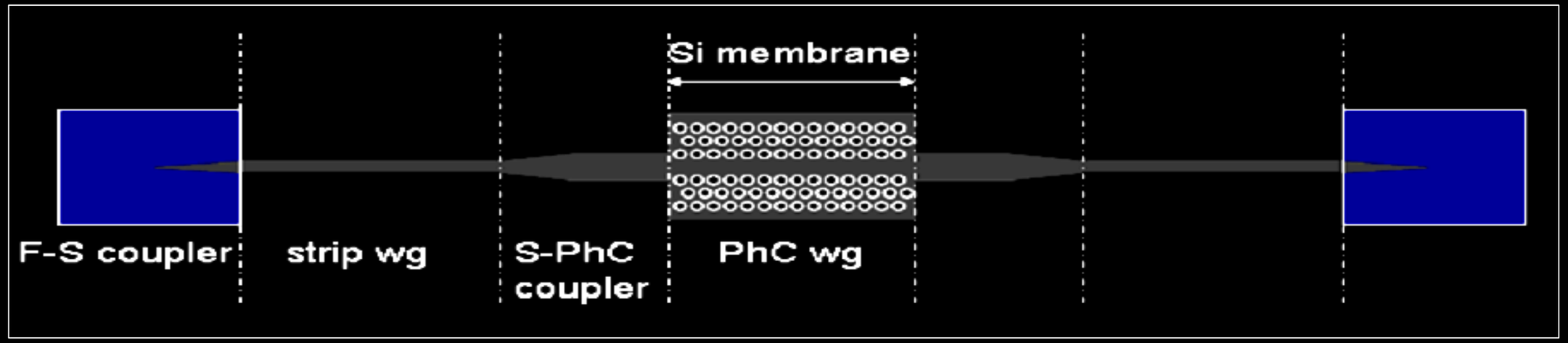


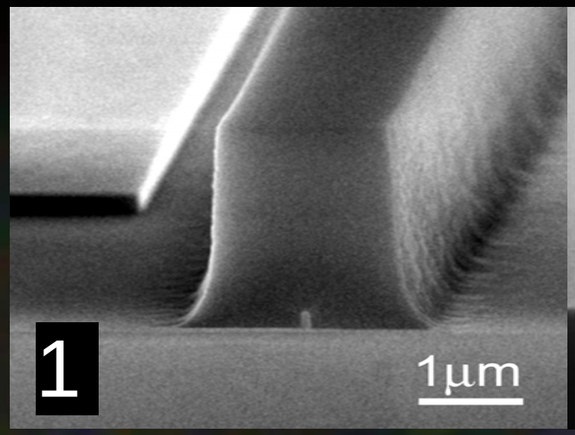
Propagation loss	1.7±0.1 dB/cm
Coupling loss	<0.5 dB/port
Alignment tolerance at 3dB	±1um
Coupling bandwidth	300nm

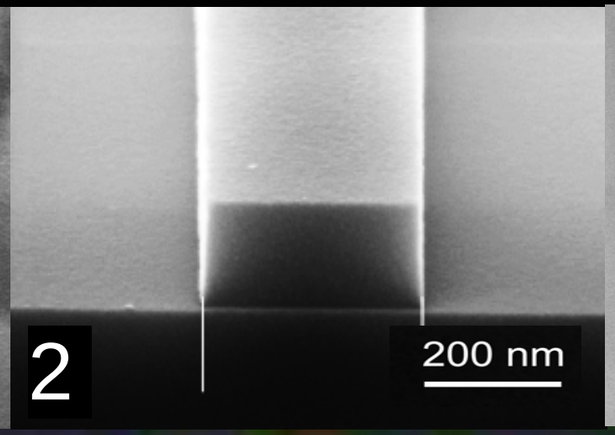
McNab, Moll, Vlasov, Opt. Exp. 11 (2003)

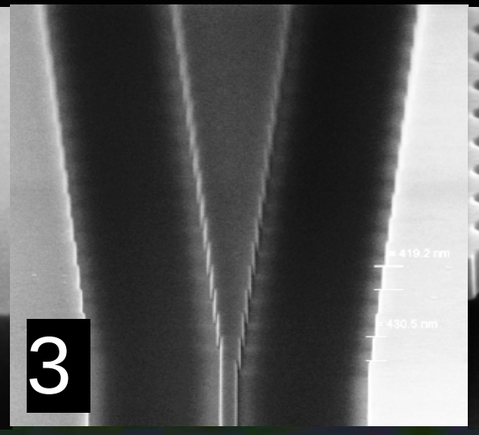
2003 IBM Milestone

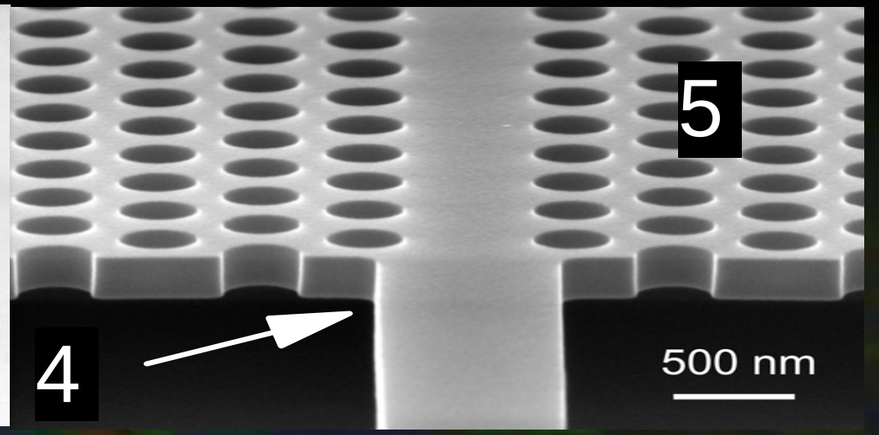
Demonstration of a complete circuit employing photonic crystal waveguides with record low losses 8 ± 2 dB/cm





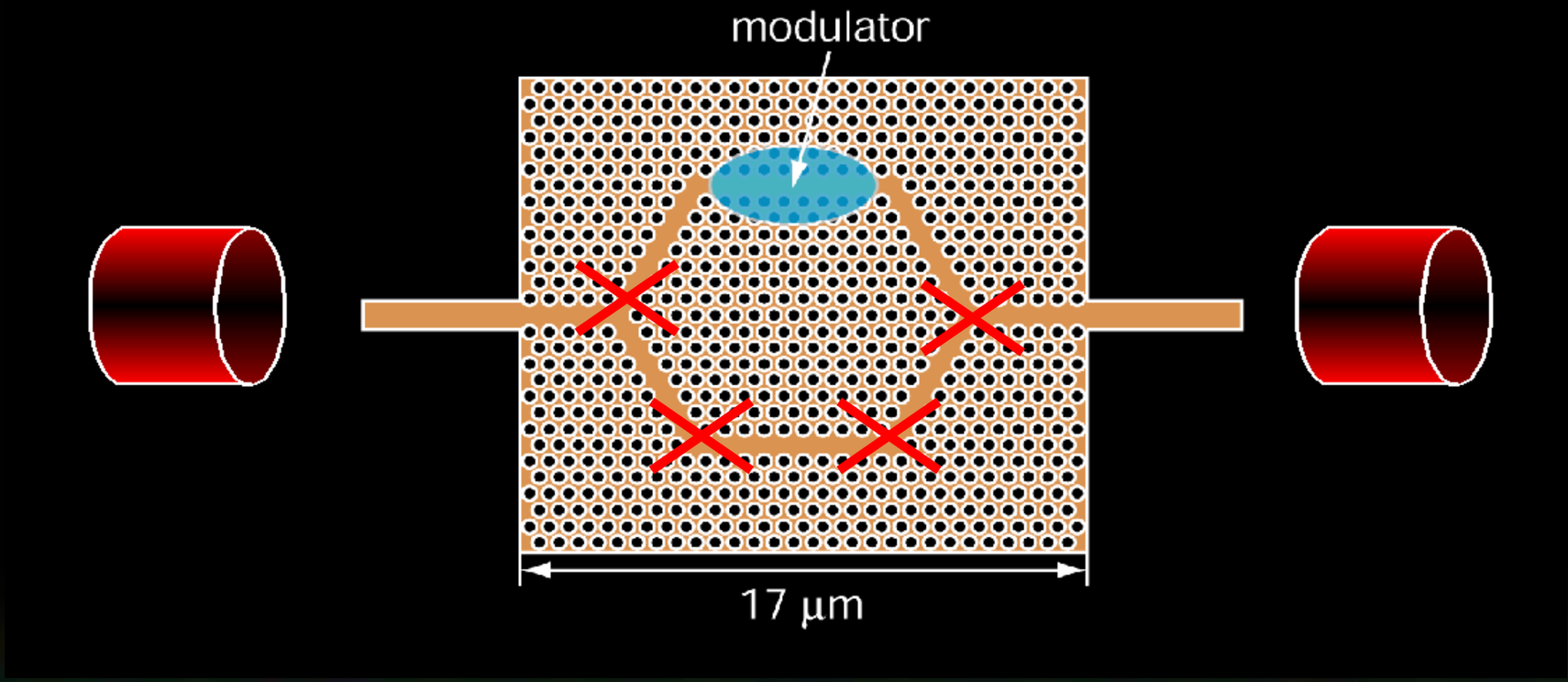






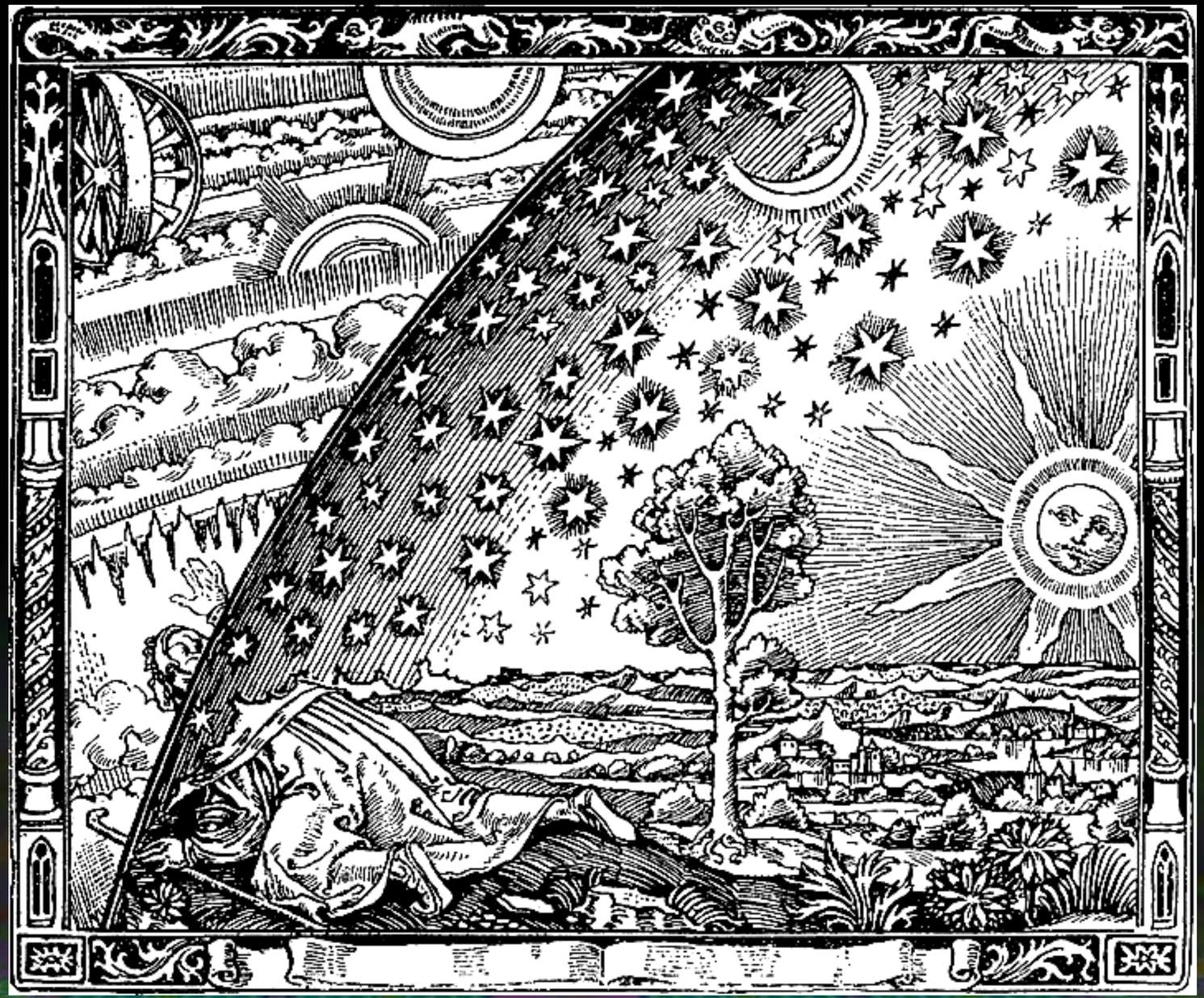
McNab, Moll, Vlasov, Opt. Exp. 11 (2003)

Design of PhC based MZI



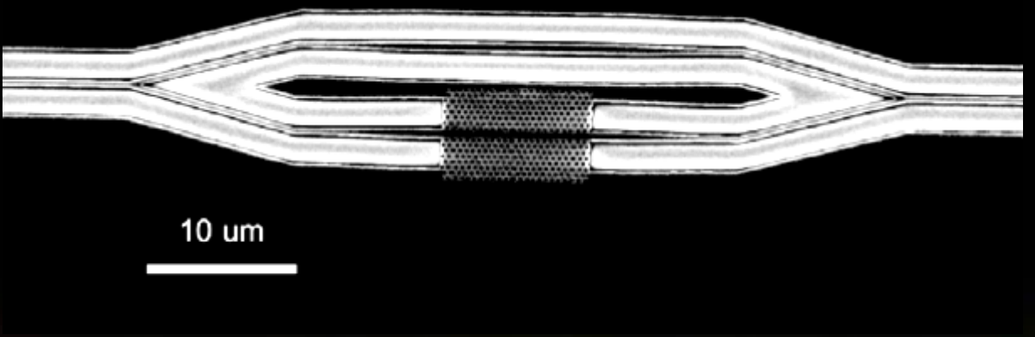
- fiber-to-strip coupler 2
- access strip waveguide 2
- strip-to-PhC couplers 2
- ~~splitter/combiner 2~~
- ~~sharp bend 4~~
- phase shifter 1

Breaking out of the sphere



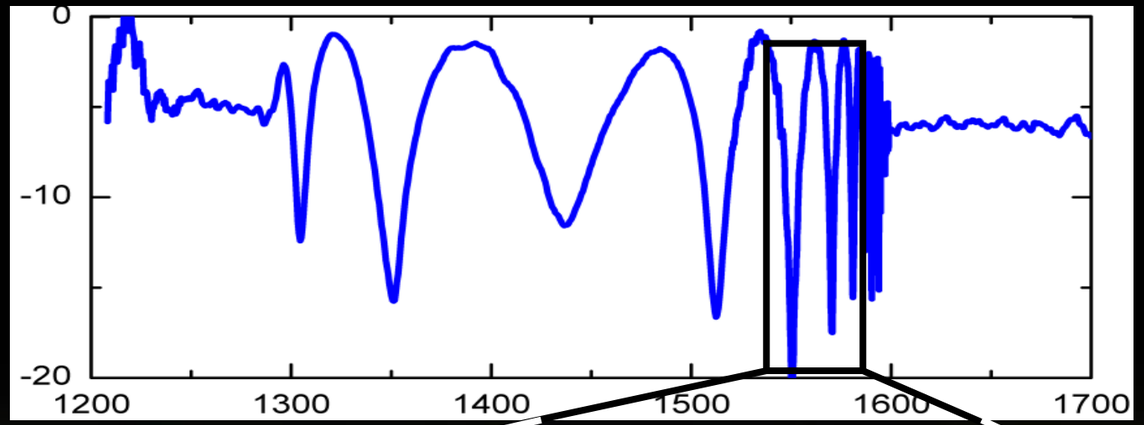
2004 IBM Milestone

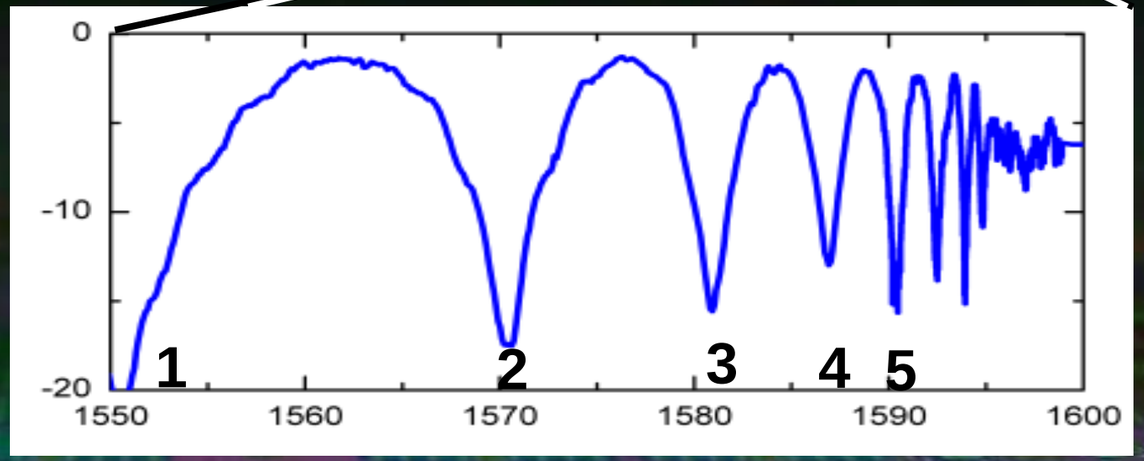
Demonstration of the passive Mach-Zehnder interferometer employing photonic crystal waveguides with losses below 3dB.



PhC Mach-Zehnder Interferometer

Up to 300 π phase shifts





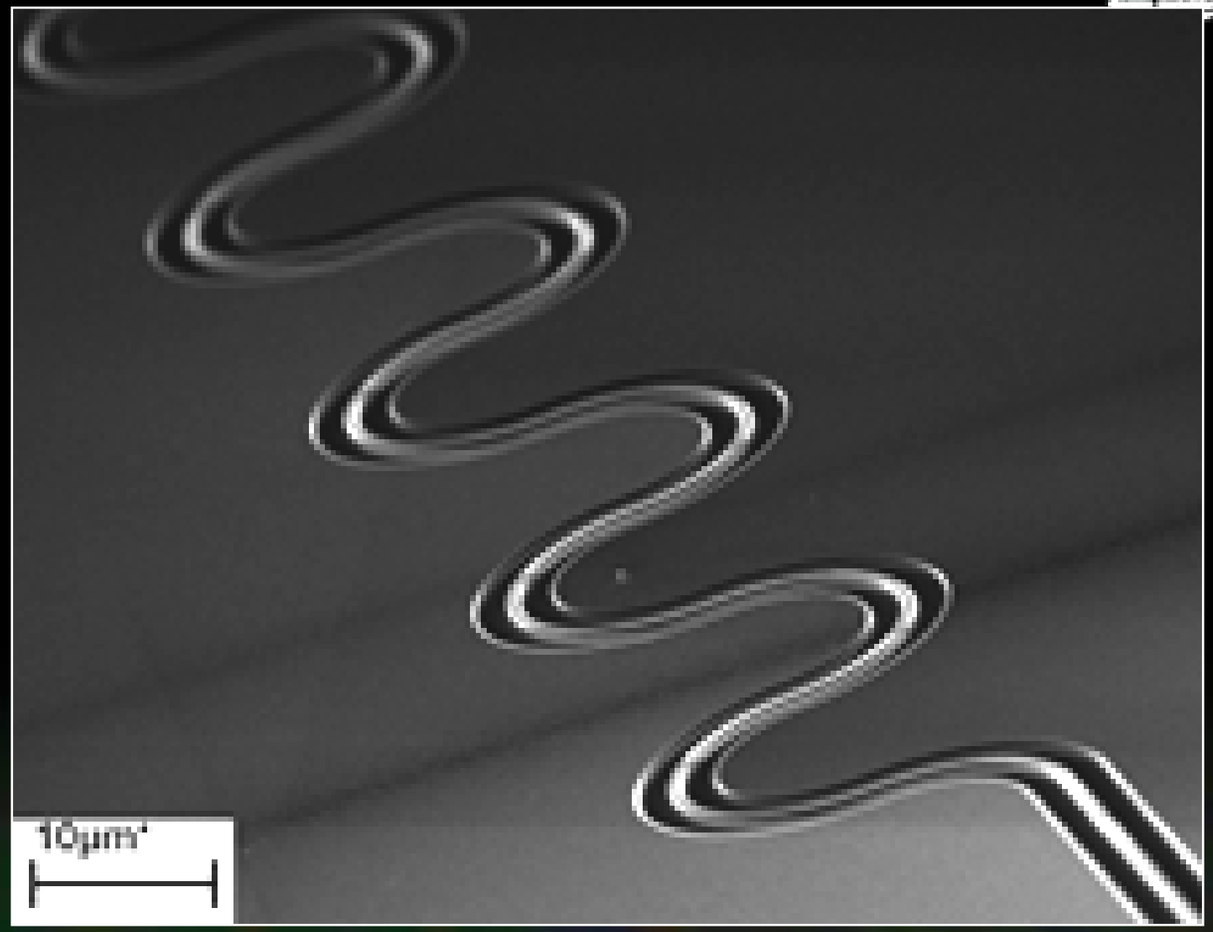
Y.Vlasov et al, Nature, March 2005

Losses in sharp bends

(measured with 20 bends)

R	Losses per 90º bend
1um	0.086±0.005dB
2um	0.013±0.005dB
5um	0.005±0.005dB

Vlasov, McNab, Opt. Exp. 12 (2004)

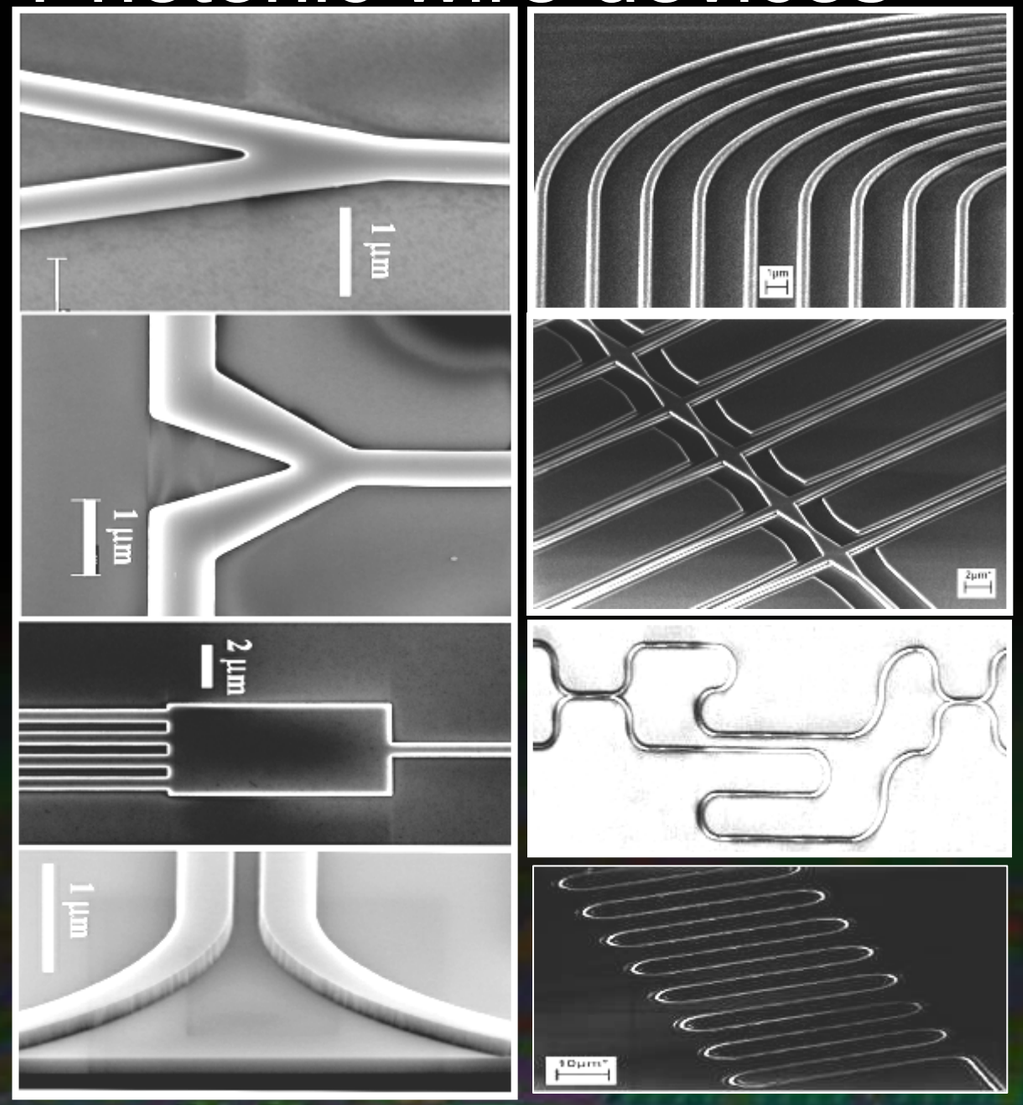


R=6.5um (measured with 280 bends)

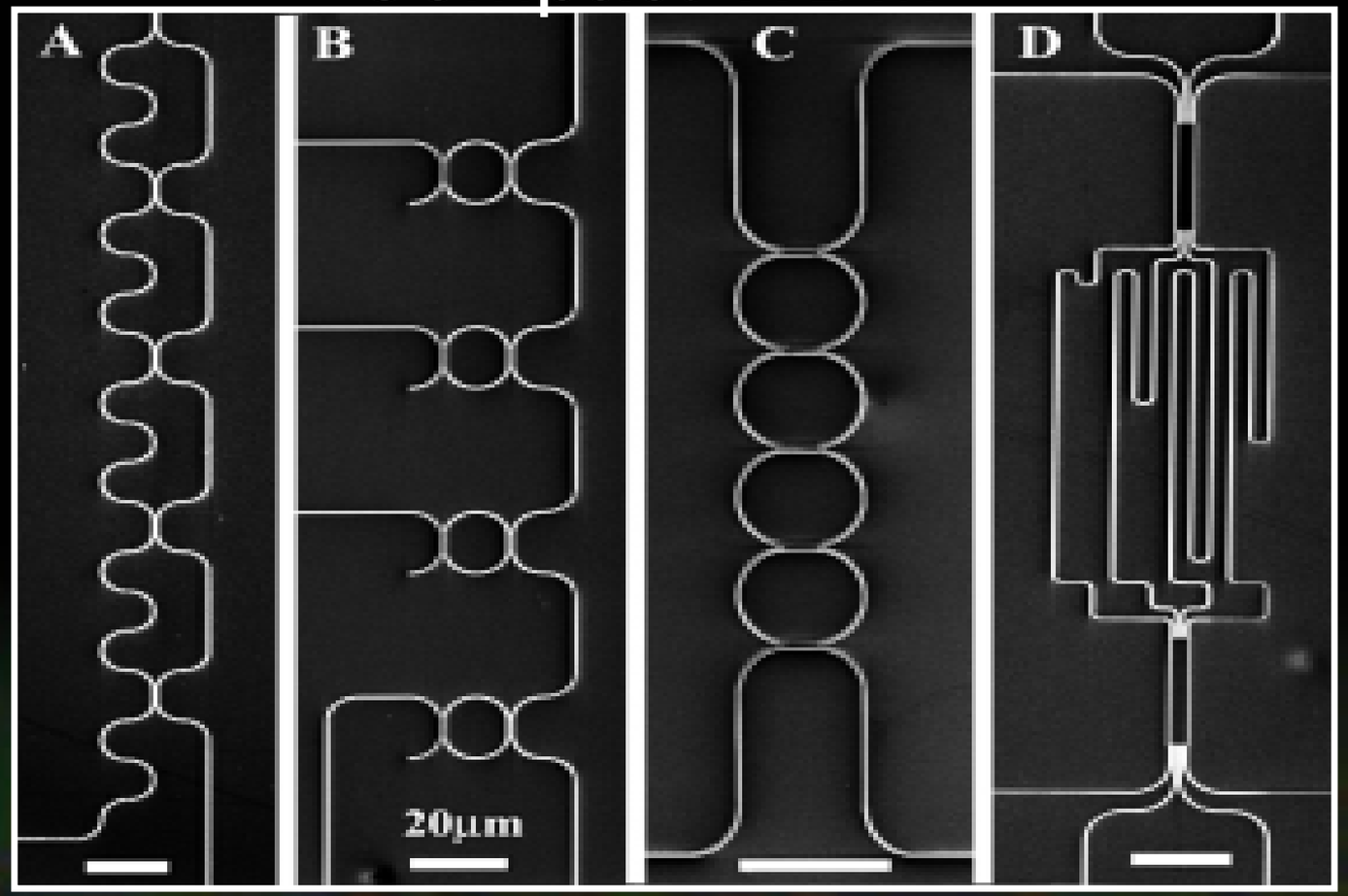
Loss/90° bend 0.0043±0.0005dB

Bandwidth 250nm

Photonic wire devices

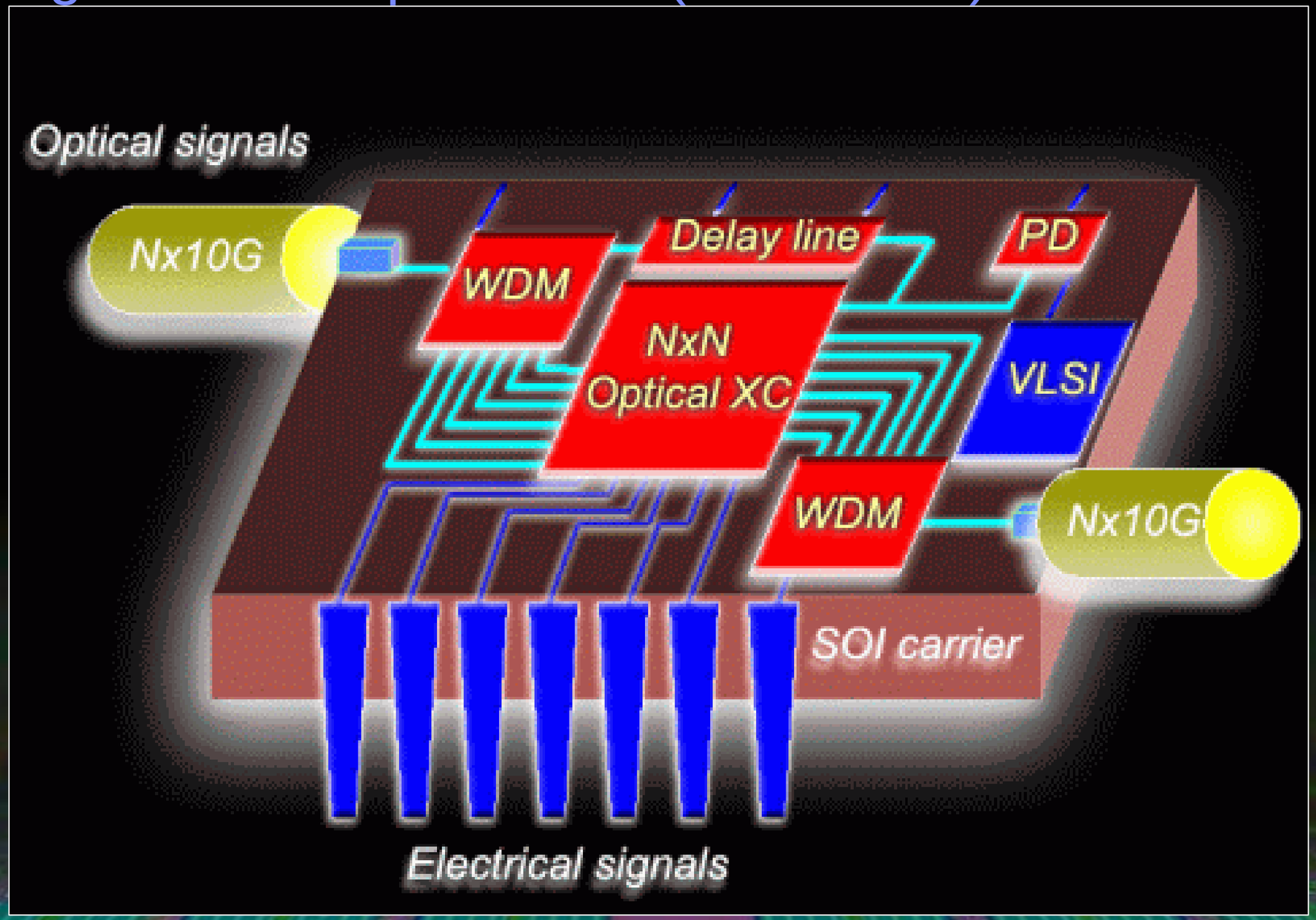


Compact WDM



Footprint is as small as 0.03mm^2

Silicon Integrated Nanophotonics (circa 2004)



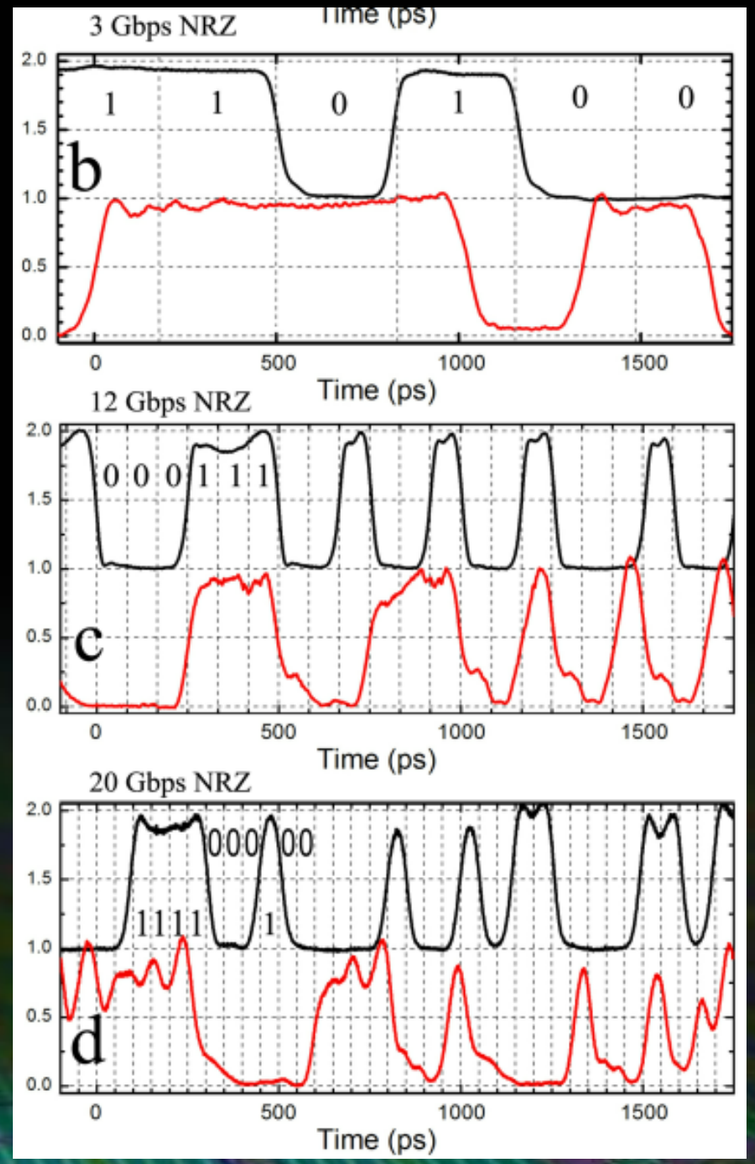
2006 IBM Milestone

Ring resonator delay line

3 Gbps	1.7 bit delay
12 Gbps	6 bit delay
20 Gbps	10 bit delay

- Bandwidth is inversely proportional to delay
- Loss is proportional to delay

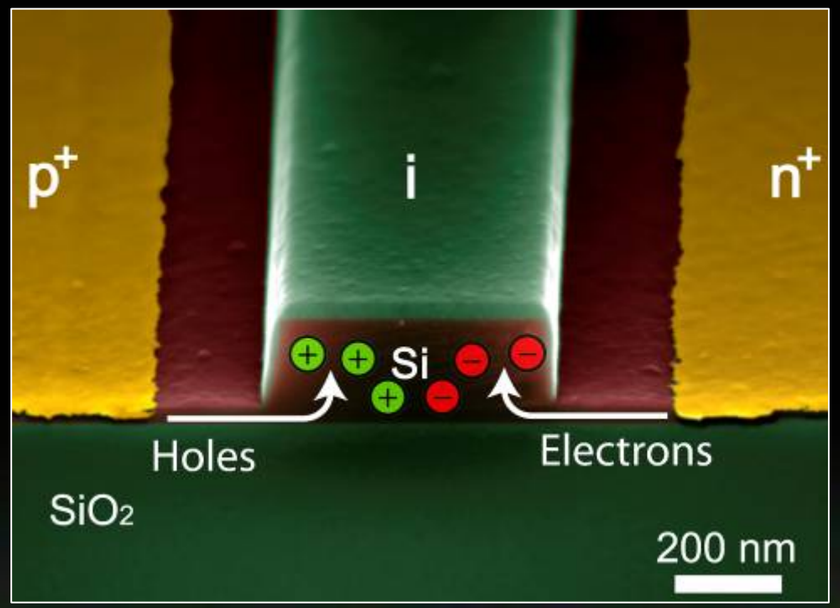
Footprint ←→ Loss
←→ BW ←→ Delay



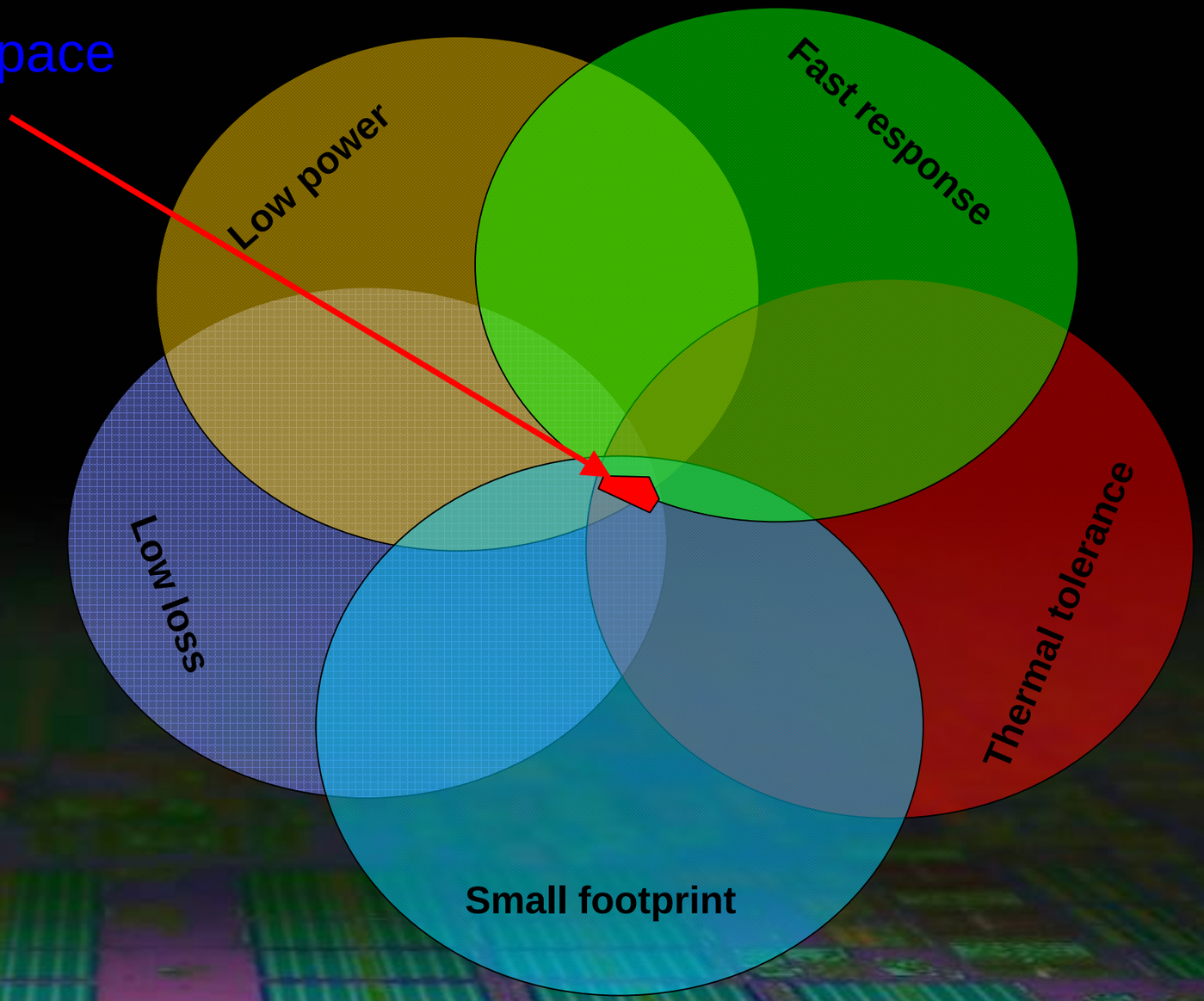
F.Xia et al Nature Photonics 2007

Electrooptic Device Design Space

Modulator design-space



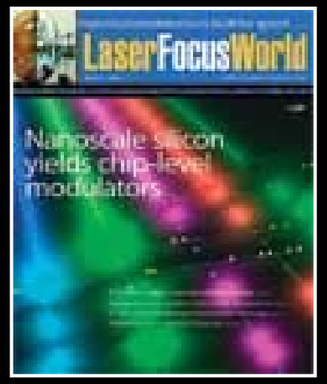
Switching by free-carrier injection



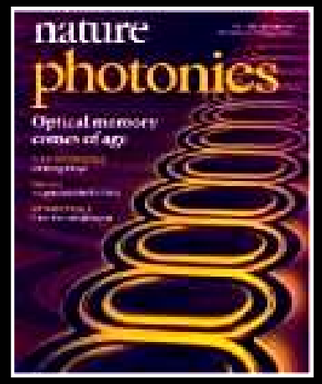
W.Green et al Opt. Exp. 2007

IBM Silicon Nanophotonics – Scientific Impact (2003-2010)

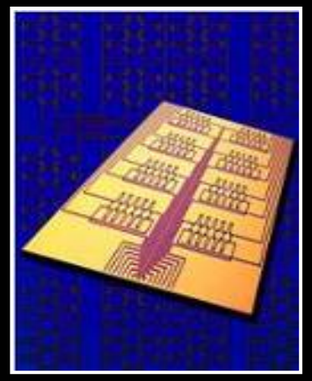
2005
Slow Light



2006
Si Modulator



2007
Optical Buffer



2008
Si Switch

2009
APD Detector

2010
Amplifier

2010
Ge Receiver

Journal papers:	**>60 (including 5 Nature, 6 Invited)**
Conferences:	**>250 (including >100 Invited/Plenary)**
Citation index:	**>4000**
Patents:	**>30**

Fundamental scientific work laid down solid foundation for technology development

Midway upon the journey of our life
I found myself within a forest dark,
For the straight-forward pathway had been lost.

Longfellow translation

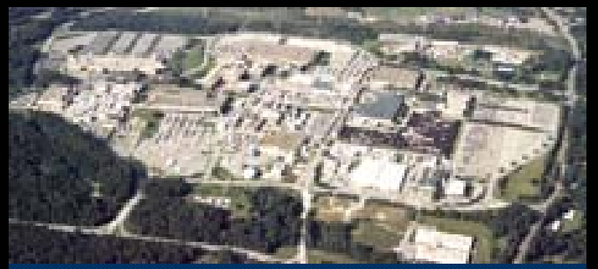
IBM Technology Innovation Pipeline

Fundamental Research

New materials, processes, & devices

- Si Nanowires
- Low Dimensional Carbon Electronics
- Phase Change Memory (PCM)
- Silicon Nanophotonics

IBM Yorktown



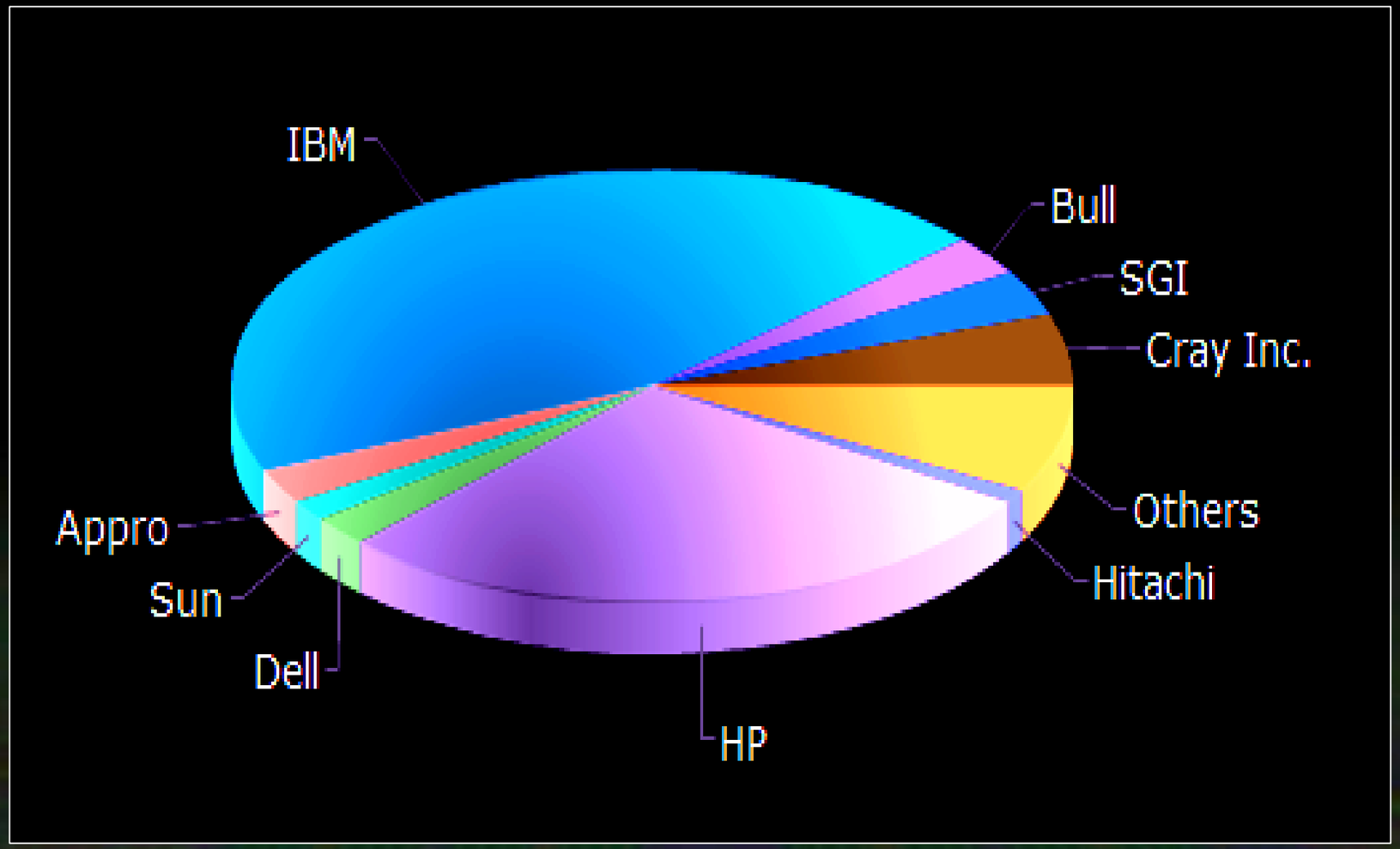
Technology Development

- High Perf SOI eDRAM Technology Alliance
- Foundry Bulk Technology Alliance
- Packaging Alliances

IBM East Fishkill
IBM Burlington
IBM Bromont
Albany Nanotech

Optical Interconnects in IBM Supercomputers

www.top500.org



IBM HPC systems

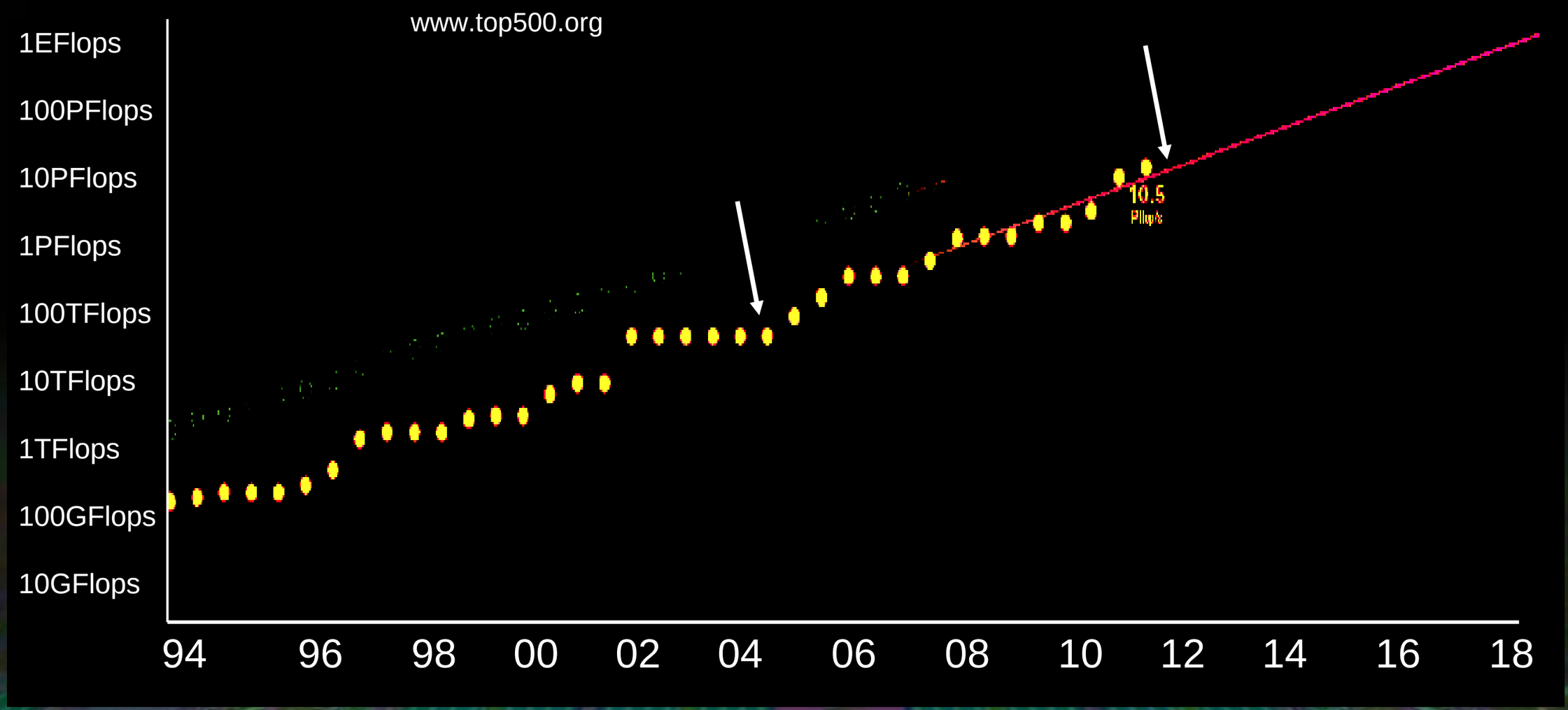
MareNostrum
2006

10,240 PowerPC970 processors, 90 TFlops

IBM P775 system
2011

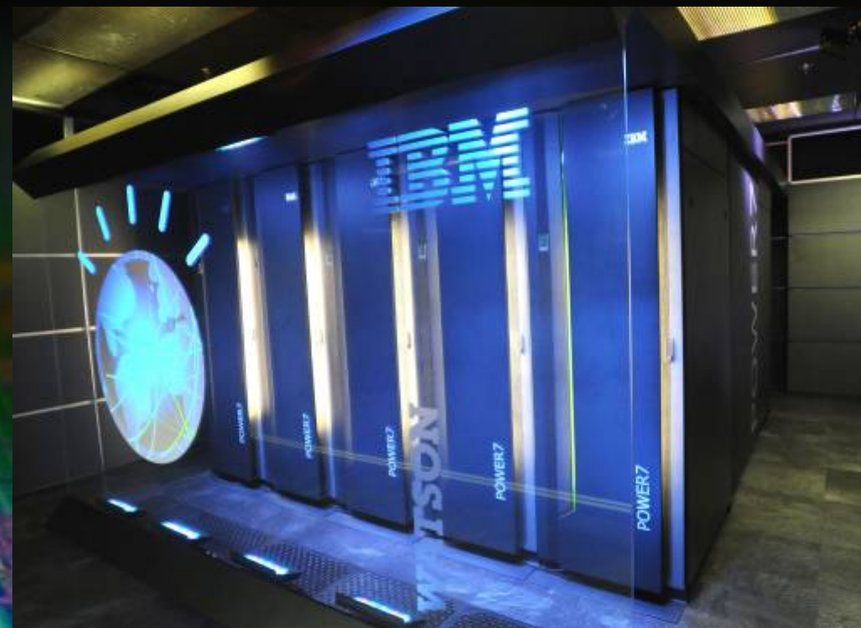
256 P7 processors, 90 TFlops

Top 500 most powerful supercomputers



Watson – questions answering supercomputer

Medical diagnostics
Market predictions
Weather forecast
.....

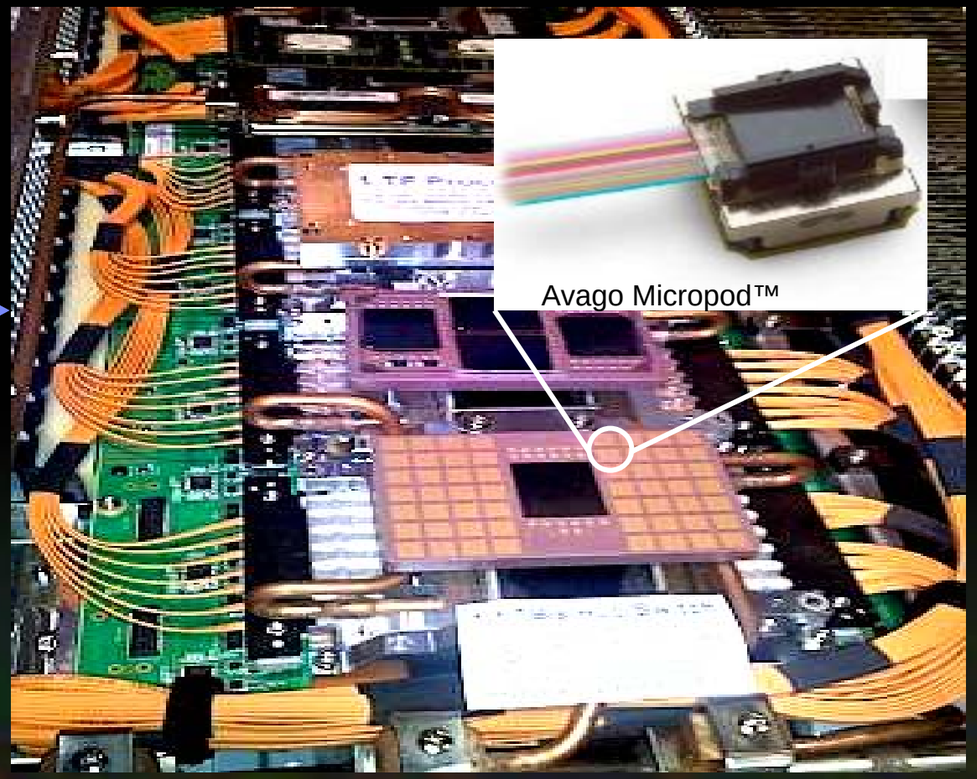


From 5K to 1M fiber links in the system

2006

MareNostrum
~5K fiber cables

2011



P775 system
~500K fiber cables

Cost and Power per bit (unidirectional)

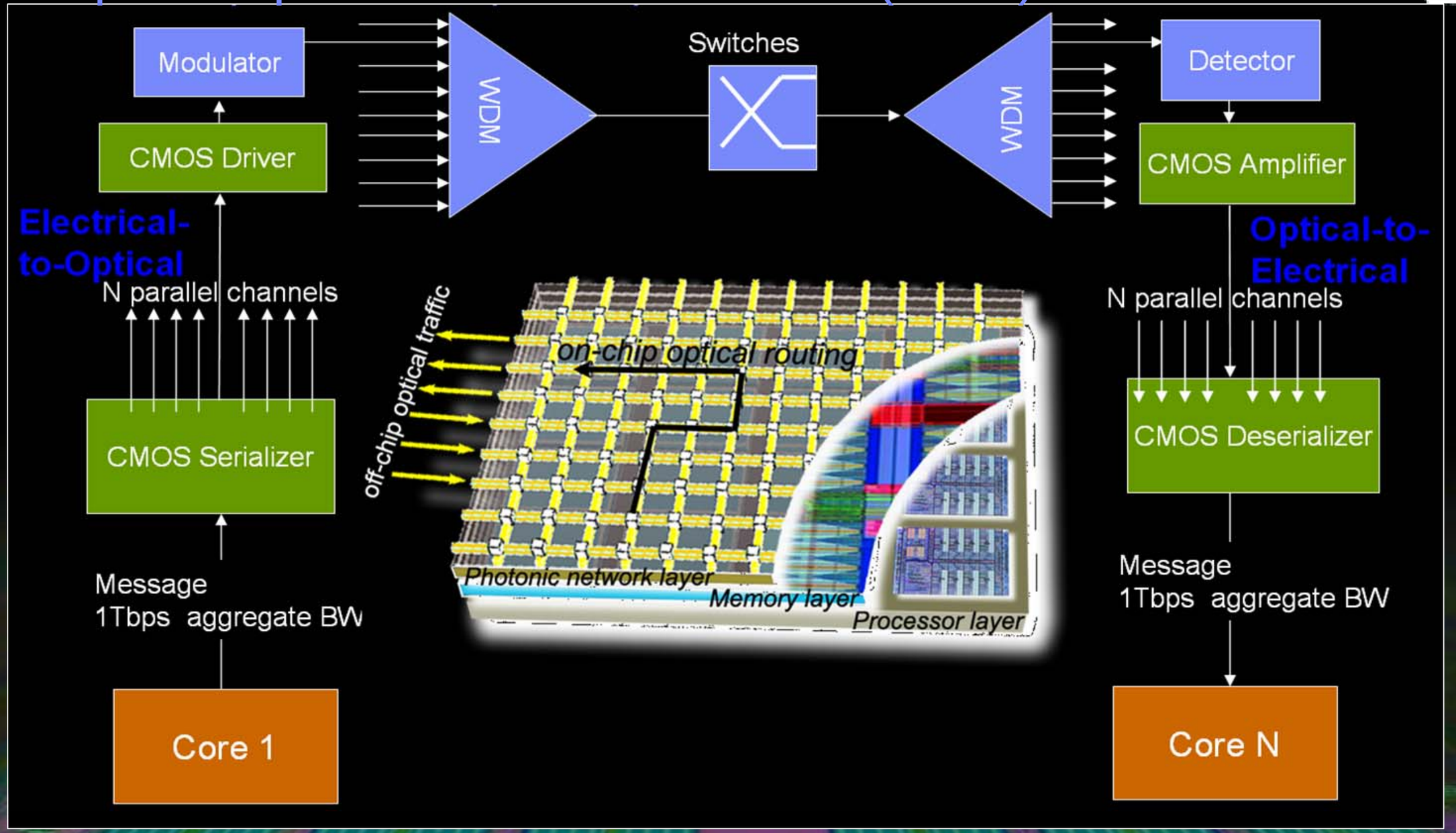
Year	Peak Performance	number of optical channels	Optics Power Consumption	Optics Cost
2008	1PF	48,000 (@ 5Gb/s)	50mW/Gb/s (50pJ/bit)	$10,000 per Tb/s
2012	10PF	$2x10^6$ (@ 10Gb/s)	25mW/Gb/s	$1,100 per Tb/s
2016	100PF	$4x10^7$ (@ 14-25 Gb/s)	5mW/Gb/s	$170 per Tb/s
2020	1000PF (1EF)	$8x10^8$ (@ 25 Gb/s)	1mW/Gb/s	$25 per Tb/s

Acknowledgment: A. Benner, J.Kash

- Future directions for optical cables:
  - –Lower cost (reducing >60%/year)
  - –Much more BW (increasing >210%/year)
  - –Much lower power (improving >45%/year)
- New technologies needed

Follow the YBR

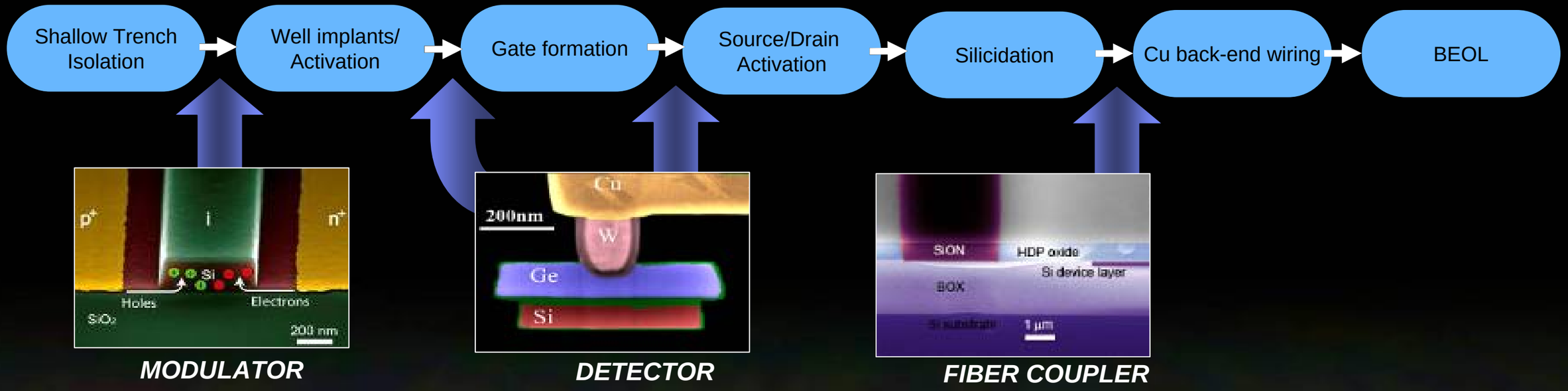
Off-Chip Nanophotonics Interconnects (2006)



Goal: Integrate Ultra-dense Nanophotonics Circuits with CMOS chip

IBM manufacturing process integration

Front-end photonics integration



MODULATOR ***DETECTOR*** ***FIBER COUPLER***

- ✓ Most of the mask levels and processing modules are shared
- ✓ Minimal additional photonics modules added

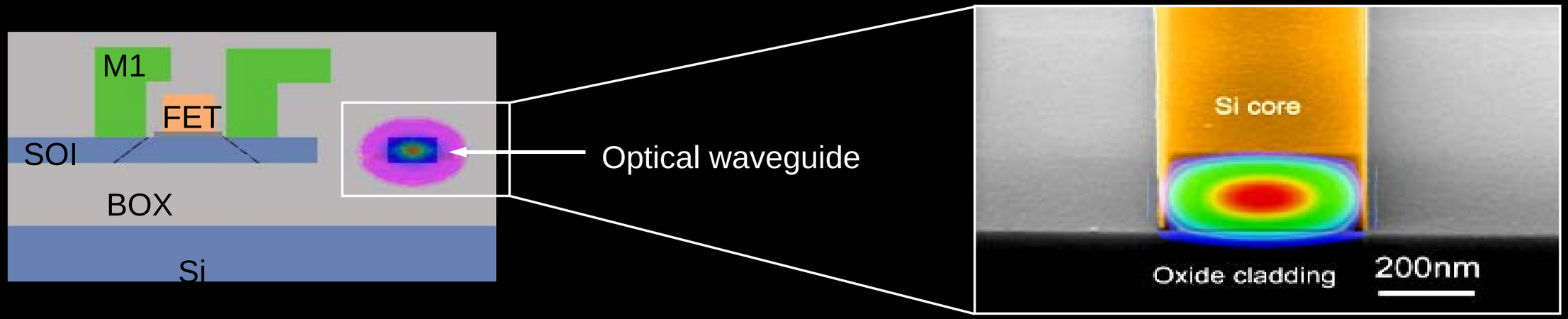
W.Green, et al, SEMICON Japan 2010;

S.Assefa et al OFC 2011

IBM press-release Dec.2010

Over 40 base patents

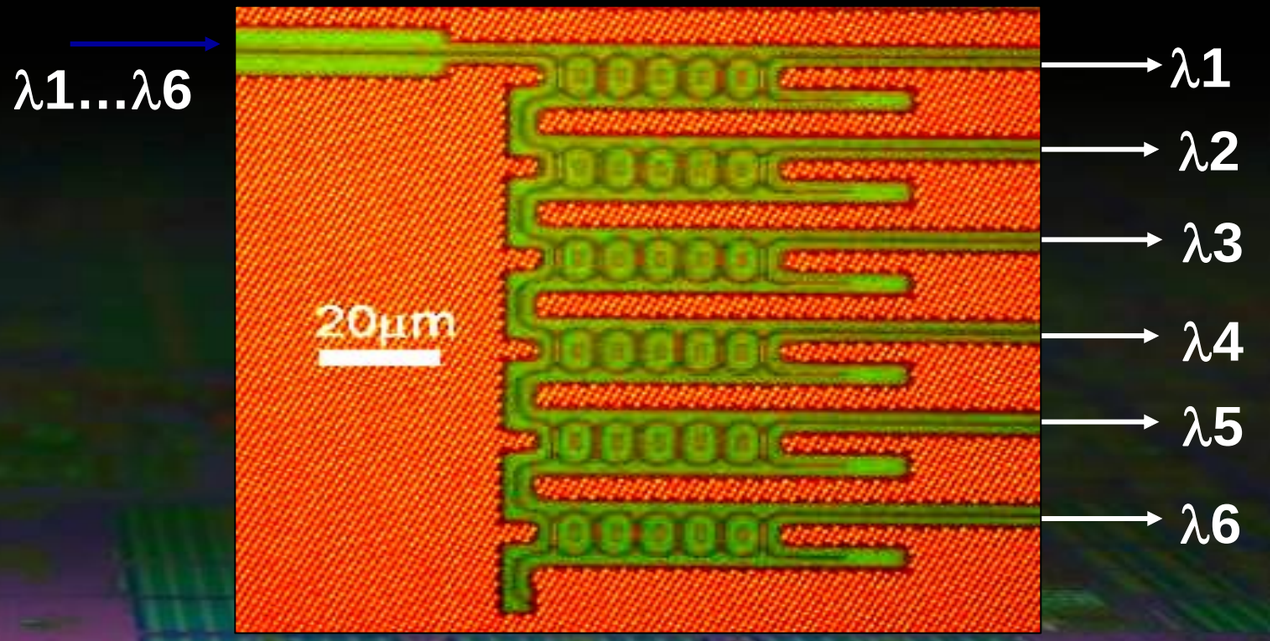
CMOS front-end monolithic Nanophotonics integration



→ Nanophotonics sharing Si layer with FET body

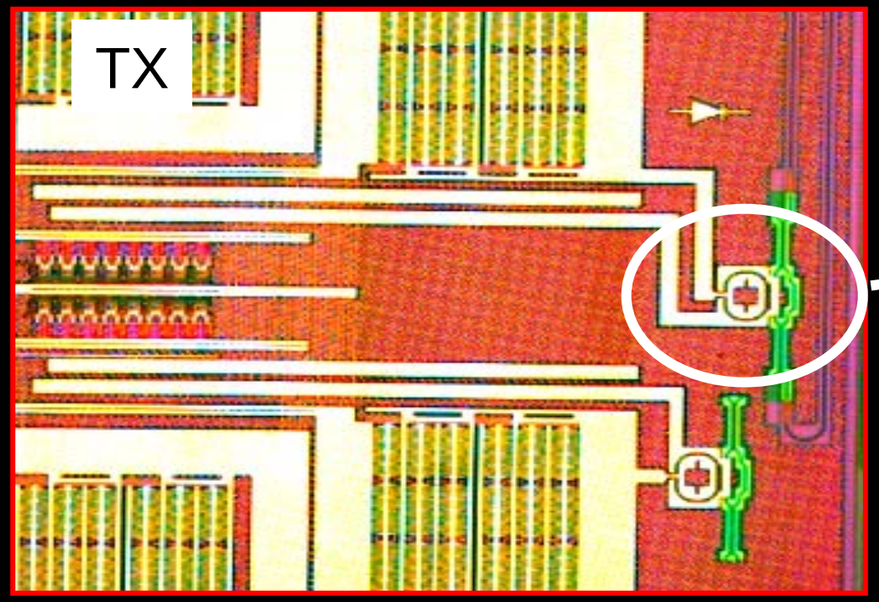
Advantages:

- ✓ Deeply scaled Nanophotonics
- ✓ Most dense integration with CMOS
- ✓ Ultra-low power optical interconnects
- ✓ Same mask set, standard processing
- ✓ Same design environment (e.g. Cadence)
- ✓ Same EDA tools and design flow
- ✓ In-line system-level testing

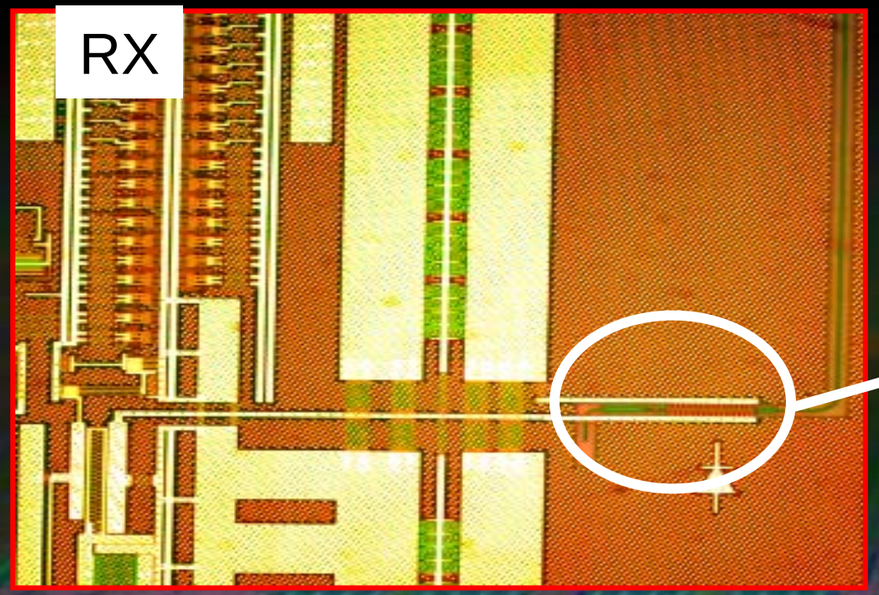


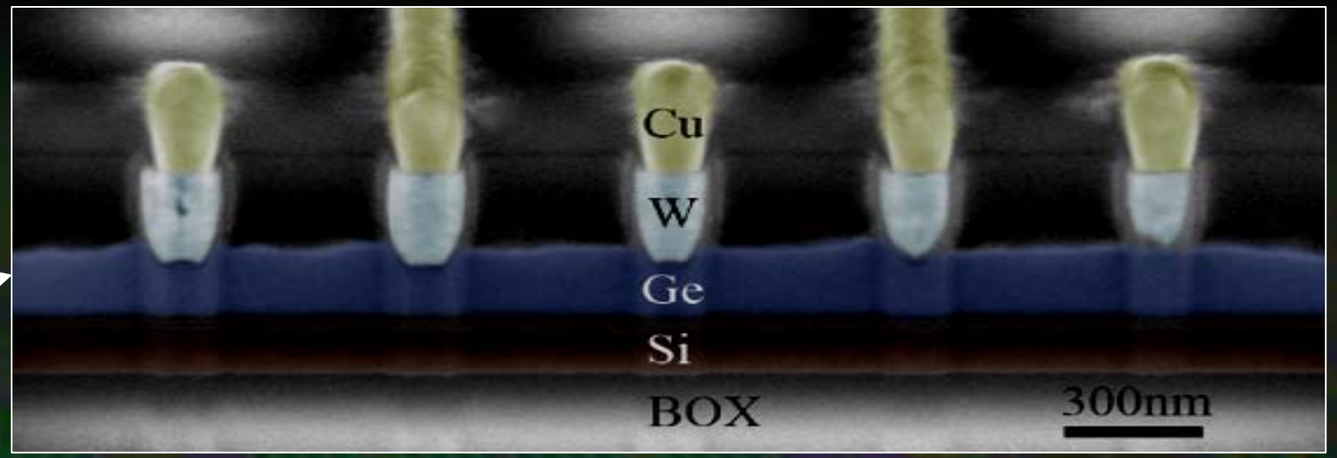
6-channel WDM

SNIPER hardware includes complete optical link



Modulator (25Gbps, 32Gbps option in testing)

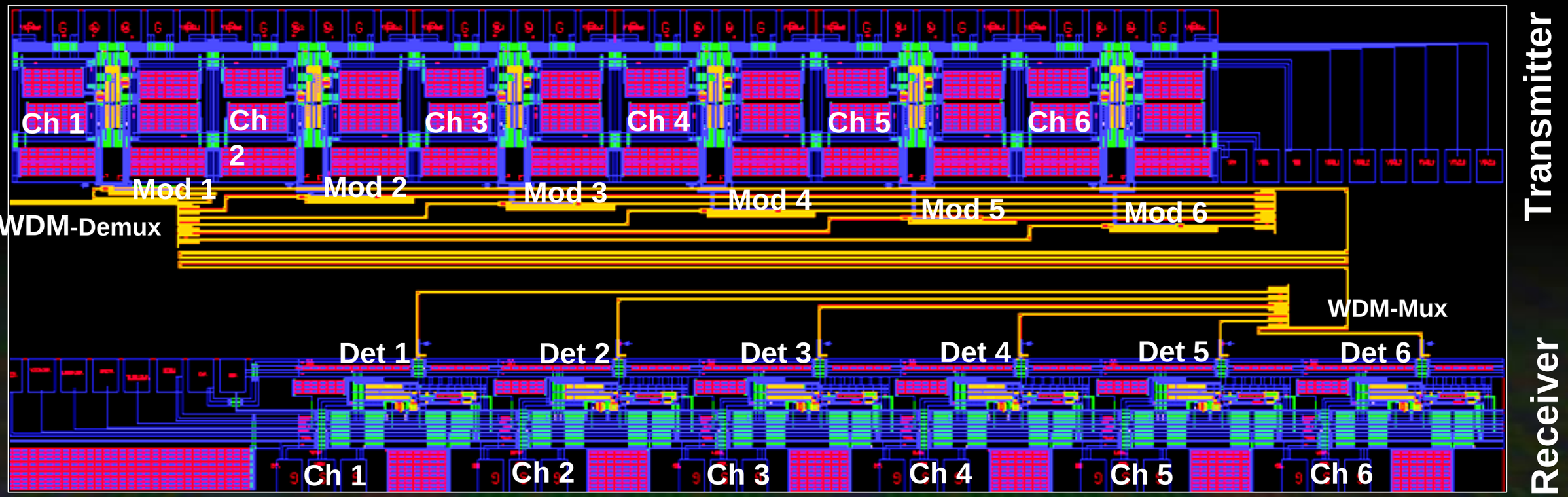




Ge Detector (25Gbps, 40Gbps option in testing)

Co-design of Photonics and CMOS

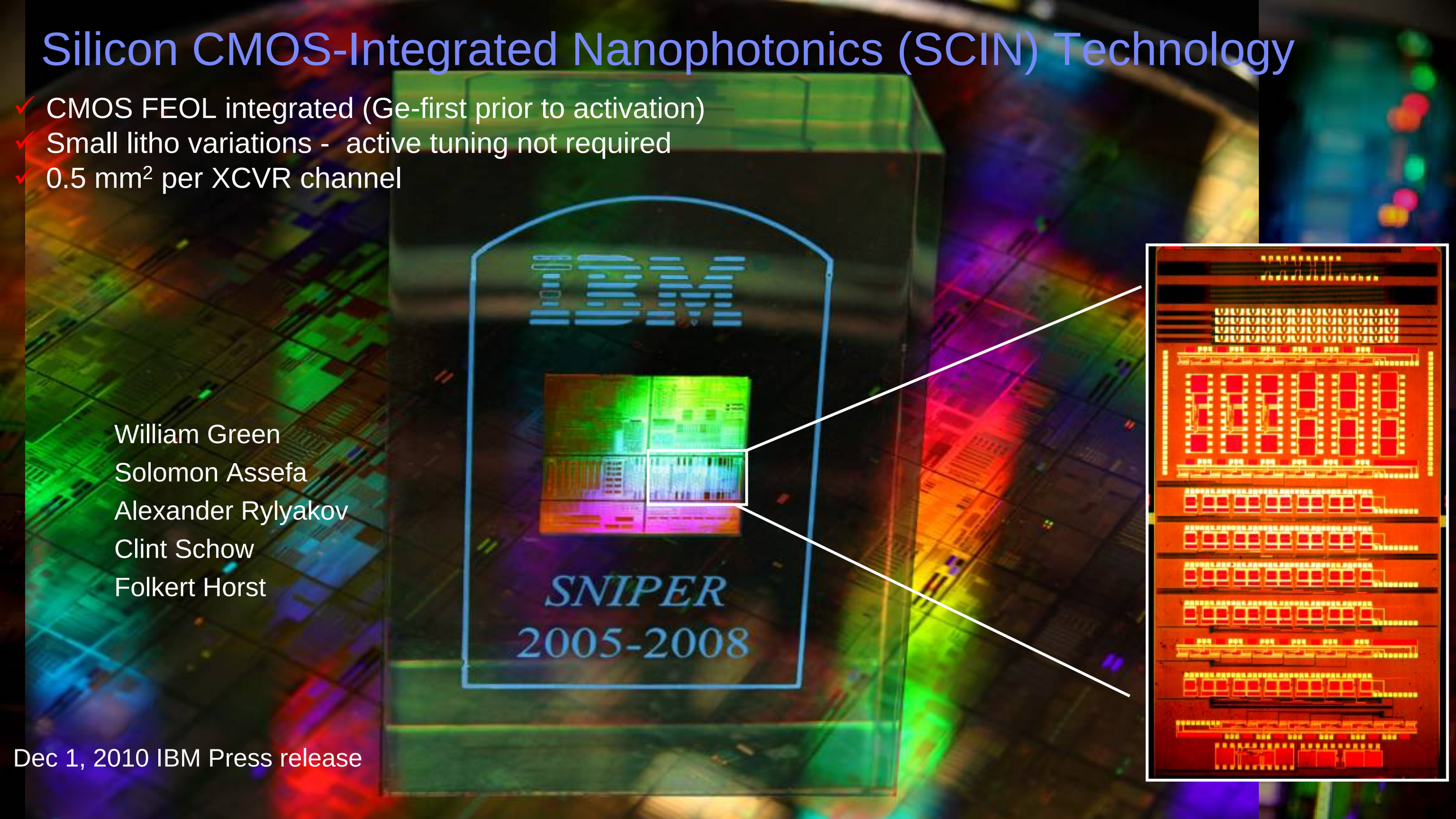
- Library of photonic components
- Photonics-enabled design rules
- Photonics-enabled DRC, LVS, modeling



✓ Allows to layout complex CMOS and Nanophotonics circuits

Silicon CMOS-Integrated Nanophotonics (SCIN) Technology

- ✓ CMOS FEOL integrated (Ge-first prior to activation)
- ✓ Small litho variations - active tuning not required
- ✓ 0.5 mm^2 per XCVR channel



William Green
Solomon Assefa
Alexander Rylyakov
Clint Schow
Folkert Horst

Dec 1, 2010 IBM Press release

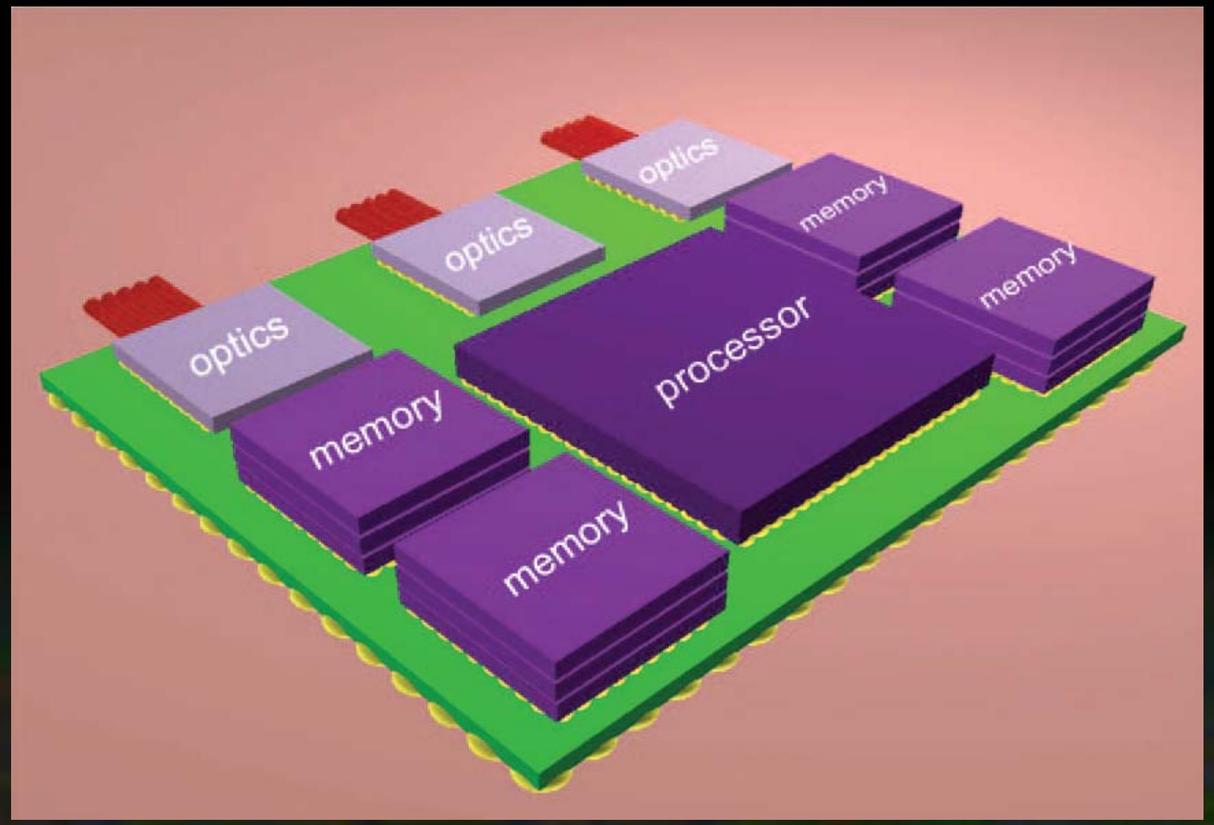
Road mapping

Applications ←→ Products ←→ Markets ←→ NRE ←→ ←→ Pricing ←→ ROI

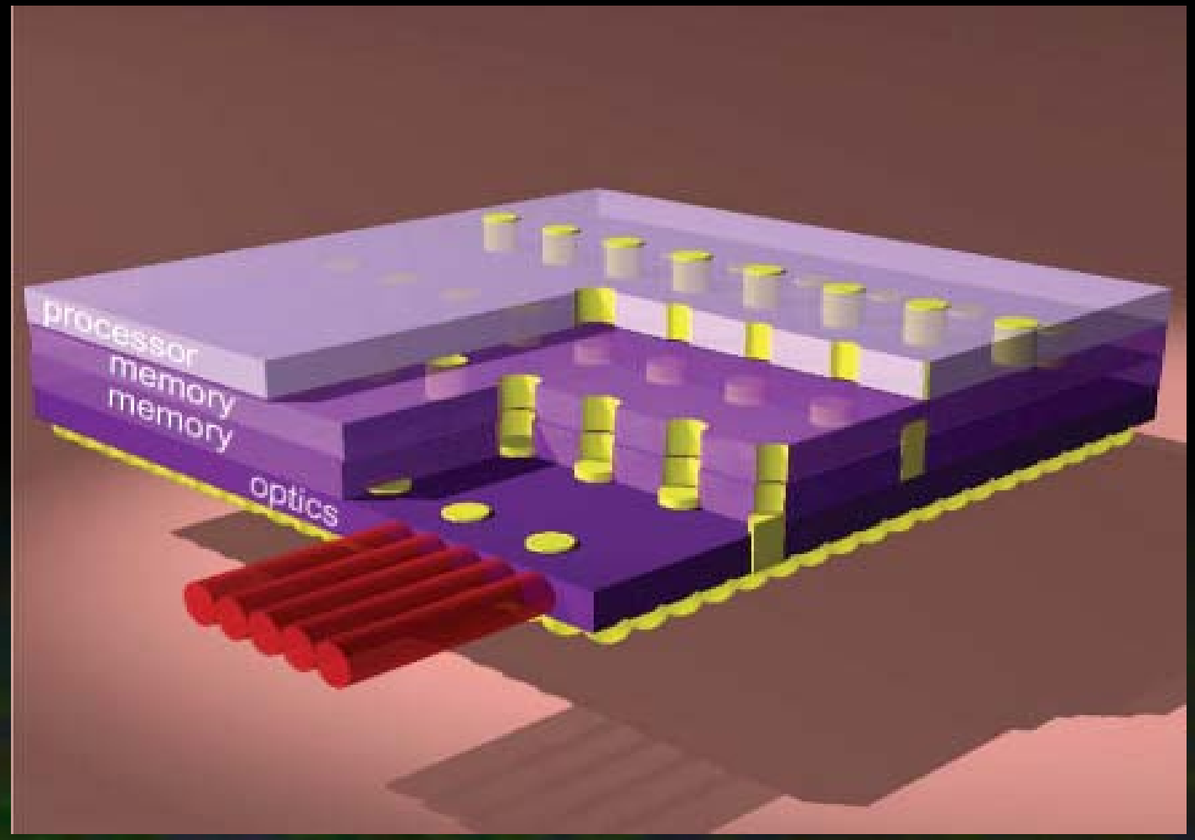
Product ←→ Performance ←→ Top-level design ←→ Component specifications ←→ ←→ Design choice ←→ Manufacturability ←→ Reliability ←→COST, COST , COST

Map of the road

Circa 2015

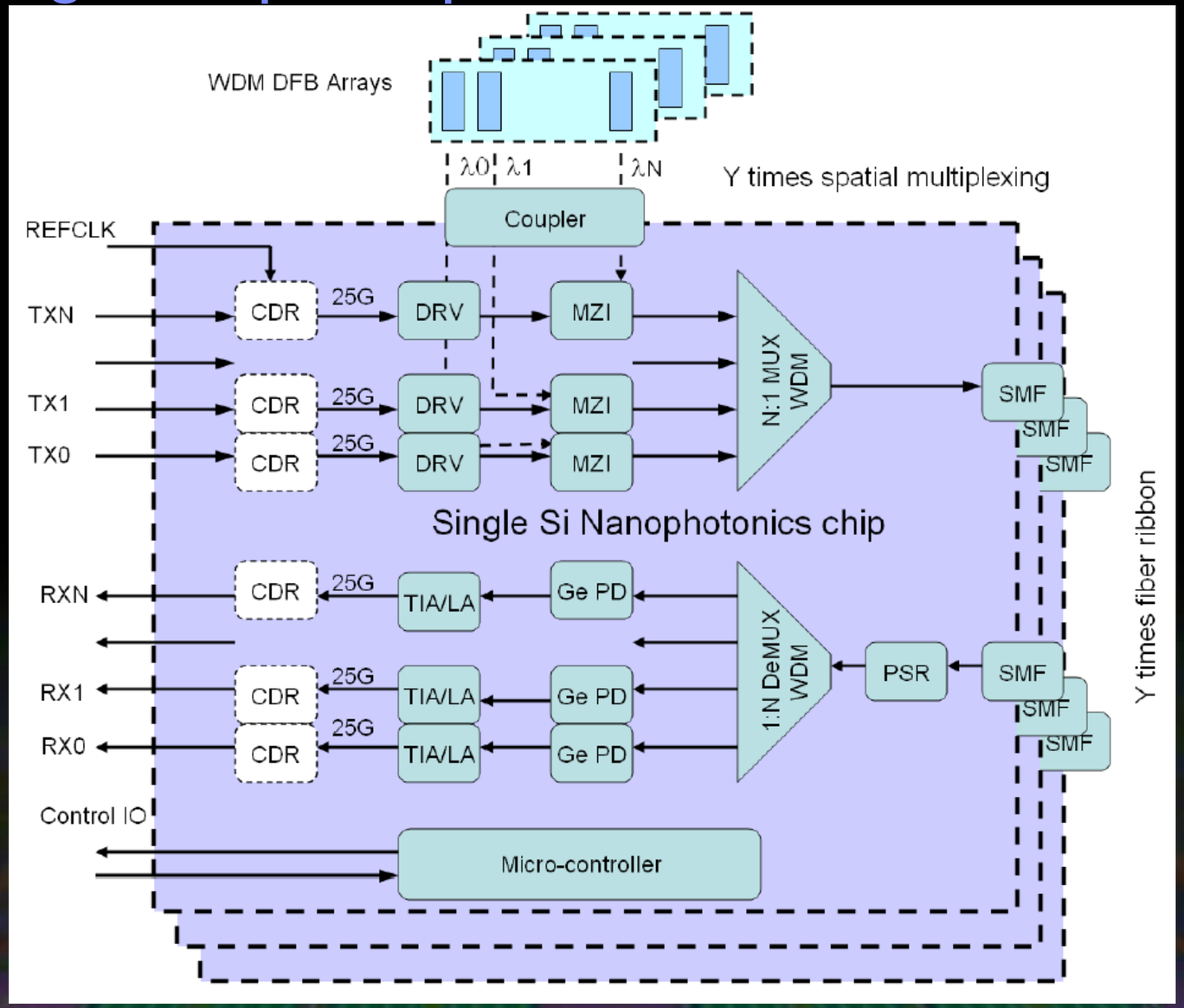


Circa 2020



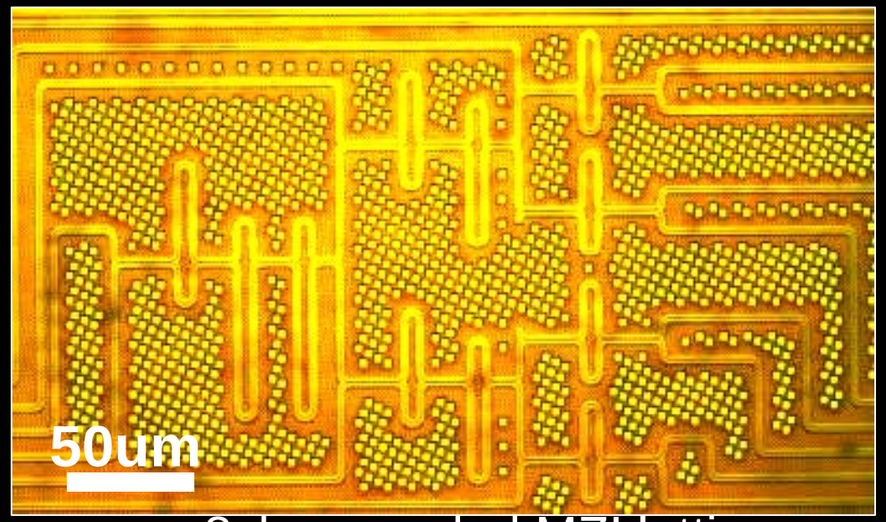
"Technologies for Exascale systems", P. Coteus, J.Knickerbocker, C. Lam, and Y. Vlasov
IBM Journ. R&D, 55, No.5, 2011

Concept of a single-chip 1Tbps transceiver

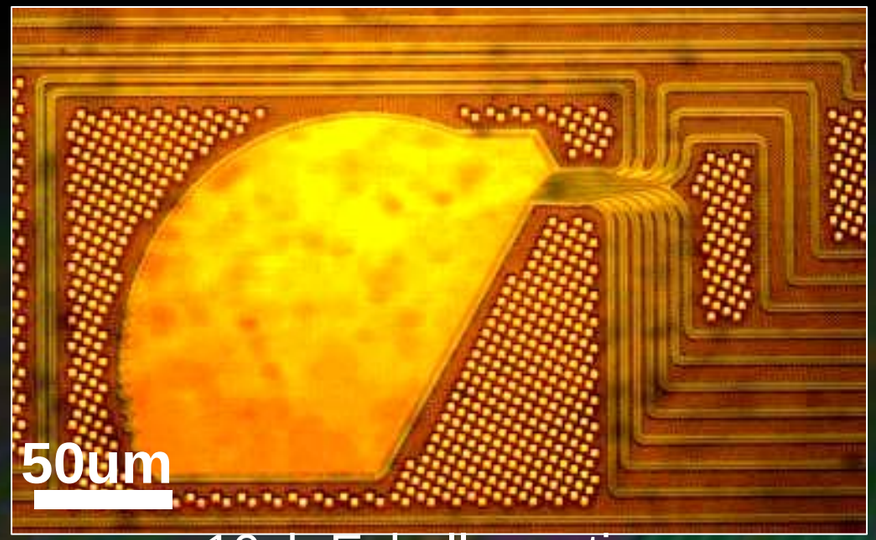


Y.Vlasov "Si Nanophotonics for Computercom beyond 100G" IEEE Comm. Mag. , March 2012,

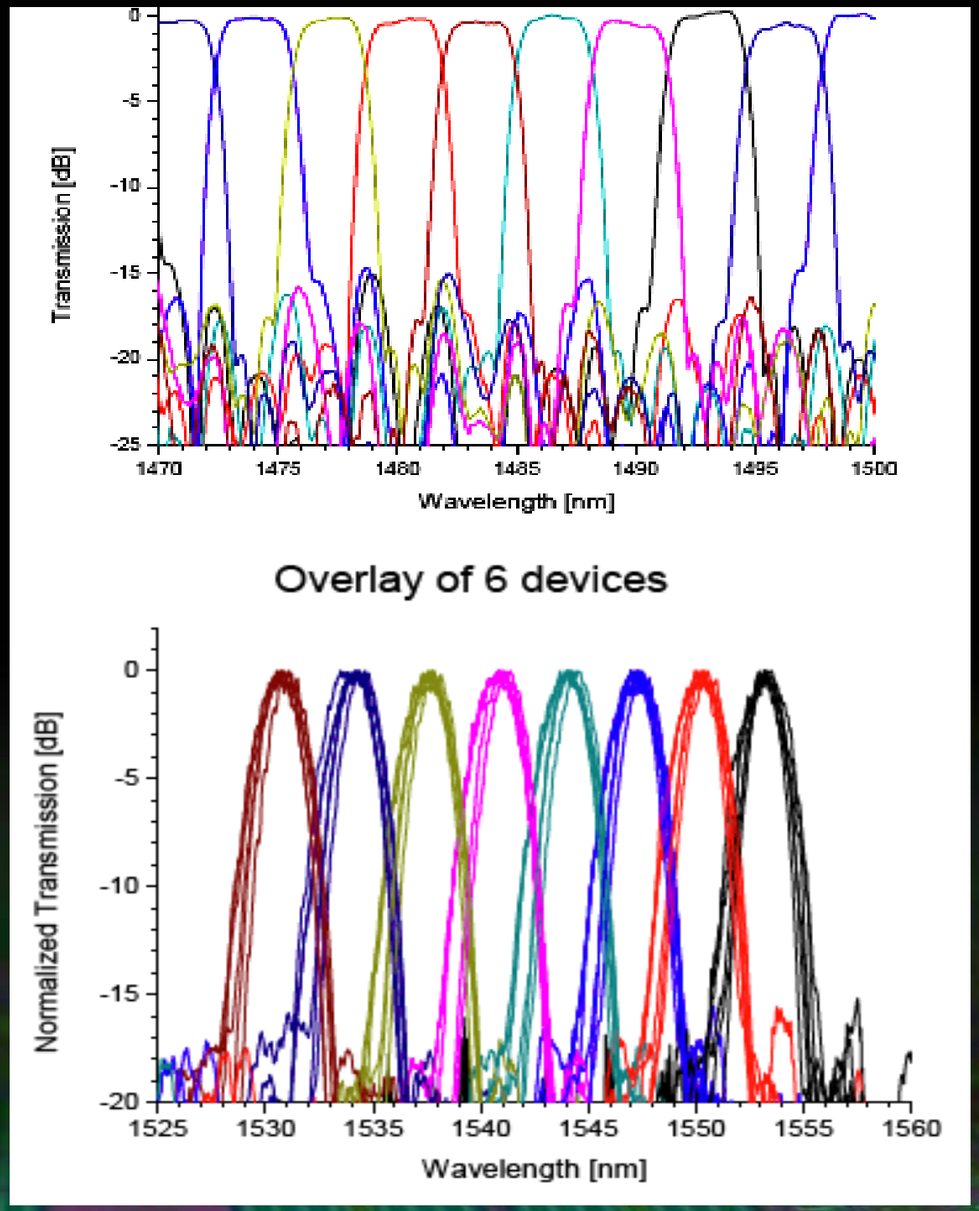
WDM multiplexers



8ch cascaded MZI lattice



10ch Echelle grating

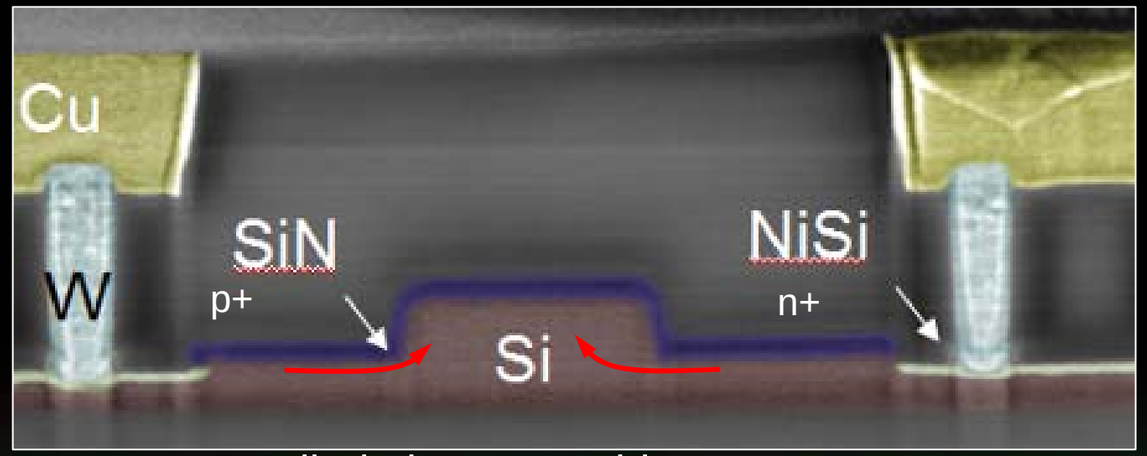


Folkert Horst (IBM Zurich) Invited talk OFC 2011

Modulator

Need 5pC for PI phase shift in Si waveguide

Capacitance per unit length is the key → PN-junction engineering



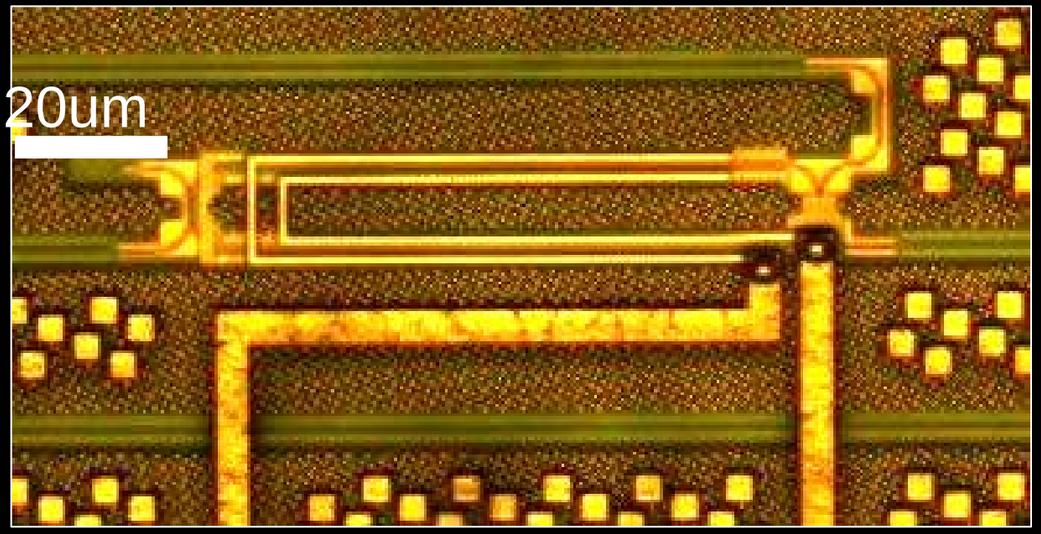
PN diode in reverse bias

A. Liu et al., Optics Express **15**, 660 (2007).
D. Marris-Morini et al., Optics Express 16, 334 (2008).
S. J. Spector et al., Optics Express **16**, 11027 (2008).
J. W. Park et al., Optics Express **17**, 15520 (2009).
P. Dong et al., Optics Express **17**, 22484 (2009)
T.-Y. Liow et al., JSTQuantum Electron. **16**, 307 (2010).
J. Fujikata et al., OFC 2010
D. M. Gill et al., JST. Quantum Electron. **16**, 45 (2010).
M. R. Watts et al., JST Quantum Electron. **16**, 159 (2010).

	$V_\pi \cdot L$
Intel	4 V·cm
CNRS/CEA-LETI	5 V·cm
Lincoln Labs/MIT	4 V·cm
IME A*STAR PN	2.5 V·cm
Bell Labs/BAE Systems	2 V·cm
ETRI, South Korea	1.8 V·cm
Kotura/Oracle	1.5 V·cm
Sandia Labs	1 V·cm
IME A*STAR MOSCAP	0.5-0.67 V·cm
IBM*	0.6 V·cm

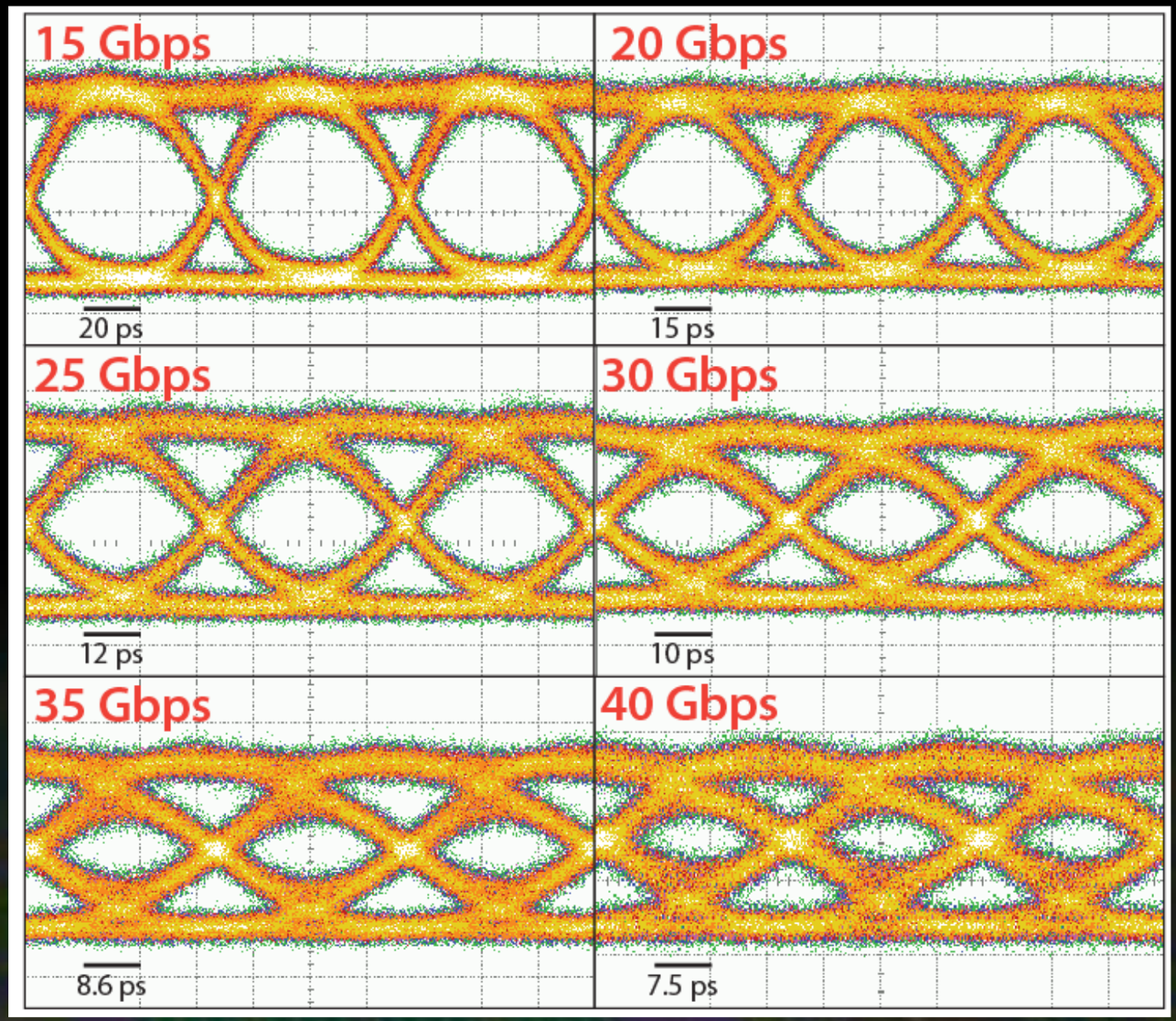
J. Rosenberg et al, PDP CLEO 2011, May 2011

Silicon ring modulator



Die photo

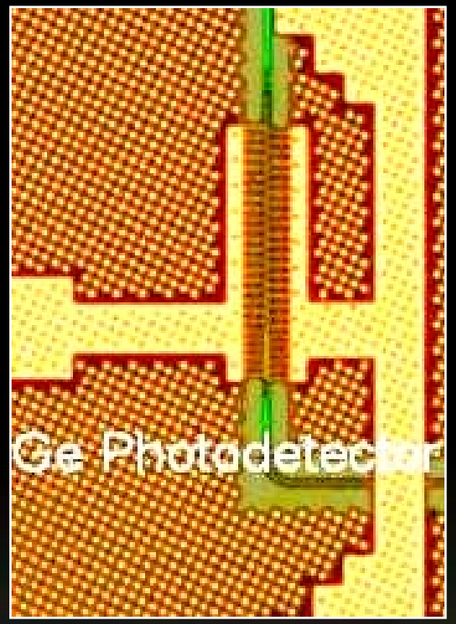
- ✓Insertion loss 1dB
- ✓Extinction ratio 3-4dB
- ✓130fF; 10 Ω
- ✓CMOS compatible voltages
- ✓Consumes 84fJ/bit at 25Gb/s



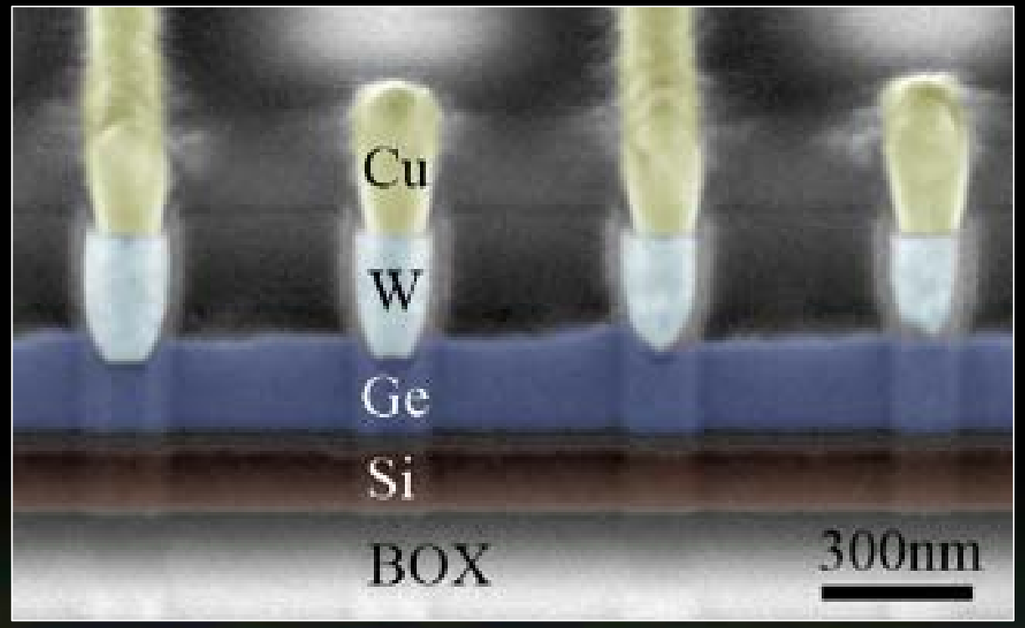
J. Rosenberg et al, PDP CLEO 2011, May 2011

Ge waveguide photodetector

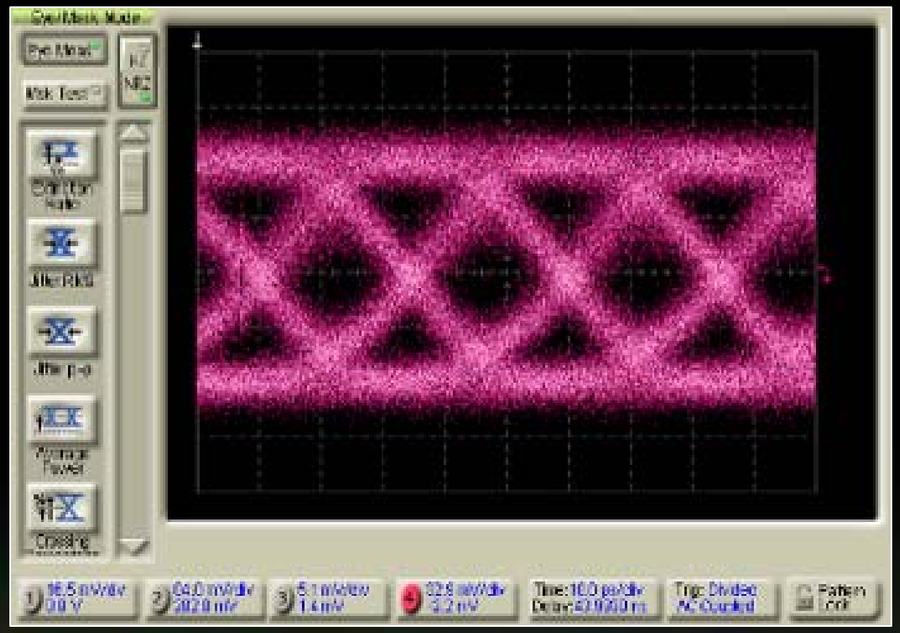
Die photo



Design



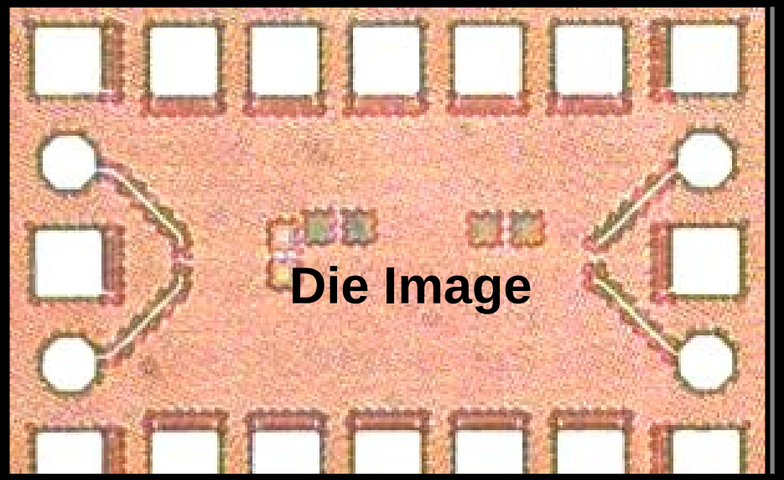
Performance

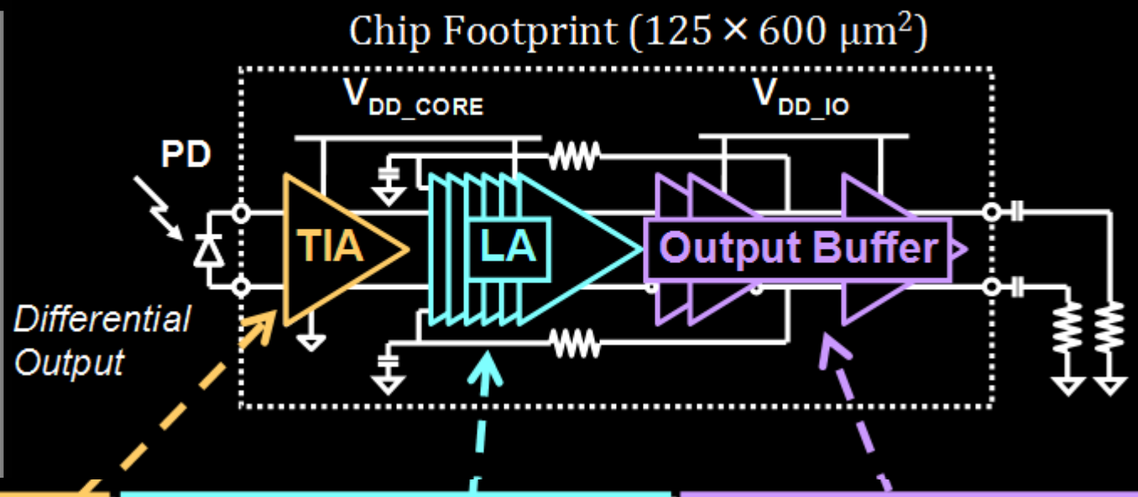


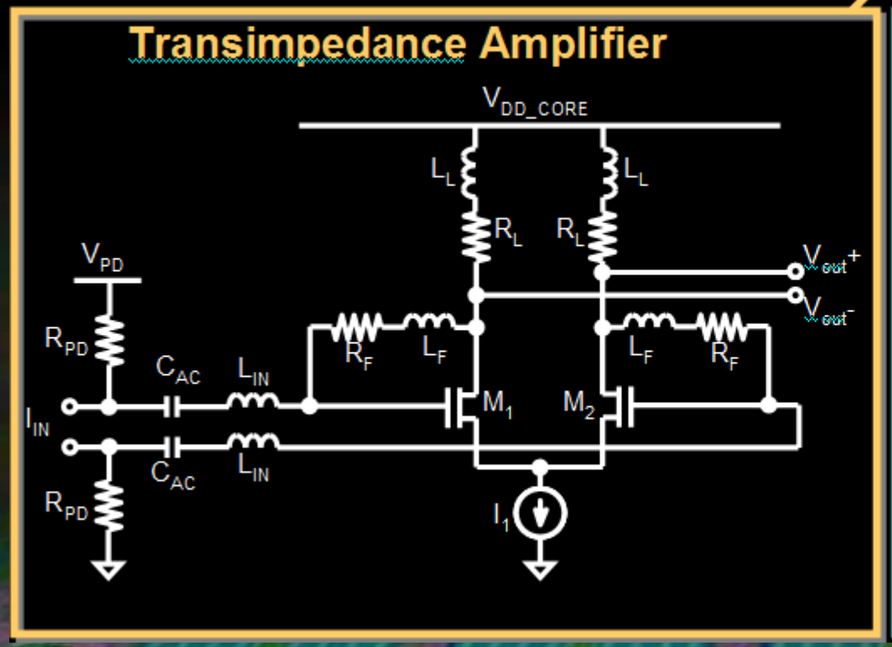
- ✓ Ge detector integrated with CMOS Circuitry
- ✓ 20um long
- ✓ 40GHz bandwidth with CMOS bias voltages
- ✓ 0.5A/W responsivity at 1.3um and 1.5um

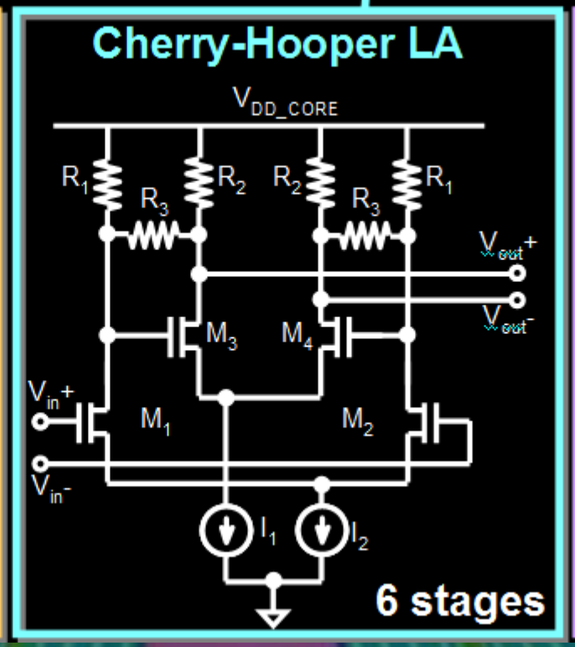
S.Assefa et al, Nature, March 2010
S.Assefa et al, OE, April 2010
S.Assefa e al , JSTQE, September 2010

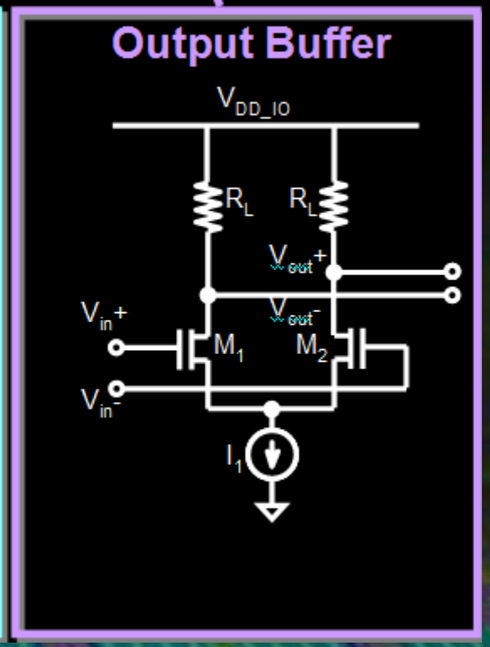
IBM Bulk 90-nm CMOS Receiver Analog IC





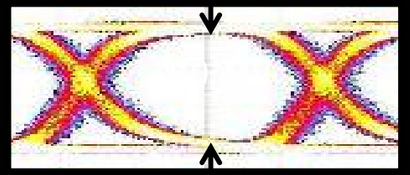
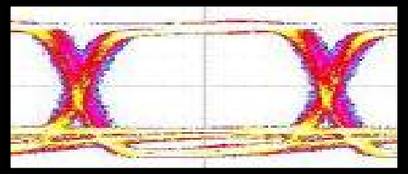
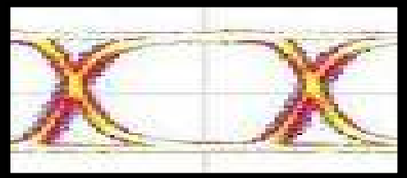
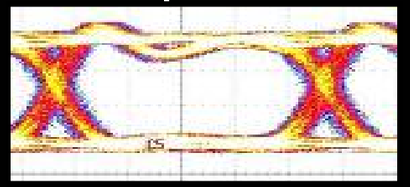
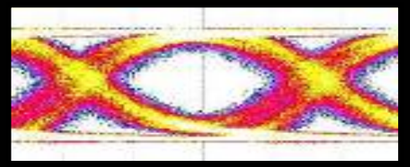
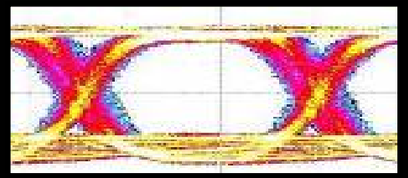
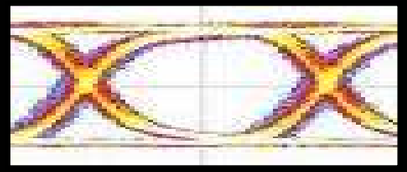
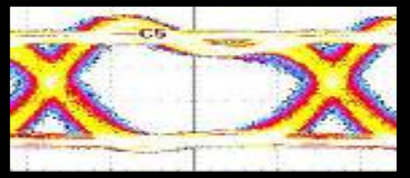
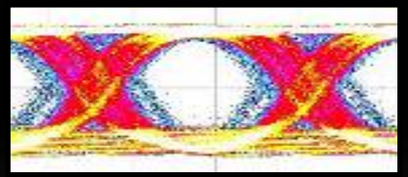
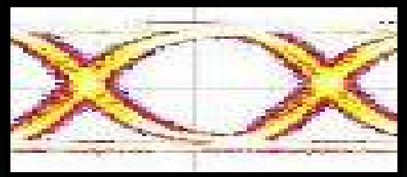
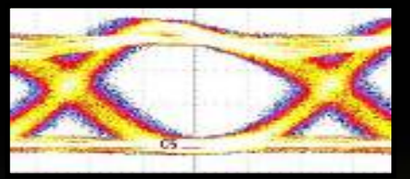
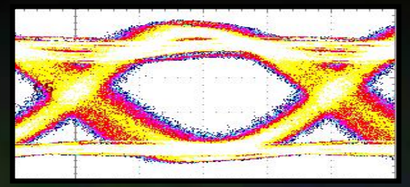
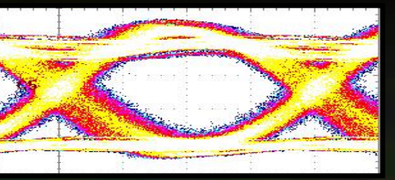
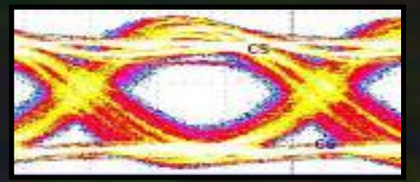






CMOS designs by A. Rylyakov and C. Schow

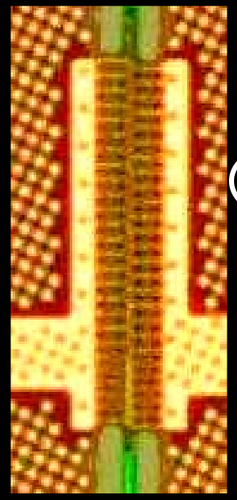
Progress 2010-2011

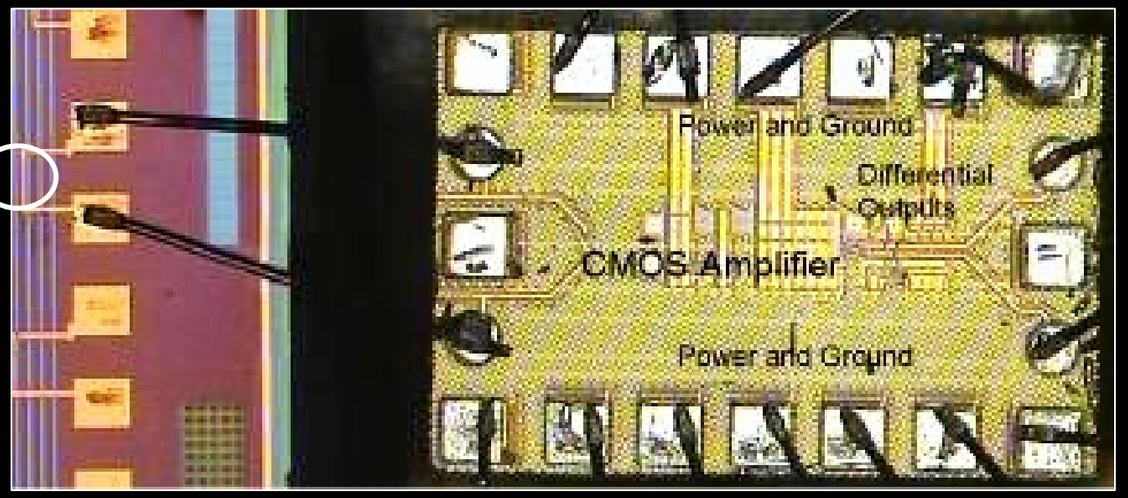
	Oct. 2010	Jan 2011	Mar 2011	Sep 2011	Oct 2011
10 Gb/s					
15 Gb/s					
20 Gb/s	15Gbps 4.7pJ/bit -8dBm				
	Assefa et al OFC 2011				
25 Gb/s		20Gbps 6.9 pJ/bit -7.1dBm	20Gbps 5.4 pJ/bit -12dBm		
		Assefa et al OFC 2011 PDP			
28 Gb/s			Assefa et al CLEO 2011	25Gbps 4.84 pJ/bit -10.2dBm	
				H.Pan et al OFC 2012	28Gbps 4.6 pJ/bit -9dBm

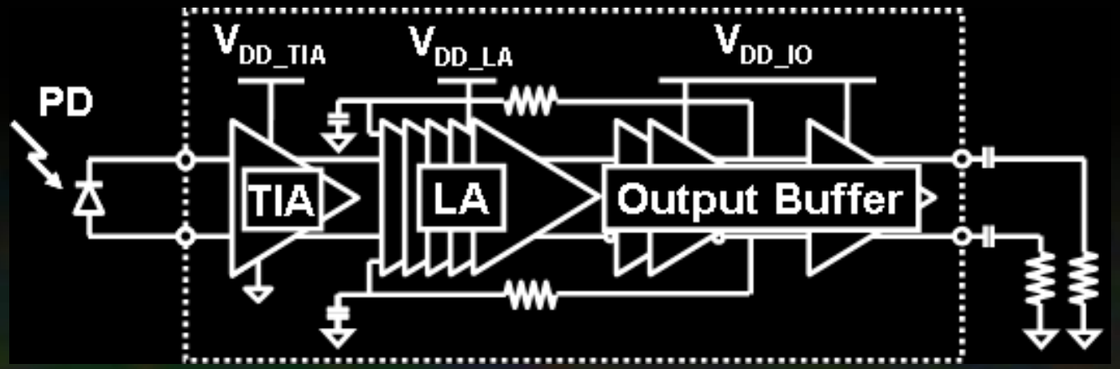
300 mVpp differential output

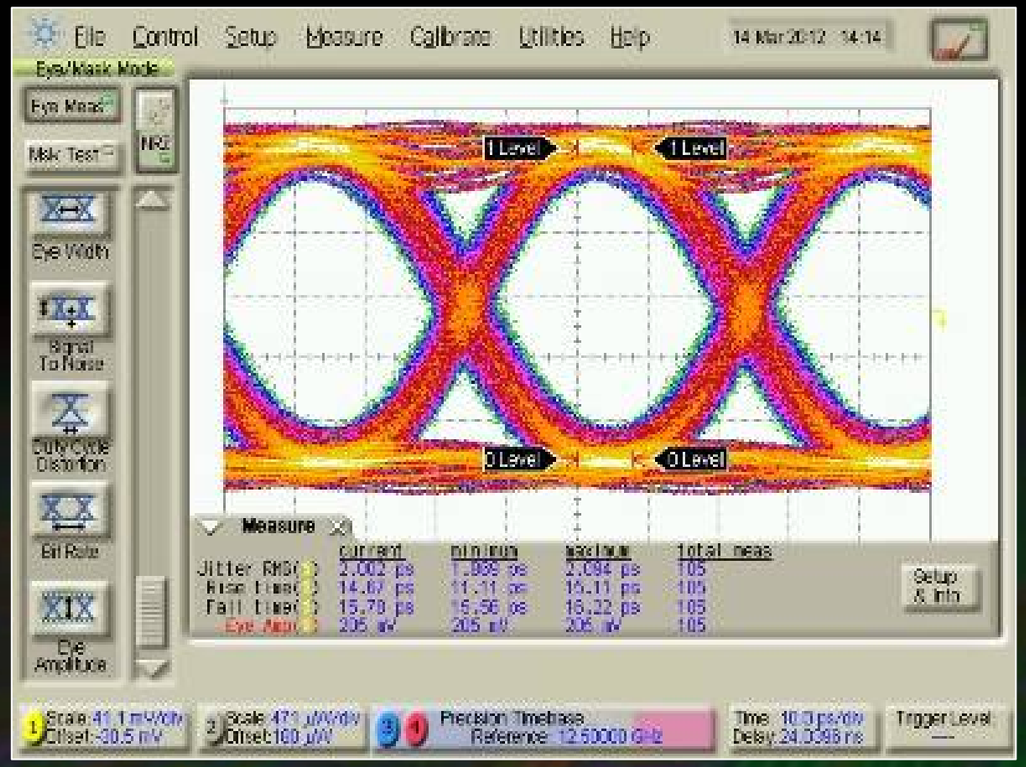
Receiver

- CMOS die 90nm
- Ge WG PD die
- wire bonded







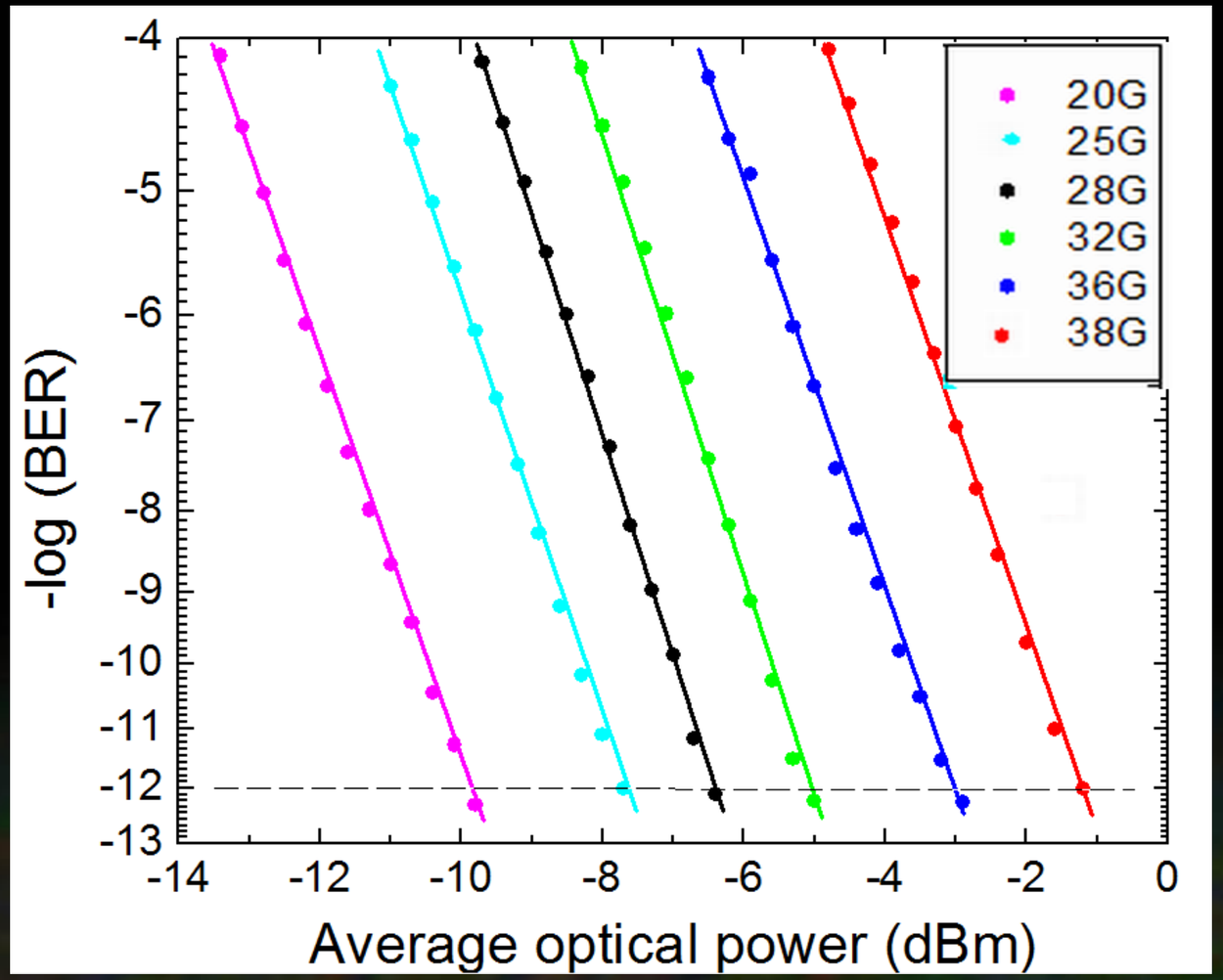


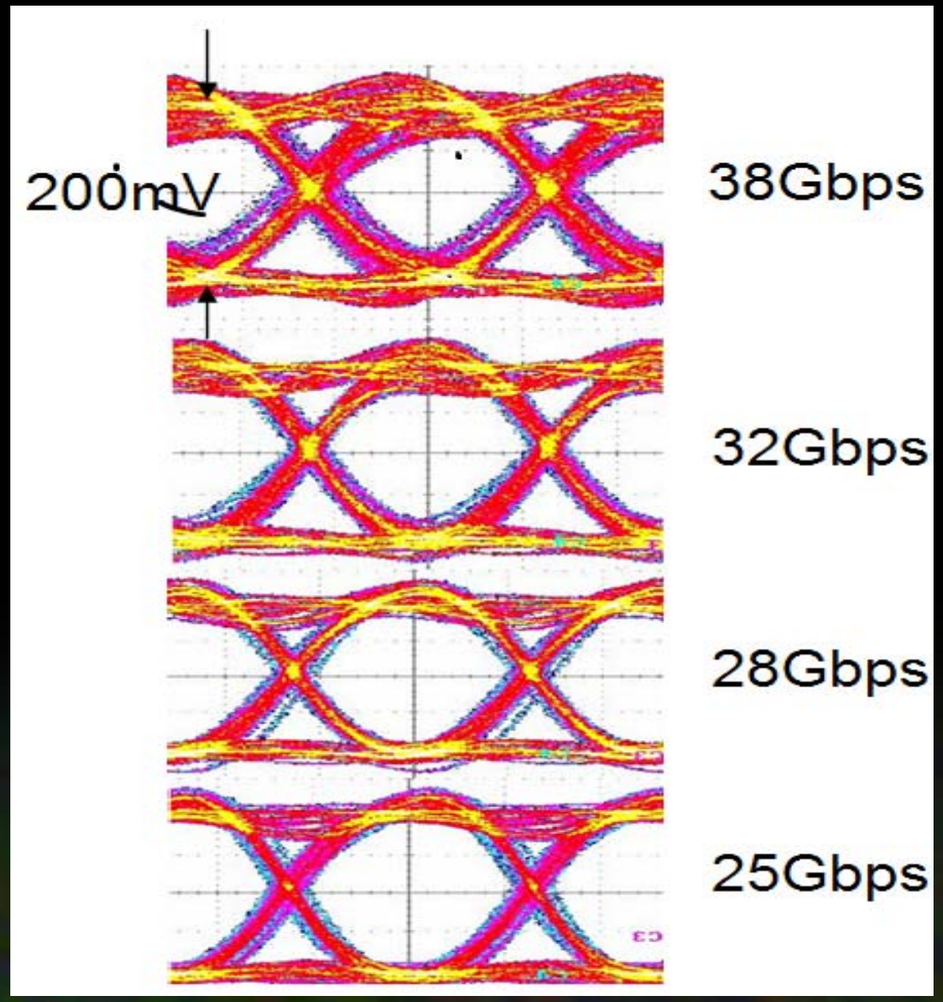
25Gbps performance

- ✓ Ge WG detector integrated with CMOS Circuitry
- ✓ 25Gbps stable operation
- ✓ Sensitivity -8.3dBm at 25Gbps

H.Pan et al, CLEO, May 2012 PDP session

Performance beyond 25G

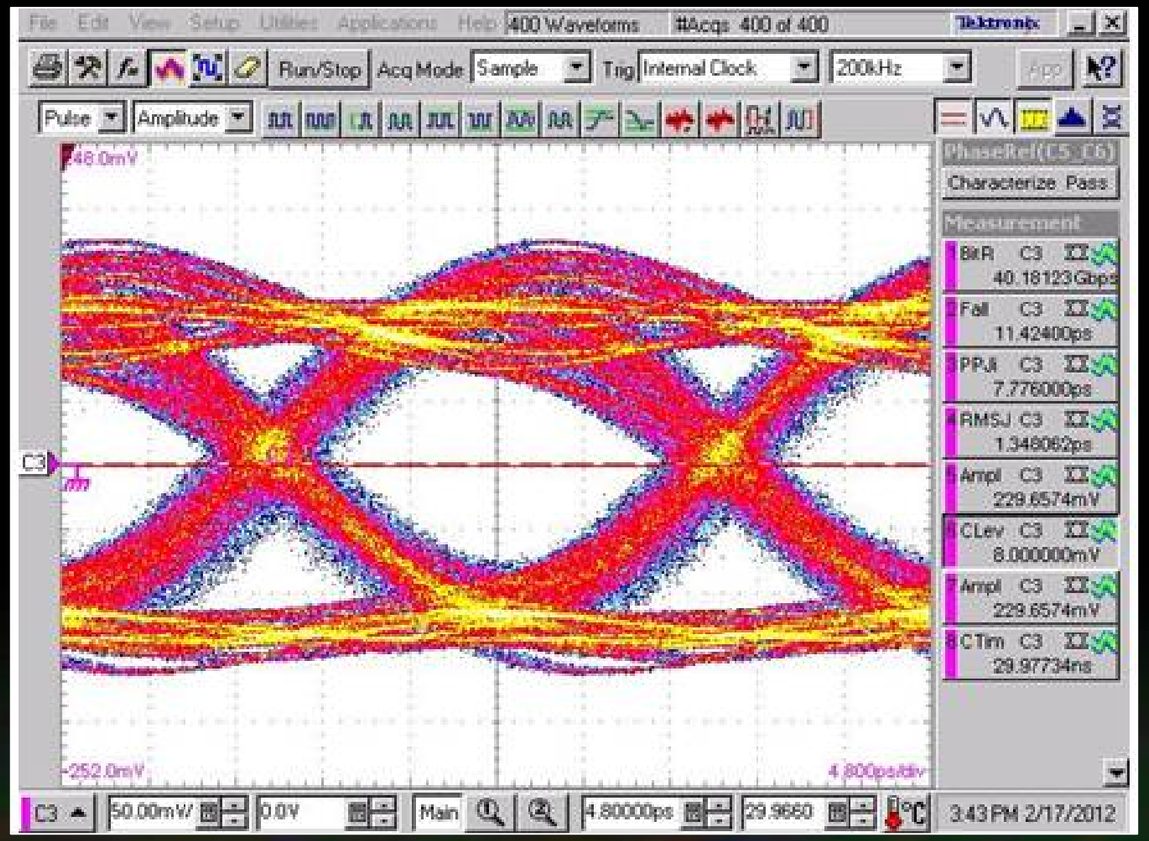


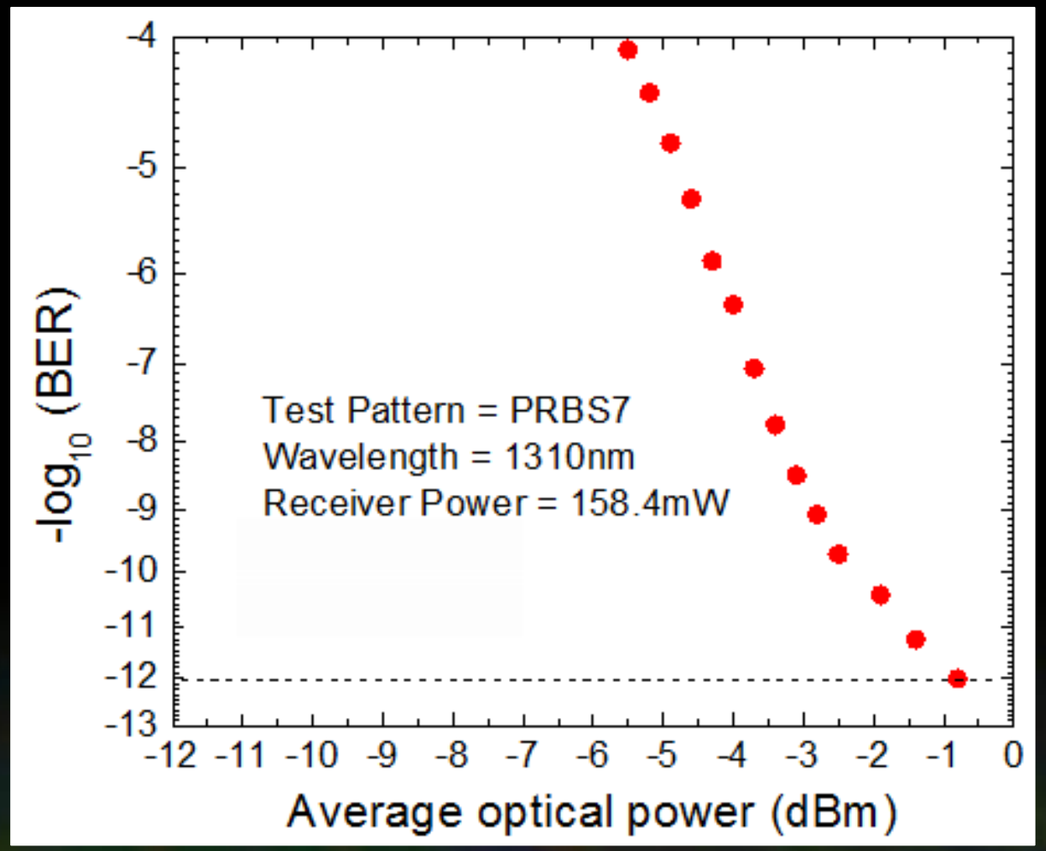


- ✓ Sensitivity -5.0 dBm at 32Gbps
- ✓ Power efficiency 1.5pJ/bit at 32Gbps

H.Pan et al, CLEO, May 2012 PDP session

Performance at 40G





✓Error-free (BER < 1e-12) up to 40Gbps

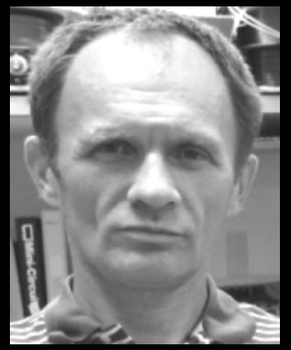
H.Pan et al, CLEO, May 2012 PDP session

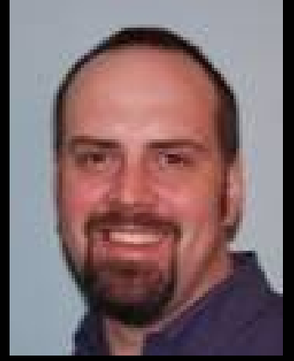
Follow the YBR

Team


Solomon Assefa


William Green


Alexander Rylyakov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