April 7, 2016

ECEN 689: Optical Interconnects

Final Project

Instructor: Sam Palermo

Project teams can consist of 1-3 students.

Project Topics

Project #1 – 10Gb/s 1km Optical Link Design

This project investigates the design of a 10Gb/s 1km optical link for a target BER=10^{-12}. A complete link budget should be constructed considering the chosen optical source, channel losses, optical channel, and receiver sensitivity. The optical source can either be a directly modulated VCSEL or an externally modulated CW laser with either a MZM, EAM, or ring resonator modulator (carrier-injection or carrier depletion). The photodetector can either be p-i-n (waveguide or discrete), APD, or OA/p-i-n. However, preference is given to a p-i-n detector. Key specs for the receiver decision element are: $1mV_{rms}$ noise, 1mV offset, and 20fF input capacitance. The driver and receiver front-end circuits should be designed at the transistor level. Note, you don't have to design the decision element. 10Gb/s eye diagrams should be produced with equivalent circuit models for the optical source and photodetectors. Show eye diagrams at both the transmitter output and the final receiver output. A key metric of the link design is the overall power efficiency (mW/Gbps). Note, for an externally-modulated system this should include the CW laser power.

Project #2 – 56Gb/s PAM4 VCSEL Transmitter

This project involves the design of a 56Gb/s PAM4 VCSEL transmitter. Non-linear equalization techniques should be implemented to compensate for the device's non-linear frequency response. A 2mW peak OMA should be achieved from the lowest to highest symbol level.

Project #3 – 5GHz Linear MZM Transmitter

This project involves the design of a highly-linear MZM transmitter for analog link applications. The driver should implement pre-distortion techniques to compensate for the inherent MZM non-linearity. These linearization techniques should provide a minimum of 10dB IMP3 improvement with the MZM is operated with a 50% modulation index.

Project #4 – Optical PLL Design for a 10Gb/s QPSK Link

This project involves the design of an optical PLL for a 10Gb/s QPSK link. This involves both the optical design of the QPSK demodulator and the electrical design of the QPSK phase detector and optical PLL loop filter. In addition to the QPSK phase detector, the optical PLL should have a frequency detector capable of a 1THz capture range.

Project #5 – High Dynamic Range Image Sensor

This project involves the design of an image sensor with 120dB dynamic range. Key specs include:

- Minimum Noise Current Integrated over 100Mhz Input Bandwidth = 100pA
- Dynamic Range of the Sensor= 120dB
- Maximum PD Current= 0.1mA
- Maximum Integration time for the PD current= 500us.
- Photodiode Responsivity = 0.4-0.5 A/W

Project #6 – 60Gb/s PAM4 DFE Receiver

This project involves the design of a 60Gb/s PAM4 DFE receiver for backplane signaling applications. The receiver should provide sufficient equalization to compensate for 20dB loss at the PAM4 Nyquist frequency. Adaptive equalization techniques should be implemented to set all the equalization taps.

Project #7 – Topic of Your Choice

I welcome any project suggestions related to optical interconnects circuits and systems.

Important Dates

- April 12 Inform Prof. Palermo of project choice
- April 19 Preliminary Report #1. This will be HW4.
- May 3 Final Report Due
- May 10 Project Presentation Due

The report must include a summary of the key specifications and background literature survey, with adequate references. A complete discussion of the architecture, with comments on the robustness should be included. There should be adequate simulations to justify the performance and a comparison with the current state-of-the-art. Project grading will be a function of the creativity and elegance of the design, completeness of the analysis, and the clarity of the report and presentation.