Computational Lithography

for Silicon Photonics Design

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Abstract

A lithography model is built using physical measurements obtained from a fabricated test pattern. The method is able to accurately predict the proximity and smoothing effects characteristic of a 193 nm deep-ultraviolet (DUV) lithography process.

The accuracy of the model is verified by visually inspecting the fabricated test patterns and comparing them to the predictions of the lithography model. Furthermore, using a benchmark device (the contra-directional coupler), the prediction accuracy of the optical response is compared against experimental measurements. The comparisons showed the predictions had good agreement with the fabricated devices.

Subsequently, an application of the lithography model is demonstrated. Design correction methods enabled by the lithography model are performed on the contra-directional coupler. The new designs were fabricated using electron-beam lithography and their experimental measurements confirmed an improved optical performance.

Lay Summary

Deep-ultraviolet lithography (DUV) is a method of fabrication for silicon photonic devices with the ability to perform large volume fabrications. However, the DUV process produces fabrication errors known as lithography effects.

In this thesis, a model able to predict the lithography effects of a DUV process is built. The model can generate a prediction of the lithography effects from any device layout. The predictions of the model demonstrated good accuracy when verified using scanning electron microscope images and experiment data.

Enabled by the lithography model, first-time-right design methods are demonstrated. These methods provide information useful for device prototyping on the DUV process without performing a DUV fabrication. Furthermore, the emulation of the DUV process using a low-cost electron beam lithography (EBL) process was demonstrated.

Lastly, using the first-time-right design methods, a revised photonic device was fabricated using EBL which produced an improvement in optical performance.

Preface

The contents in Chapter 3 of this thesis are based on the following publication of which I am the primary author:

> S. Lin, M. Hammood, H. Yun, E. Luan, N. A. F. Jaeger and L. Chrostowski, "Computational Lithography for Silicon Photonics Design," in IEEE Journal of Selected Topics in Quantum Electronics. doi: 10.1109/JSTQE.2019.2958931

I was the lead investigator responsible for concept formation, data collection and analysis, layout design, building the lithography model, and manuscript composition. H. Yun, M. Hammood, and E. Luan were involved in early stages of concept formation, layout design, and contributed to manuscript edits. N. A. F. Jaeger was involved in manuscript edits. L. Chrostowski was the supervisory author on this project and was involved throughout the project in concept formation and manuscript edits.

The schematics and scanning electron microscopy images of sub-wavelength devices presented in Chapter 1 of this thesis are designs developed by Han Yun and Enxiao Luan of the Microsystem and Nanotechonology Group at the Department of Electrical and Computer Engineering of the University of British Columbia.

The scanning electron microscopy images presented in Chapters 1, 2, 3, 4 and 5 were taken by Dr. Gethin Owen from the Centre for High-Throughput Phenogenomics at the Faculty of Dentistry at the University of British Columbia.

The test pattern set used to develop the lithography model in Chapter 3 is provided by the Mentor Graphics Calibre Workbench Software.

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List of Abbreviations

ArF Argon Fluoride. 2, 14

CD Critical Dimension. xi, xii, xvi, 24, 27–32, 34, 57, 60

CMOS Complementary Metal-Oxide-Semiconductor. 1, 13–15

contra-DC Contra-directional Coupler. viii, ix, xi–xvi, 2, 3, 6–11, 17, 18, 20–23, 31–33, 35–37, 39–42, 45–47, 52, 56–58

DUV Deep-Ultraviolet. x, xii–xv, 1, 13–21, 24, 29, 37, 41–47, 53, 56, 57, 59, 60

EBL Electron Beam Lithography. xiii–xv, 1, 13, 14, 41–46, 52

EMU Emulation of Deep-Ultraviolet Lithography. xiii–xv, 42–45, 50, 53

FDTD Finite-Difference-Time-Domain. x, xv, 6, 10, 11, 20, 21, 33, 46, 47, 55, 56, 61

KrF Krypton Fluoride. 14

OPC Optical Proximity Correction. 1

SEM Scanning Electron Microscopy. x, xi, xiii, xiv, xvi, 2, 17–20, 22, 24, 25, 28, 29, 31, 32, 42, 43, 45, 56–60

SOI Silicon-on-Insulator. 1, 6, 13, 14

SR Self-Reflection. viii, xii, 32, 33, 38, 40

SWG Sub-wavelength Grating. x, 17–19

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To all the hardworking and brilliant people of science,
I hope the results showcased in this thesis contributes in your endless
pursuit of improving technology and human knowledge.

Chapter 1

Introduction

In recent years, silicon-on-insulator (SOI) platforms have increased in popularity. Many key devices, such as, filters [1], modulators [2], and photodetectors [3] have been demonstrated on such platforms [4][5]. SOI platforms have two common choices for patterning the silicon: electron-beam lithography (EBL) and deep-ultraviolet (DUV) lithography. EBL is performed by writing the design directly onto the resist via an electron beam. This maskless fabrication approach can achieve smaller feature sizes with fast turnaround times, at the cost of low throughput. This makes EBL attractive for rapid-prototyping research and development purposes [6]. Conversely, DUV lithography performs the design patterning using a binary mask. The mask exposes the resist via a laser within a projection system (such as full-wafer projection, full-wafer scanning, step-and-repeat also known as a stepper, and step-and-scan also known as a scanner) which prints a copy of the design onto the wafer[7]. As a result, the DUV process has high throughput and is more suitable for mass production.

SOI device performance suffers from discrepancies between as-designed and as-fabricated structures. Photolithographic effects, such as smoothing [8] and proximity effects [9], are large contributing factors to these discrepancies. Previous efforts have been made to correct for photolithography effects. These include optical proximity correction (OPC) [10][11][12][13][14] and using phase shifted masks [15][7]. However, the SOI platform does not yet have a "first-time-right" design approach akin to that of the CMOS platform [16].

As silicon photonics marches towards commercialization, it is crucial that it brings with it the robustness in fabrication that exists in mature CMOS processes [4]. Previous work demonstrated that photolithography smoothing effects of 2-port Bragg grating devices could be modelled by fitting the modelled responses to experimental responses [8][17]. However, designers would ideally wish to understand and model the effects of photolithography prior to fabrication.

In this work, we use a computational lithography model to predict the outcomes of a commercial dry 193 nm DUV lithography fabrication process,

that uses an ArF laser stepper and a binary mask. The predictive model is built using measurement data obtained from fabricated test patterns and simulates the photolithography effects on an input shape. Our model is process specific and allows designers to predict their device's performance for a particular fabrication process. To verify the accuracy of the model, we use the optical response of a 4-port, Bragg-grating-based filter, known as a contra-directional coupler (contra-DC) [18], as a benchmark. The configuration of the contra-DC consists of two Bragg gratings placed in close proximity to each other for coupling purposes. We use the contra-DC as a benchmark because it is particularly susceptible to photolithography effects, such as smoothing and proximity effects. The device is susceptible to smoothing because it uses sidewall-corrugated, Bragg-grating waveguides and is susceptible to proximity effects because the two waveguides are in close proximity to each other. As the contra-DC has two output ports, and an optical response sensitive to design parameters, it is an excellent candidate for the validation of our model. We are able to demonstrate excellent visual resemblance between the output of our computational lithography model and the Scanning Electron Microscopy (SEM) images of a fabricated test pattern set. Furthermore, we are able to accurately reproduce the experimental measurements made on our benchmark device by simulating the response of the predicted device structure generated by our model.

1.1 Periodic Devices

This section explains the fundamental theory of grating-based devices using a 2-port Bragg grating filter. The focus is then shifted to a specific grating-based filter, the 4-port contra-directional coupler (contra-DC). As the remainder of the thesis emphasizes the comparison of the bandwidth, we will present the theories of the bandwidth relationship. It is especially important for readers to appreciate/understand how sensitive the device performance is due to fabrication variations.

The contra-DC is a 4-port grating-based filter device. The device consists of two grating-based waveguides placed in close proximity for coupling purposes. During fabrication, lithography smoothing and proximity effects occur on the device. The gratings are subject to smoothing due to their shape (square) and small dimensions (typically $\leq$100 nm). The gaps between the two waveguides are minimized (typically around 100 nm) to obtain the highest possible coupling strength. The gap size approaches fabrication limits and inevitably induces proximity effects. Minute variations to these

parameters incur large changes to the device performance such as bandwidth reductions and central wavelength shifts. This makes the contra-DC an ideal benchmark device to evaluate the accuracy/validity of the lithography model as we can compare the experimentally measured response against the predicted response.

1.1.1 Bragg Grating Filters

The Bragg grating structure is a photonic device that utilizes periodic modulation to create a filter response. The device is simple in structure and does not require special fabrication steps for realization. The Bragg grating has periodic effective refractive index variations along its direction of propagation. The variations of the index induce reflections at each boundary where the index changes. The reflected signals interfere constructively near a select range of wavelengths which is determined by the pitch (Λ) parameter of the design and the effective refractive index (n_{eff}). This select wavelength is known as the Bragg wavelength and is determined by the Bragg condition shown in equation 1.1.

$$\lambda_B = 2\Lambda n_{eff} \tag{1.1}$$

Outside of the Bragg wavelength, the reflected signals will instead interfere destructively, thus creating a filter response. Fig. 1.1 shows a typical Bragg filter response.

Fundamentally, the gratings function to couple the forward and backward modes. Using coupled-mode theory [19] the electric field can be described as a summation of the forward-propagating wave (R) and the backward-propagating wave (S) as shown in equation 1.2 [19]. β_0 is the Bragg propagation constant shown in equation 1.3

$$E(z) = R(z)exp(-j\beta_0 z) + S(z)exp(j\beta_0 z) \tag{1.2}$$

$$\beta_0 = \frac{2\pi}{\lambda_B} n_{eff} \tag{1.3}$$

Using the derivations shown in [19], the coupled mode equations 1.4 and 1.5 can be obtained. k is the coupling coefficient describing the coupling amount per unit length.

$$\frac{dR}{dz} + j\Delta\beta R = -jkS \tag{1.4}$$

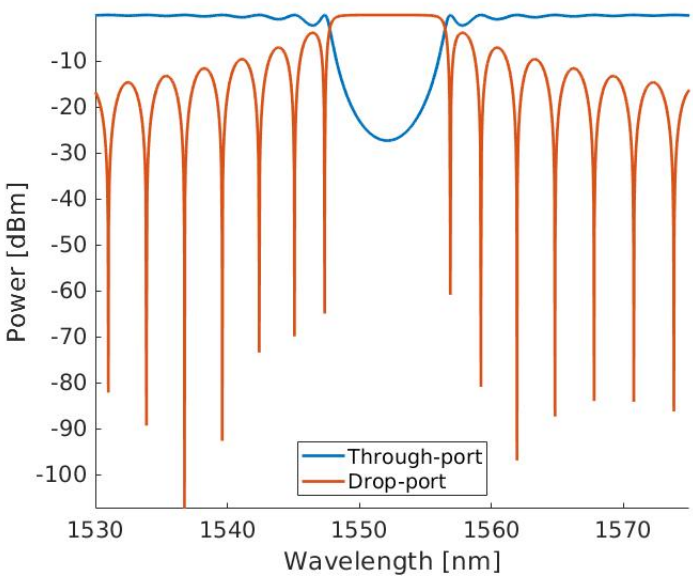


Figure 1.1: An example Bragg response is depicted. The bandwidth is depicted centered around a wavelength of 1550 nm. The reflection response shows null peaks useful for determining the bandwidth.

$$\frac{dS}{dz} - j\Delta\beta S = jkR \tag{1.5}$$

For step-wise effective index variation gratings (square gratings), the reflection at each index interface can be written as $\frac{\Delta n}{2n_{eff}}$ using Fresnel's equations where the numberator $\Delta n = n_{eff1} - n_{eff2}$ and the denominator n_{eff} is the effective index average of the two variations.

The coupling occurs at each grating period which is the pitch (Λ) parameter of the device. Each period will create two reflections which we include when writing the relationship of the coupling coefficient in equation 1.6. The coupling coefficient can be further simplified using the Bragg condition (equation 1.1) to obtain equation 1.7 [19].

$$\kappa = 2\frac{\Delta n}{2n_{eff}}\frac{1}{\Lambda} \tag{1.6}$$

$$\kappa = 2\frac{\Delta n}{2n_{eff}}\frac{2n_{eff}}{\lambda_B} = \frac{2\Delta n}{\lambda_B} \tag{1.7}$$

From the solutions of the coupled mode equation [19], we can obtain the reflection coefficient relationship shown in equation 1.8 for a uniform grating with a length L [19].

$$r = \frac{-i\kappa sinh(\gamma L)}{\gamma cosh(\gamma L) + i\Delta\beta sinh(\gamma L)} \tag{1.8}$$

where $\gamma^2 = \kappa^2 - \Delta\beta^2$ and $\Delta\beta$ has the relationship shown in equation 1.9 [19].

$$\Delta\beta = \beta - \beta_0 = \frac{2\pi n_{eff}(\lambda)}{\lambda} - \frac{2\pi n_{eff}(\lambda_B)}{\lambda_B} \approx -\frac{2\pi n_g}{\lambda_B^2}\Delta\lambda \tag{1.9}$$

The group index n_g and wavelength relation [4] being:

$$n_g = n_{eff} - \lambda\frac{dn_{eff}}{d\lambda} \tag{1.10}$$

When $\Delta\beta = 0$ the reflection of the Bragg grating is at its maximum, this simplifies the reflection equation down to equation 1.11 and 1.12 for field and power respectively [19].

$$r = -itanh(\kappa L) \tag{1.11}$$

$$R_{max} = tanh^2(\kappa L) \tag{1.12}$$

Aside from the power, we are also interested in the bandwidth of the device. We define the bandwidth in this case to be between the first nulls around the target wavelength's reflection peak. Using equation 1.11 and our relation for γ, we can write an equation for the condition at which the reflectivity in the system is equal to zero (equation 1.13).

$$-\gamma^2 = \Delta\beta^2 - \kappa^2 = \left(\frac{M\pi}{L}\right)^2 \qquad M = 1, 2, 3, .. \tag{1.13}$$

Now, by taking the first order ($M = 1$) of equation 1.13 which corresponds to the two null peaks next to the Bragg wavelength and rearranging, the expression shown in equation 1.14 for the bandwidth can be obtained [20][21].

$$\Delta\lambda = \frac{\lambda_B^2}{\pi n_g}\sqrt{\kappa^2 + \left(\frac{\pi}{L}\right)^2} \tag{1.14}$$

As a final note, the gratings described in this chapter are considered to be lossless. To include the loss in the equations $\Delta\beta$ can be instead substituted with $\Delta\beta - j\alpha_f$ where α_f is the loss coefficient for the field.

1.1.2 Contra-directional Couplers

The contra-DCs in this thesis are designed in the following steps:

1. Match Bragg condition - determine the period (Λ)
2. Evaluate coupling strength - determine the corrugation widths (ΔW)
3. Calculate using equations - rough estimates for the bandwidths
4. Simulate using FDTD bandstructure - fine estimates for bandwidths

Building on the Bragg reflectors discussed in the previous section, K. Ikeda, et. al [18] showed on the SOI platform that two reflectors can be placed in coupling proximity to create a four-port device in which the reflection spectrum can be read from the drop port. Ikeda referred to this device as a wavelength selective coupler with vertical gratings. In recent years, it has become commonly known as the contra-directional coupler (contra-DC) first proposed by Yariv [22].

As the name implies, the contra-DC operates in the contra (opposite) direction of the input flow. The device functionally solves many of the nuisances of a standard SOI Bragg reflector which will first be briefly discussed: In application, the reflections from the Bragg reflector prove challenging to read and measure, requiring either an isolator/circulator [23] or costly measurement apparatus. A potential solution involving using an integrated circulator is possible [24], but there is a substantial trade-off in device footprint.

In contrast, the contra-DC provides an on-chip integrated solution that separates the input, transmission, and reflection ports, removing the need of isolators or circulators [25][26]. Furthermore, the contra-DC has 4-ports, creating potential for multiplexing and demultiplexing applications [27].

To design a contra-DC, we first have to meet three Bragg conditions, shown in equations 1.15, 1.16, and 1.17.

$$2\beta_1 = \frac{2\pi}{\Lambda} \tag{1.15}$$

$$2\beta_2 = \frac{2\pi}{\Lambda} \tag{1.16}$$

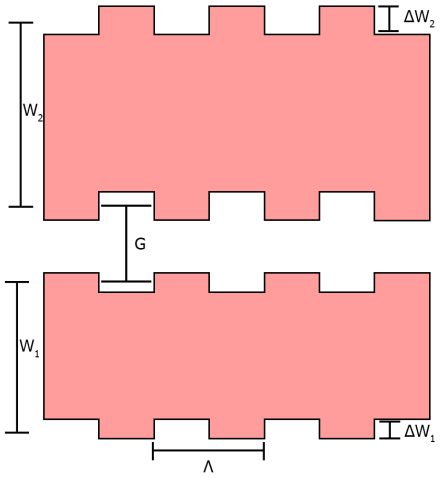


Figure 1.2: A diagram of the contra-DC device with the parameters labeled.

$$\beta_1 + \beta_2 = \frac{2\pi}{\Lambda} \tag{1.17}$$

where β is the propagation constant and Λ is the pitch of one unit cell of the grating. The subscripts on β refer to waveguide 1 or 2 of the contra-DC system. Equation 1.17 can be interpreted as the average of equation 1.15 and equation 1.16. Hence, the average propagation should be chosen in relationship to our target wavelength. As the propagation β relates directly to the refractive index n, and thus the waveguide's width (W_1 , W_2), we are able to narrow down potential width parameters for our contra-DC. Figure 1.2 shows a diagram depicting the contra-DC paramters. Figure 1.3 shows an example of the phase-match condition for a contra-DC with $W_1 = 560$ nm, $W_2 = 440$ nm, Gap=220 nm, $\Lambda = 318$ nm, ΔW_1=50 nm, and ΔW_2=30 nm. The corresponding simulated response of this device is shown in Figure 1.4 using the SiEPIC Photonics Package [28]. Note that only the lower self-reflection is shown. This is because the input is set to W_2. If the input in W_1 the self-reflection at the higher wavelength will show instead.

With the phase match condition satisfied, the next parameter of interest is the gap and corrugations of the contra-DC. These two parameters directly correspond to the coupling strength of the device. There are three coupling coefficients that are of interest [26]: the backward coupling of waveguide 1 (equation 1.18), the backward coupling of waveguide 2 (equation 1.19), and

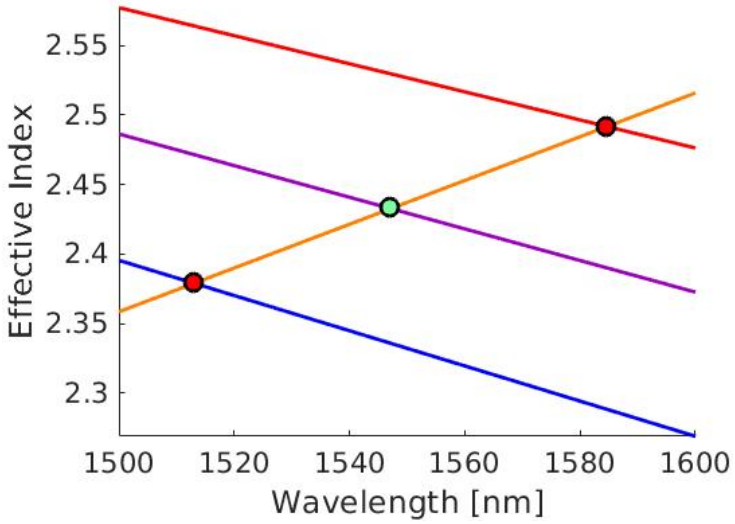


Figure 1.3: The phase match condition for a contra-DC with parameters of W_1=560 nm, W_2=440 nm, Gap=220 nm, Λ = 318 nm, ΔW_1=50 nm, and ΔW_2=30 nm is shown. W_1's effective index is plotted in red, W_2's effective index is plotted in blue. The average effective index of the two waveguides is plotted in purple. The phase match condition is plotted in orange. The center wavelength (at λ=1550 nm of the main bandwidth is marked with a green dot. The locations of the self-reflection bandwidths (λ=1510 and 1585 nm) are marked with red dots.

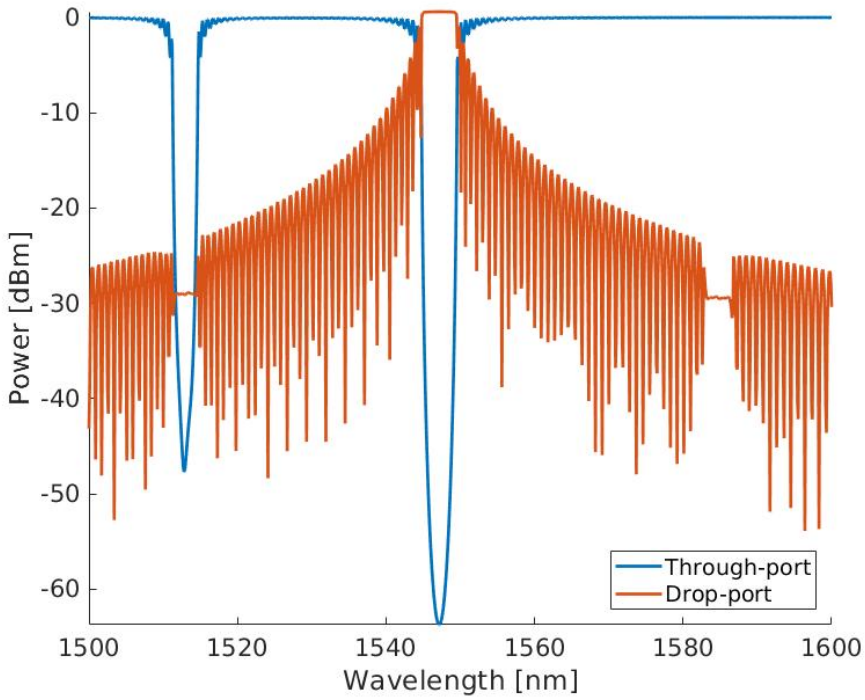


Figure 1.4: The couple mode theory-transfer matrix method simulation response for a contra-DC of $W_{1,2}$=560, 400 nm, Gap=220 nm, Λ=318 nm, and $\Delta W_{1,2}$=50, 30 nm. The through-port is shown in blue and the drop-port is shown in orange. The main band can be seen centered at λ=1550 nm and the lower self-reflection can be seen centered around λ=1510 nm. Note that only the self-reflection of the input waveguide will be visible from the through-port. The plot was generated using the SiEPIC Photonics Package.

the contra-cross coupling between waveguide 1 and waveguide 2 (equation 1.20).

$$\kappa_1 = \frac{\varepsilon_0 \omega}{4} \langle E_1 | \Delta n_g^2 | E_1 \rangle \tag{1.18}$$

$$\kappa_2 = \frac{\varepsilon_0 \omega}{4} \langle E_2 | \Delta n_g^2 | E_2 \rangle \tag{1.19}$$

$$\kappa_c = \frac{\varepsilon_0 \omega}{4} \langle E_1 | \Delta n_g^2 | E_2 \rangle \tag{1.20}$$

Here, ε_0 is the vacuum permittivity, ω is the angular frequency of light, and E_1, E_2 are the field distributions of waveguide 1 and 2 respectively.

$$\Delta n_g^2 = \begin{cases} -(n_{core}^2 - n_{clad}^2)\frac{f(z)+1}{2}, & \text{In silicon region} \\ 0, & \text{In oxide region} \end{cases} \tag{1.21}$$

For Equation 1.21, Δn_g^2 is the index perturbation. In the grating region, the perturbation is related to the index of the core and the index of the cladding. The period function $f(z)$ here describes the geometry of the grating (relating to the pitch Λ). Furthermore, equation 1.21 reveals that larger corrugations (larger Δn_g^2) will increase the coupling strength of our contra-DC.

Using the equation 1.22, the rough estimates of the bandwidth can be obtained [18]. Here, κ is the backward coupling coefficient. $\kappa_{1,2}$ is each waveguide's local backward coupling (this is also known as the self-reflection bandwidth). κ_c is the coupling of the main bandwidth centered at the target wavelength. κ can also be used with the couple mode theory-transfer matrix method [26] to simulate the spectrum response of the device.

$$\Delta\lambda_i = \frac{\lambda^2 |\kappa_i|}{\pi n_{eff}} \qquad L_i = \frac{1}{|\kappa_i|} \qquad i = 1, 2, c \tag{1.22}$$

Subsequently, using the device parameters to create a 3D polygon, a fine estimate of the bandwidth can be obtain via the Finite-Difference-Time-Domain (FDTD) bandstructure method. The bandstructure method operates by assuming an infinitely long periodic grating. Only one unit cell of the grating is required to be simulated [29]. The FDTD Bloch boundary conditions are applied along the propagation direction. The Fourier transforms of the time domain signals can then be used to estimate the bandwidth ($\Delta\lambda$) and center wavelength (λ_0). Furthermore, The coupling value κ can be extracted from the bandstructure and used in equation 1.22 or in the

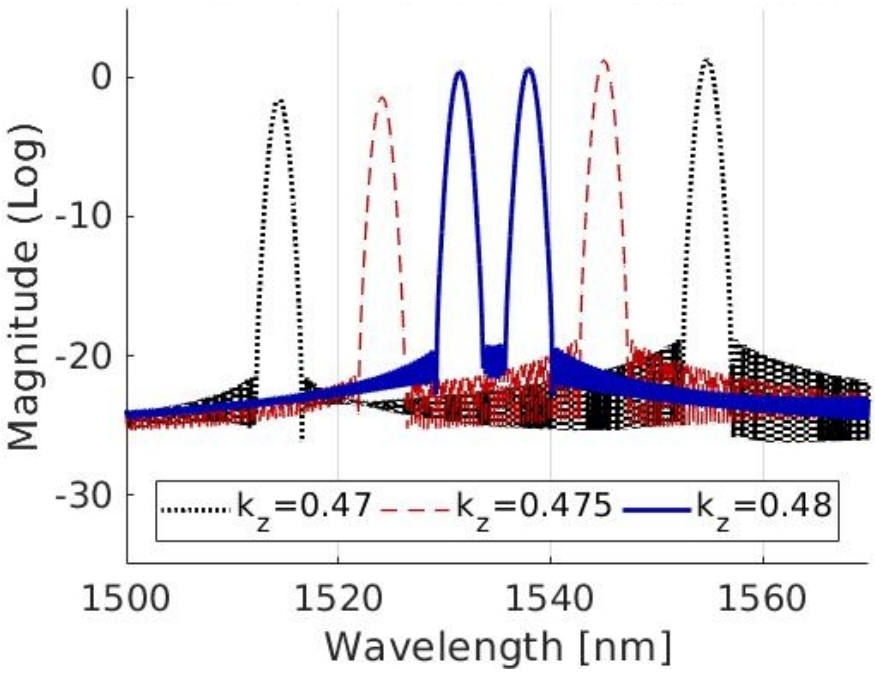


Figure 1.5: The magnitude of the Fourier Transforms of the time domain signal at various k_z values are depicted. The two peaks for each transform can be used to obtain the bandwidth and center wavelength. The peaks can also be plotted to obtain the bandstructure diagram shown in Figure 1.6.

couple mode theory-transfer matrix method [26][28] to produce a response plot.

Figure 1.5 shows an example of the magnitude of the Fourier transforms of the time domain signals from a FDTD simulation of a contra-DC. Figure 1.6 shows a plot of the wave vector k_z versus the wavelength. k_z is a unitless wavevector (normalized by length to the period of the contra-DC). The peaks of Figure 1.5 correspond to the data points highlighted in Figure 1.6. The most narrow section of the bandstructure, highlighted in Figure 1.6 at $k_z = 0.48$, corresponds to the devices main bandwidth, i.e. contra-directional coupling bandwidth, and center wavelength. Furthermore, the self-reflection bandwidths and their center wavelengths can be seen at $k_z = 0.5$. The reflection of the narrow waveguide is at the lower wavelength and the reflection of the wide waveguide is at the higher wavelength.

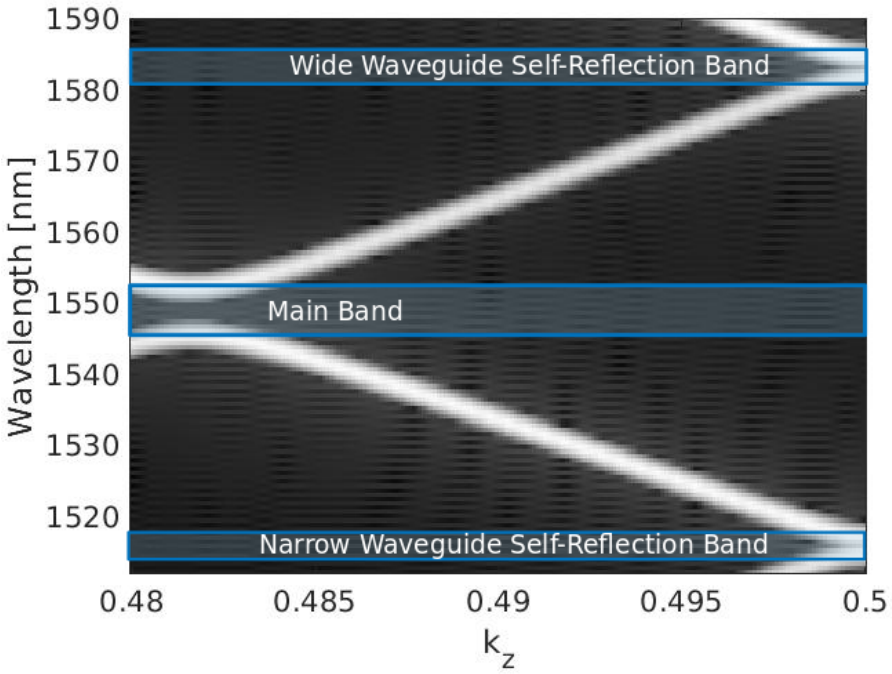


Figure 1.6: The bandstructure plot obtained from a sweep of k_z is depicted. The main band is around k_z=0.48 while the self-reflection band can be seen at k_z=0.5.

1.2 Fabrication

For designers of the silicon-on-insulator (SOI) platform the fabrication process is often the limiting factor between academic proof-of-concept devices and large scale commercialization.

There are two choices available for SOI fabrication: electron beam lithography (EBL), and a state-of-the-art optical lithography known as deep-ultraviolet lithography (DUV). The DUV process is derived from CMOS fabrication processes with the intent of reusing existing CMOS foundries to save money and smooth the transition of adopting photonic technologies. EBL and DUV each have their own benefits and drawbacks for photonics fabrication. EBL fabrication uses an electron beam to write the pattern onto the substrate. Hence, EBL is known as the "maskless" fabrication and has the benefits of a smaller feature size, and lower production cost per fabrication. This makes EBL very suitable for academics and designers for rapid-prototyping purposes [6]. However, as designs must be written one by one in the EBL process its main drawback is the rate of writing [7], consequentially making it unsuitable for commercial large scale production [6]. Unlike EBL, DUV lithography uses a mask to expose the whole chip schematic all at once onto the substrate [30], hence, DUV lithography is fitting for large volume chip production. Unfortunately, DUV lithography has drawbacks of larger feature sizes, high production costs per fabrication [6], and significant lithography effects [31][32].

Ideally, both processes are utilized to drastically reduce the time from prototyping to commercial production: designers would prototype using EBL until the mature design is ready for DUV lithography mass fabrication. Additionally, the transition from EBL designs to DUV is difficult due to feature size limits and lithography effects. Opportunely, the lithography model proposed in this thesis would enable designers to simulate the DUV lithography effects on their designs. Furthermore, this method could be used to prototype for DUV process using EBL fabrication.

In the next section, the details of DUV lithography are provided starting with an overview of the fabrication process. Afterwards, the lithography effects are described and the examples on various devices are showcased.

1.2.1 Deep-Ultraviolet Lithography

Deep-ultraviolet (DUV) lithography is an optical fabrication process adopted from the fabrication of CMOS circuits [33]. This allowed for lower production costs, higher yields [34] and the potential for photonic integrated circuits

(PIC) to be built alongside CMOS [35][36]. Originally using KrF lasers [7] operating at the 248 nm wavelength [37][38][39][40], modern, state-of-the-art ArF lasers [7] operating at the 193 nm wavelength are being promoted by industry foundries [37][38][39][40]. In photonics fabrication, DUV lithography operates by using a mask and an illumination source to expose areas on the resist on the silicon-on-insulator (SOI) wafer [7][37][31]. The primary machine, known as a wafer stepper, exposes and steps to sections on the wafer, imprinting the circuit design onto the wafer [41]. Hence, DUV lithography has a high rate of production and is suitable for commercialization purposes [34][6]. The individual steps of the lithography process can be summarized [41]:

1. Adhesion promotion: The SOI wafer surface is treated to improve bonding with the resists. Resist coating: The resist, typically made of organic polymers, are applied onto the wafer. A standard method is to apply the resist to the center of the wafer and spun wafer at high speeds to evenly coat the wafer. As the solvent in the resist evaporates, the resist layer becomes solid.

2. Softbake: The wafer with resist is baked to fully dry off any residual solvent.

3. Patterning and Exposure: The mask designs are patterned onto the resist via lithography using ultraviolet light. The exposed resist undergoes a chemical reaction: The selectively of the developer chemical to the resist is determined by the type of mask and resist used. Ultimately the circuit pattern is created onto the resist film.

4. Development: The photonic circuits are created by stripping/etching the resists and underlying silicon layer in selective areas (based on the mask and resist combination).

Prior to the DUV lithography described above, a mask of the desired circuit is created using a maskless process such as electron beam lithography (EBL) [42]. The mask are planes of glasses covered with an opaque material (typically Chromium) [7] [41]. An electron beam exposes the resists on the mask used for DUV fabrication and is then developed using chemicals to create the desired patterns.

On a related note, EBL fabrication is an alternative fabrication method to DUV for silicon photonics fabrication. The EBL SOI fabrication uses direct writing on the SOI wafer by first exposing the resist of the wafer

using an electron beam and then using a reactive ion etch to create the photonic devices onto the wafer [43]. In this thesis, the mentions of EBL will be referring to the EBL SOI fabrication.

There are two types of photomasks: dark-field masks where the pattern areas are etched to allow light to pass, and light-field masks where the pattern areas are etched to block light [7][41][44]. Each type of mask has its own fabrication effect such as linewidth widening/shortening [7][32], thus, fabrications can involve multiple mask types based on the desired devices [7].

Once the mask is ready, the type of resist is considered. Photoresists are categorize into two types: positive and negative [7]. Positive resists have low solubility in the developer chemical and become soluble upon exposure by the DUV light. Negative resists are instead soluable in the developer chemical and become insoluable upon exposure to the DUV light [41]. Based on the designs utilized in the circuit, the mask and resist combination is chosen.

An example of the DUV fabrication process is depicted in Fig. 1.7. The figure shows a light-field mask and positive photoresist combination: The DUV light passes through the light-field photo mask to expose the resist, creating an outline of the desired pattern. As the resist is a positive resist, the exposed areas become soluble to the developer chemical. During the development step, the exposed resist areas (and the silicon underneath those sections) are washed away. A secondary developer targeting only the resist strips the unexposed areas. The result is the desired pattern formed onto the silicon layer. For complex chip designs requiring different layers: the patterning & exposure, and development steps are repeated as necessary.

Figure 1.8 shows an illustration of the characteristic smoothing of a DUV lithography PIC fabrication. A dark-field mask of the desired pattern is shown on the bottom left and an aerial render of the resulting fabrication is shown on the bottom right. It is important to note the smoothing of corners, slight reduction in widths of the patterns, and changes in the gap between the two structures. These lithography effects create difficulties for many photonic devices and lack a solution akin to CMOS optical proximity correction (OPC) methods [14]. OPC defines the smoothing is known as two effects: linewidth shortening and corner smoothing. For simplicity the linewidth shortening and corner smoothing will be referred to as "smoothing effect" in this thesis. There are also "proximity effect", which are dimensional changes induced by structures being placed closely to one another. The smoothing effect and proximity effect are discussed in detail in the next section.

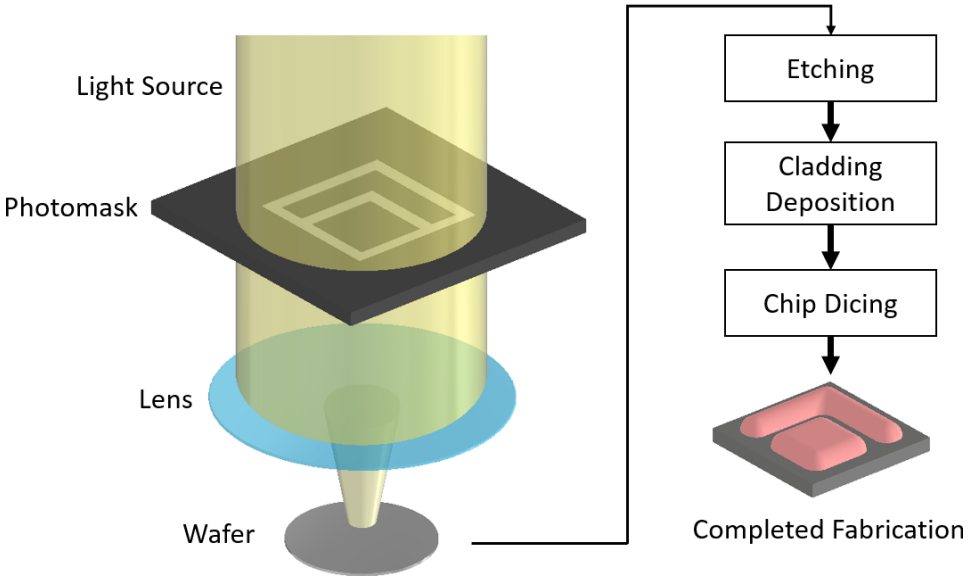


Figure 1.7: A simplified diagram of the DUV Lithography Process. The Optical light is selective filtered using the light-field photomask to create the desired topography shapes. The filtered light beam is then focused via a lens and then imprinted onto the wafer.

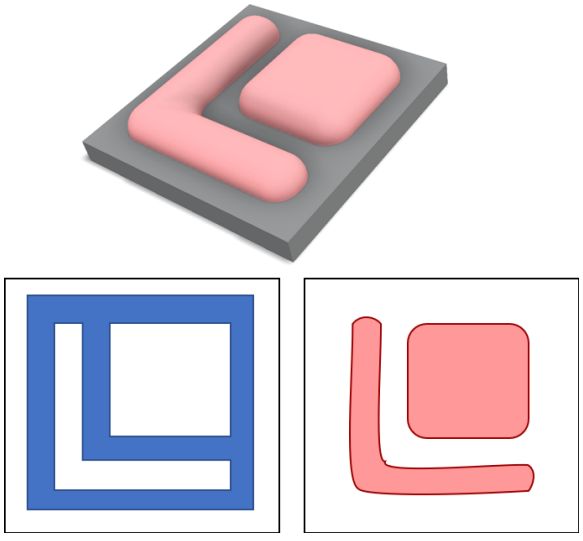
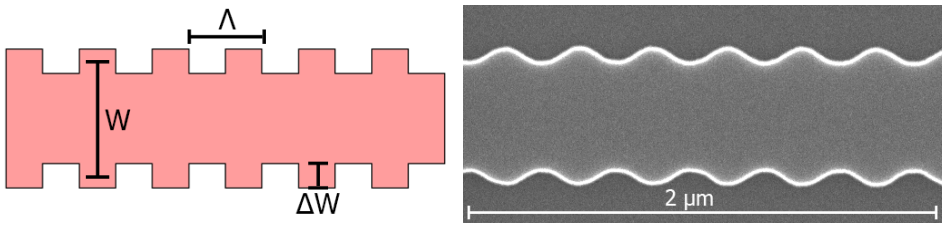


Figure 1.8: An illustration of the shape profile of the silicon device. The dark-field photomask as-drawn design is shown on the left in blue. A top-down view of the resulting fabrication is shown on the right in pink.



(a) As-drawn layout. (b) DUV fabrication.

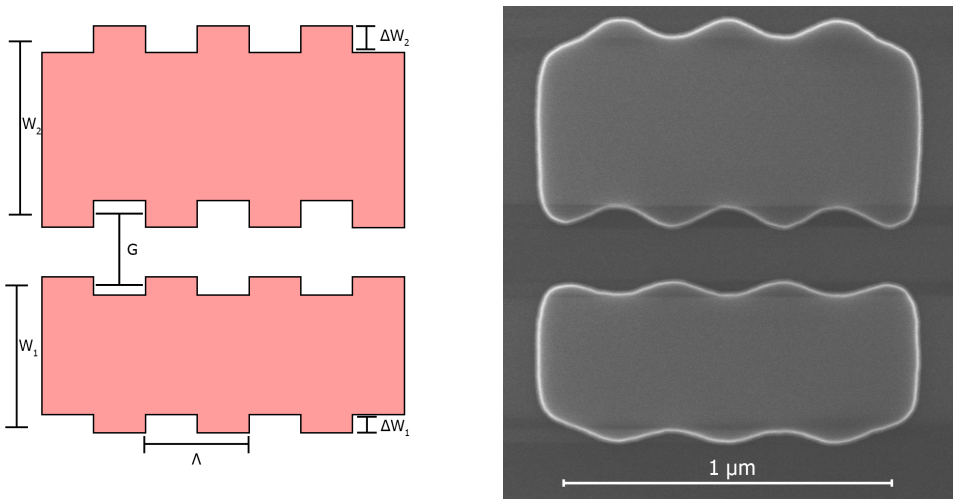
Figure 1.9: The layout and DUV fabrication result of a Bragg grating filter are depicted. The grating is made of rectangular notches which periodically modulate the refractive index. Smoothing effects on the gratings reduce the optical performance. The SEM is taken at 25,000x magnification with 15.00 kV voltage, 50 pA current, using secondary electron mode. The SEM was taken at the University of British Columbia.

1.2.2 Smoothing and Proximity Effects

In this thesis the lithography effects of the deep-ultraviolet (DUV) lithography process are categorized into two categories: smoothing effects and proximity effects. Smoothing effects include the reductions to aerial dimensions (length and width) of the drawn pattern (known as line shortening [7]) and corner rounding [7]. Proximity effects [7] are additional smoothing effects that can occur when a pattern requires two structures to be placed in close range to each other. In silicon photonics, the lithography effects heavily affect the optical responses. Many published devices, such as Bragg filters [8], contra-direcional couplers (contra-DC) [1][9], and sub-wavelength grating devices (SWG) [45] to name a few examples, have attributed lithography effects as the cause for reduced optical performance. The following are three example devices showcasing the lithography effects and the difference between the as-drawn layout and the DUV fabrication:

1) Figure 1.9a illustrates a Bragg grating filter device. The device consists of a waveguide with gear-like notches along the side walls. These sidewalls act like mirrors to reflect the target wavelength(s) backwards, effectively filtering the response of those wavelength(s). The depths of the gratings, known as the corrugation width ΔW, and the pitch Λ are precise parameters chosen based on the target operation wavelength. Figure 1.9b shows the DUV fabrication of the Bragg-grating filter. The ΔW have become sinusoidal-like and their widths reduced significantly.

2) Figure 1.10 shows a contra-DC device consisting of two Bragg grating

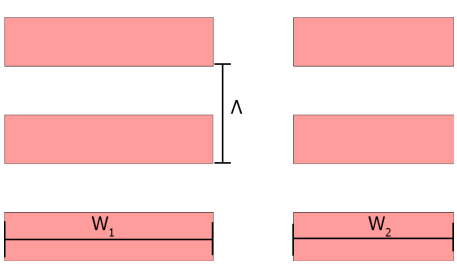


(a) As-drawn layout. (b) DUV fabrication.

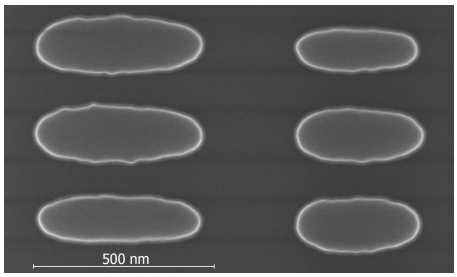
Figure 1.10: The layout of a contra-directional coupler and SEM image of the DUV fabrication are depicited. The device functions similar to a Bragg grating filter. An additional complexity is introduced in the form of a second coupling grating waveguide. As seen from the SEM image, the device is prone to smoothing of the gratings and proximity-effects at coupling region between the two waveguides. The SEM is taken at 65,000x magnification with a voltage of 15 kV, current of 50 pA, using secondary electron mode. The SEM was taken at the University of British Columbia.

filters placed within coupling range from each other. The coupling distance, referred to as the gap, affects the coupling power between the waveguides: a smaller gap results in substantial increased coupling. Hence, the gap is approaching fabrication feature size limits. As such, the gap of the contra-DC oftens exhibits proximity effects post-fabrication. Figure 1.10b shows the DUV fabrication of the contra-DC. The gratings are smoothed in a similar manner as the Bragg grating filters. The proximity effect can be seen between the two waveguides: The gratings of the coupling region are smoothed more than the gratings on the outer waveguide edge resulting in a mismatch of the ΔW parameter and thus undesired optical response changes.

3) Figure 1.11 illustrates the layout of a SWG device. The device consists of rectangular silicon structures placed at a fixed spacing (Λ). The widths of the rectangles (W) and the Λ are chosen with respect to the tar-



(a) As-drawn layout.



(b) DUV Fabrication.

Figure 1.11: The layout and DUV fabrication of a SWG coupler are depicted. The DUV fabrication rounds the gratings noticibly. Furthermore, proximity effects can be seen; the distance between gratings on both the right side vary. The SEM is taken at 120,000x magnification with a voltage of 15 kV, current of 50 pA, using secondary electron mode. The SEM was taken at the University of British Columbia.

get operating wavelength. Figure 1.11b shows the DUV fabrication in which the rectangular gratings have become oblong due to the smoothing effects. Also, there are proximity effects between each grating of the same waveguide resulting in different gaps between the gratings.

To summarize, the examples demonstrate the smoothing and the proximity effect. The SEM images depict a clear difference between the as-drawn layouts and the fabrication. As small geometric changes can greatly reduce optical performance, it is necessary to develop a lithography model.

Chapter 2

Cross-Sectional Analysis of Contra-DCs

In this thesis, the contra-directional coupler (contra-DC) is used as a benchmark device to verify the lithography model. Since the lithography model only considers the aerial shape profile of the device it is important investigate optical performance changes due to the cross-section geometry. In this chapter we conduct an analysis on the contra-DC at various sidewall angles and boundary cases of waveguide height variations. We compare the bandwidth and central wavelength to determine which value is unaffected by the cross-sectional changes and therefore would be suitable to evaluate the top-down lithography effects of DUV. The values for the sidewall angle and wafer thickness are chosen based on the fabrication process specifications provided by the foundry.

The results are from 3D-Finite-Difference-Time-Domain (FDTD) simulations performed using Lumerical Inc.'s FDTD software. We compare the optical performance of the contra-directional coupler, specifically the center wavelength and bandwidth of the device.

Two sets of width parameters were used in the contra-DC of this thesis. As such, an analysis is performed for each of the following: 1) widths $W_{1,2}$=560, 440 nm, period Λ=318 nm, gap=160 nm, and corrugation widths of $\Delta W_{1,2}$=50, 30 nm. 2) widths $W_{1,2}$=370, 270 nm, period Λ=325 nm, gap=185 nm, corrugation widths of $\Delta W_{1,2}$=60, 50 nm, and a 90 nm high slab layer.

Figure 2.1 shows a schematic of how our variations are modelled in the software. Regarding sidewall angles, we measure the angle from the base of the device forming a trapezoid cross section. The width of the waveguide is defined to be located at the center of the structure height-wise, and measured horizontally to the opposite edge.

Regarding sidewall angles, Table 2.1 provides the range of parameters and the corresponding center wavelengths and bandwidths.

Figure 2.2 illustrates the cross-sectional geometry assumed in this analysis. Figure 2.3 shows a SEM image of a contra-directional coupler fabricated

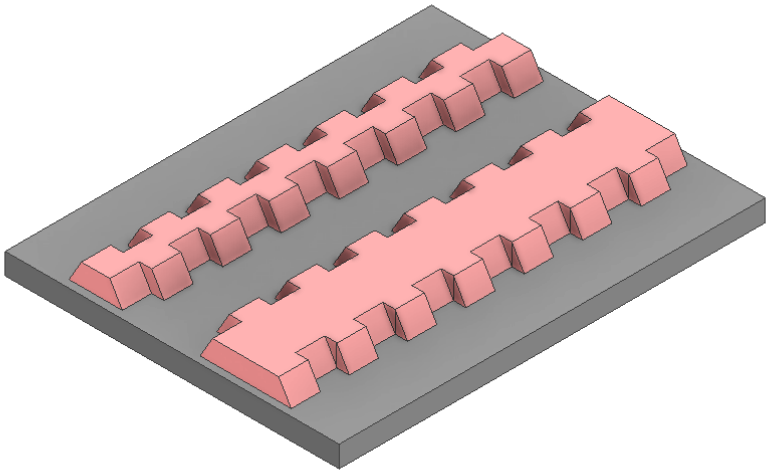


Figure 2.1: Orthogonal view of the schematic used for 3D-FDTD simulations depicting sidewall angles on the grating faces.

in a DUV process, verifying the geometric assumption.

We define two figures of merit for simplified comparison: 1) The averaged change in bandwidth/central wavelength per change in angle. 2) The averaged change in bandwidth/central wavelength per change in waveguide height.

Regarding the sidewall angles, the bandwidths and central wavelength for at each angle increment is listed in Table 2.1 for $W_{1,2}$=560, 440 nm and Table 2.2 for $W_{1,2}$=370, 270 nm.

For a contra-DC of $W_{1,2}$=560, 440 nm the figures of merit are $\frac{\Delta\Delta\lambda}{\theta}$=0.012 $\frac{nm}{\theta}$ for the bandwidth and $\frac{\Delta\lambda_0}{\theta}$=0.033 $\frac{nm}{\theta}$ for the central wavelength. This indicates that the sidewall does not have significant impact on the bandwidth nor the central wavelength (less than 1 nm per angle in both cases).

For a contra-DC of $W_{1,2}$=370, 270 nm the figures of merit of $\frac{\Delta\Delta\lambda}{\theta}$=0.026 $\frac{nm}{\theta}$ for the bandwidth and $\frac{\Delta\lambda_0}{\theta}$=0.429 $\frac{nm}{\theta}$ for the central wavelength. This indicates that devices using this width parameter have bandwidths that are tolerant to the sidewall angle but the central wavelengths is sensitive to changes (shifting nearly 0.5 nm per angle).

Figure 2.2: Cross-sectional profile of the contra-directional coupler device depicting the sidewall angles. The angle variation locations are labelled in green.

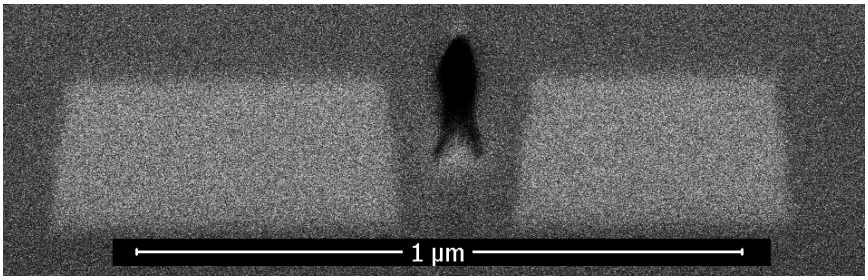


Figure 2.3: Cross-sectional SEM of a contra-DC demonstrating sidewall angles taken at 64,963x magnification using a voltage of 2.00 kV, current of 0.10 nA, in back-scatter electron mode. The pocket located between the two trapezoidal silicon structures is a manufacturing error. The SEM was taken at the University of British Columbia.

Angle (Θ)	Bandwidth (nm)	Center Wavelength (nm)
90°	7.49	1534.66
85°	7.45	1534.76
80°	7.47	1534.88
75°	7.59	1535.14

Table 2.1: Bandwidth and central wavelength for a contra-DC of $W_{1,2}$= 560, 440 nm at various angles.

Angle (Θ)	Bandwidth (nm)	Center Wavelength (nm)
90°	16.63	1351.765
85°	16.88	1349.58
80°	16.94	1347.45
75°	17.02	1345.33

Table 2.2: Bandwidth and central wavelength for a contra-DC of $W_{1,2}$= 370, 270 nm at various angles.

Waveguide Height (nm)	Bandwidth (nm)	Center Wavelength (nm)
215	7.53	1528.19
220	7.49	1534.66
225	7.65	1541.29

Table 2.3: Bandwidth and central wavelength for a contra-DC of $W_{1,2}$= 560, 440 nm at various waveguide heights.

Waveguide Height (nm)	Bandwidth (nm)	Center Wavelength (nm)
215	16.38	1350.52
220	16.63	1351.765
225	17.09	1355.645

Table 2.4: Bandwidth and central wavelength for a contra-DC of $W_{1,2}$= 370, 270 nm at various waveguide heights.

Regarding wafer height variations, we performed a corner analysis using the expected height variation provided by the foundry. The results for $W_{1,2}$=560, 440 nm are listed in Table 2.3 and Table 2.4 for $W_{1,2}$=370, 270 nm.

For a contra-DC of $W_{1,2}$=560, 440 nm the figures of merit are $\frac{\Delta\Delta\lambda}{h}$=0.020 $\frac{nm}{nm}$ for the bandwidth and $\frac{\Delta\lambda_0}{h}$=1.31 $\frac{nm}{nm}$ for the central wavelength. This indicates the bandwidth is insensitive to height variations but the central wavelength is highly sensitive (shifting more than 1 nm per nm of height change).

For a contra-DC of $W_{1,2}$=370, 270 nm the figures of merit are $\frac{\Delta\Delta\lambda}{h}$=0.071 $\frac{nm}{nm}$ for the bandwidth and $\frac{\Delta\lambda_0}{h}$=0.513 $\frac{nm}{nm}$ for the central wavelength. The figures of merit show that the bandwidth remains tolerant to the height changes while the central wavelength will have a noticeable change (shifting by 0.5 nm per nm of height change).

From the results we conclude that the bandwidth is insensitive to the sidewall angles and waveguide height variations as each respective figure of merit shows insignificant change. Concurrently, the central wavelength has shown high sensitivity to the sidewall angles and waveguide height variations in each respective analysis. Hence, the bandwidth of the contra-DC is a suitable choice for verification of the lithography model, as the changes to the bandwidth can be attributed to solely the aerial smoothing and proximity effects.

Chapter 3

Computational Lithography Model

The computational lithography model is built using the known parameters of the 193 nm DUV process, estimated parameters of the process, and feature size measurements obtained from a fabricated test pattern set. The parameters of the model are optimized such that the error between the predicted feature sizes and the measured feature sizes are minimized. As the model is built from a fabricated test pattern, it is foundry process specific. However, our methodology in building the model can be applied generally to any foundry process.

The model is built using Mentor Graphics Calibre software [46]. A standardized test pattern set is included in the software. Figure 3.1 shows the SEM of a section of the test pattern. Each test structure in the test pattern set has a feature size of interest, e.g., a gap or width, from which we take measurements. These feature size measurements are also known as critical dimension (CD) measurements.

3.1 Test Pattern Data Extraction

The test pattern set consists of 216 structures. The various structures used are depicted in Fig. 3.2. The structures can be categorized into "solid" and "inverse" structures. Solid structures have the surrounding silicon removed to obtain their shape, as shown in Figs. 3.2a - 3.2h. Their inverse counterparts are negative imprints of the structure, as shown in Fig. 3.2k - 3.2l. As the solid and inverse pairs share the same as-drawn CD, it is anticipated that they would fabricate similarly. However, in each case, the as-fabricated CD trends of the solid and inverse pairs are different. Figure 3.3 shows the trends

A version of Chapter 3 has been published: S. Lin, M. Hammood, H. Yun, E. Luan, N. A. F. Jaeger and L. Chrostowski, "Computational Lithography for Silicon Photonics Design," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 26, no. 2, pp. 1-8, March-April 2020, Art no. 8201408.

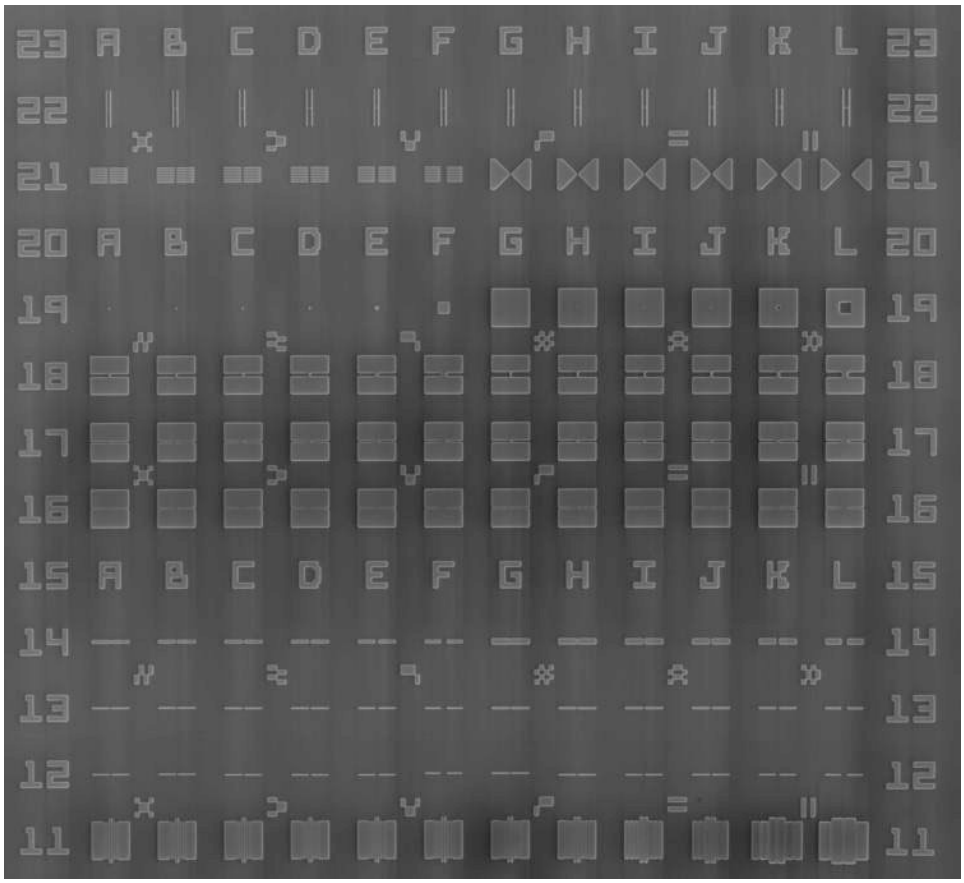
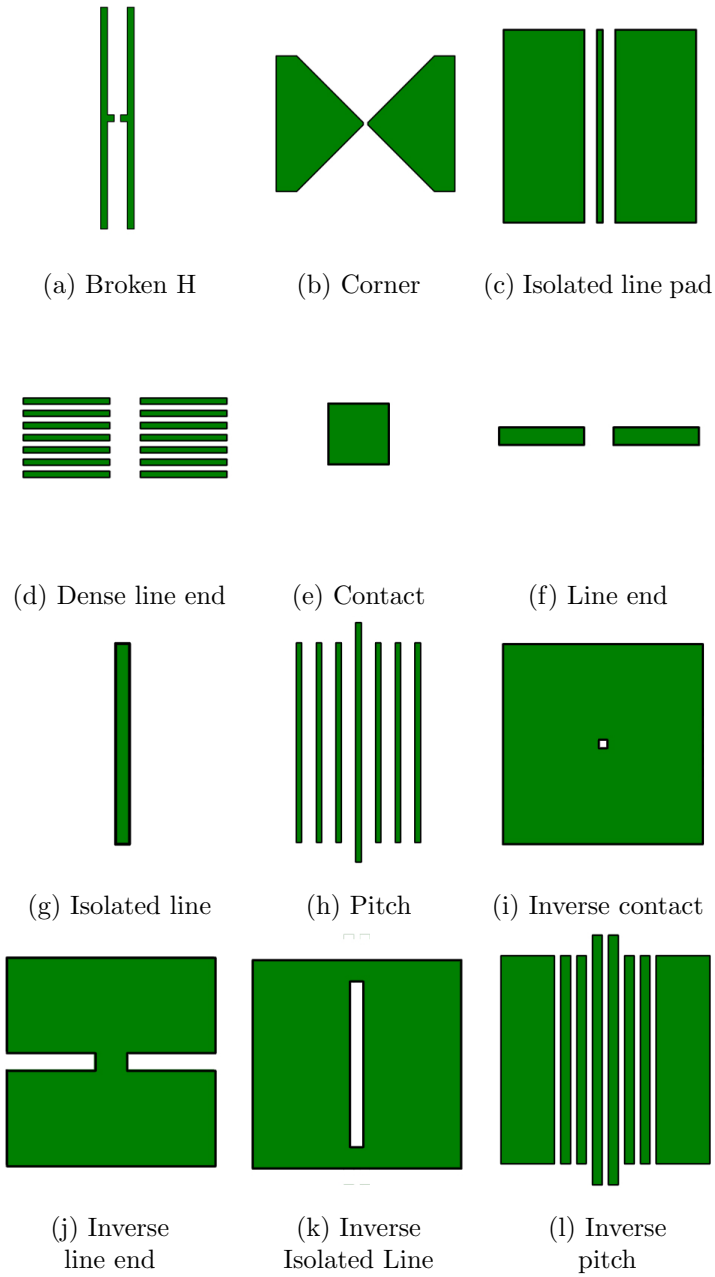


Figure 3.1: The SEM of a section of the test pattern is depicted. This SEM is obtained by stitching together individual SEM images of the patterns each taken at a magnification of 5000x, a voltage of 20 kV, and a current of 0.10 nA.



(a) Broken H (b) Corner (c) Isolated line pad

(d) Dense line end (e) Contact (f) Line end

(g) Isolated line (h) Pitch (i) Inverse contact

(j) Inverse line end (k) Inverse Isolated Line (l) Inverse pitch

Figure 3.2: The types of structure included on the standard test pattern are illustrated. The structures consist of solid structures ([a] to [h]), and inverse structures ([i]) to [l]).

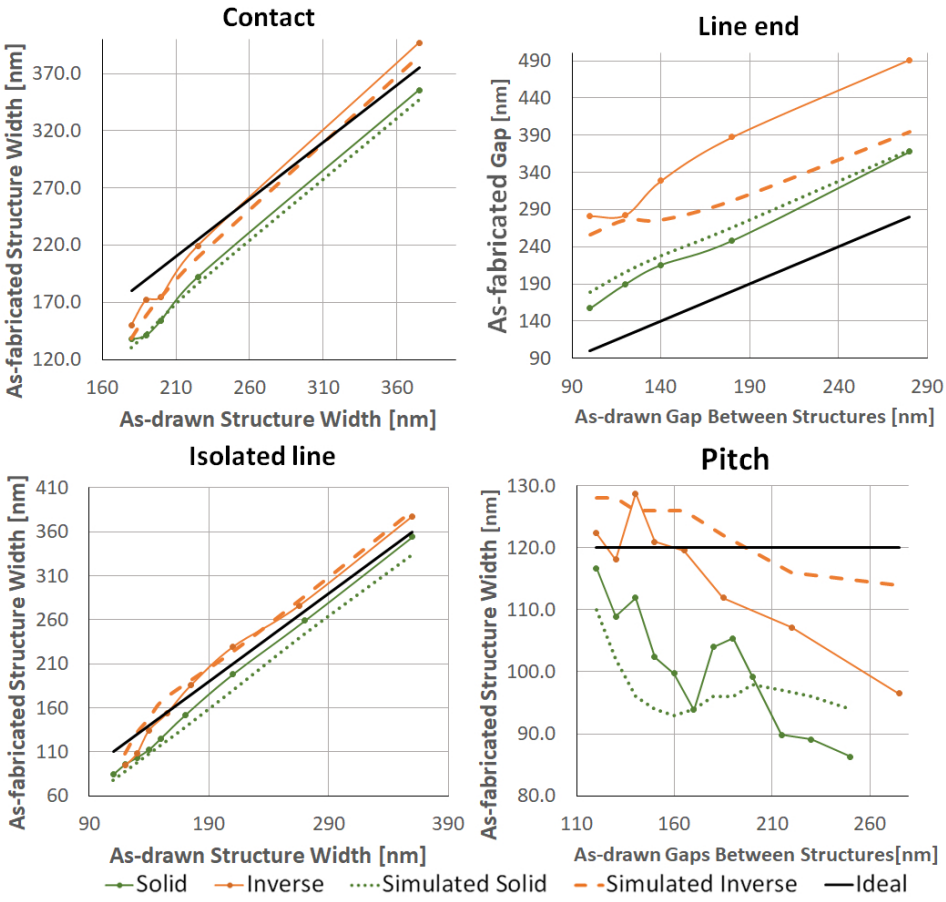
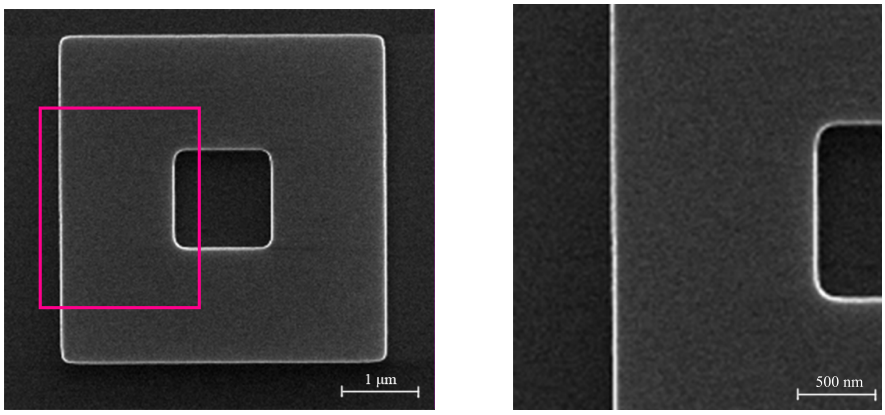


Figure 3.3: The as-fabricated CDs are plotted against the as-drawn CDs for the structures shown in Fig. 3.2e - 3.2l. Each solid structure and their inverse counterpart have shown different CD trends, indicating different process biases are required for each type of structure. The simulated CDs are also included to compare the closeness of the lithography model.

of the as-fabricated CDs for the solid and inverse structures. This indicates that different process biases are needed for different structures. Overall, the aim is to capture the photolithography effects on possible shapes that a designer might draw. SEM images are used to obtain the CD measurements of each structure on the fabricated test pattern. The measurements are performed by counting the pixels between the two locations we wish to measure. The number of pixels is then converted to SI units using a scale provided by the SEM image. The SEM images, shown in Fig. 3.4, 3.7, and 3.8, are taken using the Helios NanoLab 650 scanning electron microscope at a magnification of 5000x, using a voltage of 20 kV, and a beam current of 0.10 nA. The white borders of the structures in the SEM images (Fig. 3.4a) make it difficult to discern where a pixel measurement should be taken. As the white borders are very thick (Fig. 3.4b), a particular measurement depends on where we define the edge of the structure. To address this problem, our convention uses the average distance of the outer and inner edge of the white border. Here we are assuming that the white borders occur due to sidewall angles cause by fabrication processes [47] and that the sidewalls have a linear slope from the top to the bottom of the structure.



(a) Square hole test structure (b) Magnification of the edge

Figure 3.4: (a) An SEM of an Inverse Contact structure. (b) A zoom-in illustrating the thick white border can create CD measurement discrepancies. Our convention is to use the average distance between the outer and inner edge of the border.

3.2 Model Optimization

Calibre provides an optimization function which operates by adjusting the lithography model parameters within the aforementioned range. The optimization aims to minimizes the error between the predicted CD and the as-fabricated CD. The model's inputs are the optical lithography wavelength and each test pattern's measured CD. The optimized output produces 4 parameters of the lithography model: 1) the optical wavelength of the DUV process; 2) the NA, which is a dimensionless number that describes the ranges of angles of the projection lens seen from the position of the wafer; 3) the σ, defined as the fraction of the NA of the projection lens filled by the illuminating beam [46]; and 4) the $\delta\sigma$, defined as the delta ranges from which the intensity of the optical beam rises from 0.5% to 99.5% [46]; and 5) the threshold value, defined as the percentage of the computed illumination which is applied.

The optical wavelength is known for the 193 nm DUV dry-etch process. Unfortunately, the NA, σ, $\delta\sigma$, and the exposure threshold, are not publicly available. Hence, we instead refer to values given in previous publications for similar processes [48][49][7] to determine a range for optimization.

The optimization is performed by sweeping the NA, σ, and $\delta\sigma$ parameters, and generating a lithography prediction of the test patterns. The sweep aims to obtain the lowest error root-mean-square value for the predicted CDs versus the as-fabricated CDs. Figure 3.5 plots the NA sweep versus the error root-mean-square value. The sweep is performed in a 3-dimensional search space (as we are optimizing three parameters, the NA, σ, and $\delta\sigma$ values). The parameters starting point begin at NA $= 0.6$ $\sigma = 0.6$, and $\delta\sigma = 0$ of which the NA and σ values reported from a previous publication [8]. The ranges for the sweeps are chosen from values reported in the literature [48][49], as well as being based on our own estimations.

The equation for the error root-mean-square is shown in Equation 3.1. W_i is the weight value for each CD measurement, CD_{sim} is the CD measurement prediction by the model, and CD_{meas} is the measured CD obtained from SEM images.

$$ErrorRMS = \sqrt{\frac{\sum_i W_i (CD_{sim} - CD_{meas})^2}{\sum_i W_i}} \tag{3.1}$$

During each sweep of the optimization, the optical parameters are used to generate a computed illumination of a structure's mask, as shown in Fig. 3.6b. Next, a lithography prediction is generated using a threshold value.

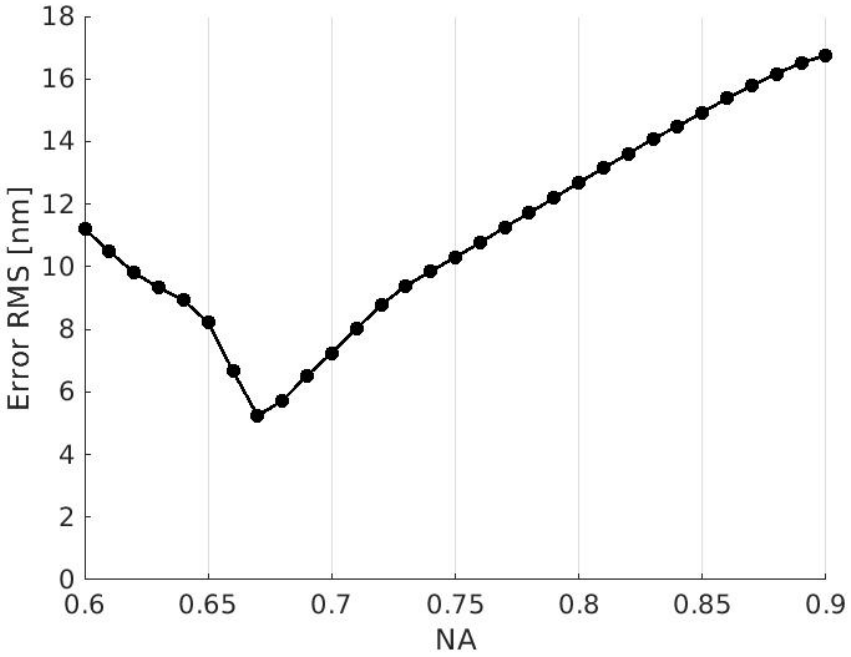
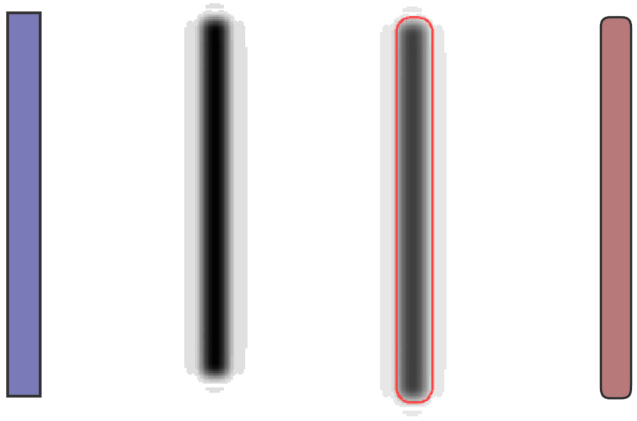


Figure 3.5: A 1-dimension search (varying numerical aperture) is presented. The error root-mean-square is plotted against the numerical aperture. The error root-mean-square is obtained by comparing the lithography predictions of the model to the CD measurements. The search aims to obtain the parameter value which produces the minimal error root-mean-square value. In the plot, the optimal value for NA is 0.67 with an error root-mean-square of 5.237 nm. The entire model building process performs this search in 3-dimensions (varying NA, σ, and $\delta\sigma$).

The threshold value is the percentage of the predicted illumination that will be applied to the structure. The optimization will select the threshold value producing the best fit (Fig. 3.6c). The error between the CD measurements are then evaluated against errors from previous sweeps. The optimization continues until a combination of parameters with the minimum error is found (Fig. 3.6d). The optimized lithography model has the following parameters: NA = 0.671, $\sigma = 0.884$, $\delta\sigma = 0.882$, and threshold = 0.165.



(a) Mask (b) Optical (c) Threshold (d) Output

Figure 3.6: Steps to optimize the lithography model: (a) the ideal as-drawn mask. (b) the computed illumination generated using the optical wavelength, NA, σ, and $\delta\sigma$. (c) the selection of the threshold value, shown in red. (d) the predicted post-lithography output.

3.3 Verification

In this section we verify the lithography model using two comparison methods. First, we visually evaluate the accuracy of the lithography model. We compare the overall shape and CD measurements of predicted structures to those of the as-fabricated structures obtained from SEM images. Second, we compare the optical responses of contra-DC devices. The simulated responses of the as-drawn designs and the predicted designs are compared against experimental responses.

As regards the visual verification, Fig. 3.7 shows the Broken H structure which has an as-drawn gap of 120 nm. The computational lithography

results predict a gap of 182 nm. The predicted gap (182 nm) closely matches with the fabricated gap (181 nm) shown in SEM images. Other features, such as the end roundings, are common to both the predicted and fabricated structures. Figure 3.8 shows a Corner structure predicting the effects on close-proximity corners. In this structure, the as-drawn gap between the two tips of the corners is 150 nm. Our computational lithography predicts a gap of 214 nm. This is very similar to the SEM image which shows a gap of 210 nm. Visually, the output of the computational lithography model corresponds very closely to the as-fabricated test patterns.

Figure 3.3 shows a plot of the CD of the contact, line end, isolated line, and pitch patterns (note the change in scale for the vertical axis of the pitch pattern). The model is able to produce results comparable to the measured CD. However, the models predictions are less accurate for the inverse line end pattern; The cause for this requires further investigation.

As regards the optical response, Fig. 3.9 illustrates the schematic of a contra-DC device. The device consists of two coupled Bragg-grating waveguides. The bandwidth of the contra-DC is sensitive to the corrugation widths (ΔWs), e.g., small changes in the ΔW will cause large changes in the bandwidth. The contra-DCs used in our comparison have the anti-reflection configuration described in Ref. [50]. Each contra-DC consists of two waveguides with different widths, and, hence, different propagation constants. The main band of each contra-DC will be centered at an operating wavelength at which the phase-match condition [18][50] is satisfied.

However, two side-bands, known as the self-reflection (SR) bands, will exist next to the "main band" for the contra-directional coupling on the contra-DC [50]. The SR bands occur due to each mode of the two waveguides having their own propagation constants leading to the conventional single-waveguide Bragg reflection at a wavelength of $\lambda_{1,2} = 2n_{\text{eff }1,2}\lambda_0$, where $n_{\text{eff }1,2}$ correspond to the effective indices for the waveguide modes located mainly in waveguide 1 and 2, respectively. For broad spectrum applications, there is an appeal to reduce the SR as the SR bands limit the operating spectral ranges.

Figure 3.10 demonstrates the photolithography effects on the contra-DC. Coupling gaps can increase and ΔWs of the device can become mismatched between the inner and outer portions. As the asymmetry between the ΔWs increases, the SR bands on the drop-port of the contra-DC become increasingly prominent. As the SR bands are related to the individual modes, and by extension the waveguide widths, small variations in the ΔWs, gap, and widths, will significantly change the main bandwidth and the SR bandwidths [50]. In our experimental results, the SR bands are approximately

40 nm away from the main band. Due to measurement limitations, we will be comparing SR nulls bandwidth at the shorter wavelength.

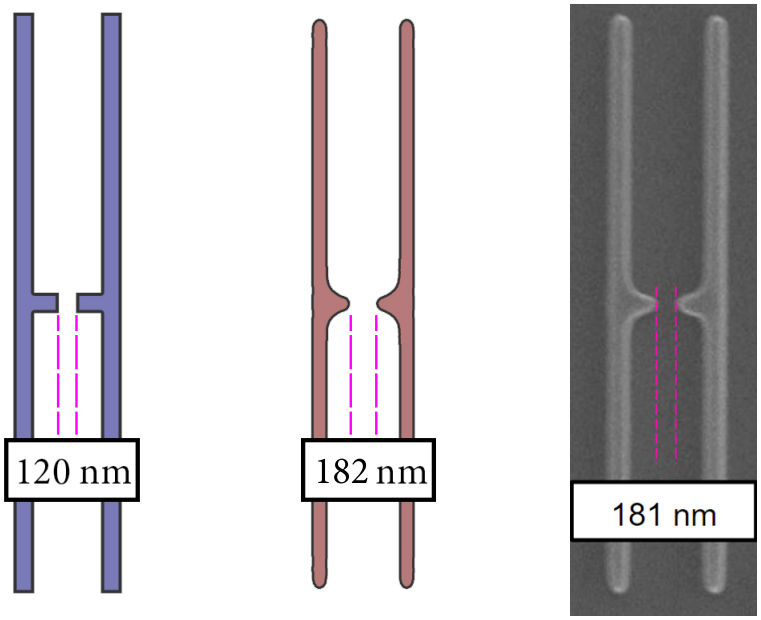
The simulated response of the as-drawn device is not accurate enough to match the as-fabricated result, as demonstrated in Fig. 3.11 for the main band and Fig. 3.12 for the SR band. Thus, it is apparent that the photolithography effects of the fabrication process have heavily impacted the contra-DC's performance.

Using the lithography model, we predict the resulting shape of the contra-DCs after photolithography effects have been taken into account. The parameters of each of our contra-DCs are listed in Table 3.1. We perform a Finite-Difference-Time-Domain (FDTD) simulation using Lumerical Inc.'s FDTD software and bandstructure method [17]. The coupling coefficient, kappa, and bandwidths are extracted from the bandstructure. The contra-DC response is then simulated using kappa and a Couple-Mode-Theory-Transfer-Matrix-Method based model [26][22][51]. We calculate the nulls bandwidths of the experimental results listed in Table 3.2 and Table 3.3 using the nulls method [52].

Figure 3.11 shows the main band response of our CDC3 device. The as-drawn simulation (Fig. 3.11a) shows an ideal bandwidth of 11.5 nm. Our as-predicted simulation (Fig. 3.11b) shows a reduced bandwidth of 5.6 nm. The actual (experimental) bandwidth of 6.4 nm (Fig. 3.11c) closely correlates with the predictions of the lithography model.

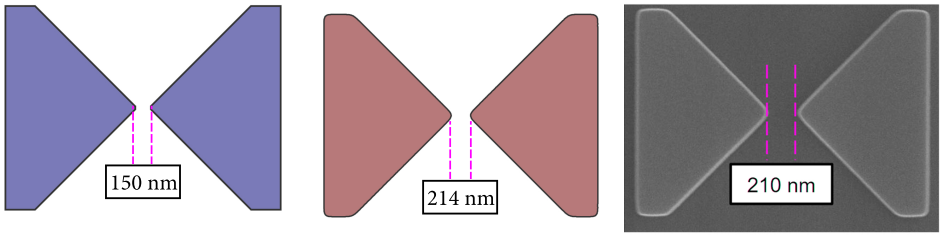
Furthermore, Fig. 3.12 shows the SR band response of our CDC3 device. The drop-port response is illustrated for readability purposes. In the ideal as-drawn simulation, the SR bandwidth is shown to be 11.1 nm (Fig. 3.12a). Using the lithography model, we predict that the bandwidth will be reduced to 6.0 nm (Fig. 3.12b). The experimental result, shown in Fig. 3.12c, has a SR bandwidth of 5.4 nm.

Figure 3.13 and Figure 3.14 show the main band nulls bandwidths and the SR band nulls bandwidths respectively, for the as-drawn simulation, the as-predicted simulation and the experimentally measured results. The ideal as-drawn simulations include process width variations from Ref. [53]. Each as-predicted simulation showed a significant improvement in accuracy over the as-drawn simulation for both the main nulls bandwidth and the SR nulls bandwidth.



(a) Test Pattern (b) Simulation (c) Fabricated

Figure 3.7: A Broken H structure is depicted. The CD location is between the two center protrusions and captures how small grating-like structures will be effected by photolithography. The CD predicted by our method (b) is nearly identical to the fabricated one (c).



(a) Test Pattern (b) Simulation (c) Fabricated

Figure 3.8: The Corner structure, which captures how two corners interact when in close proximity, is depicted. The resulting CD from our simulation is highly similar to that of the fabricated one.

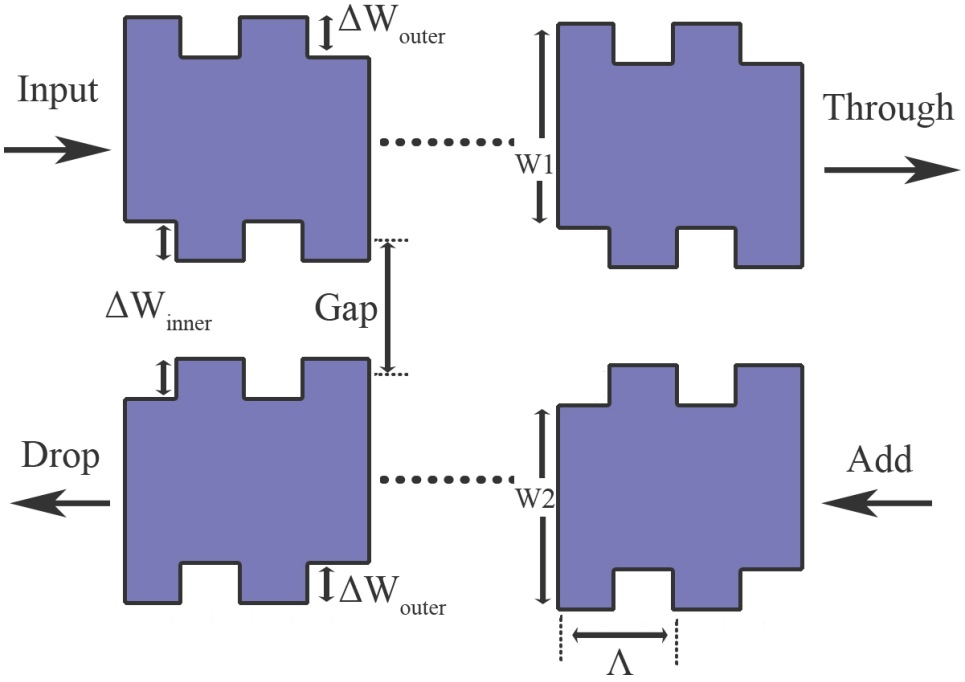
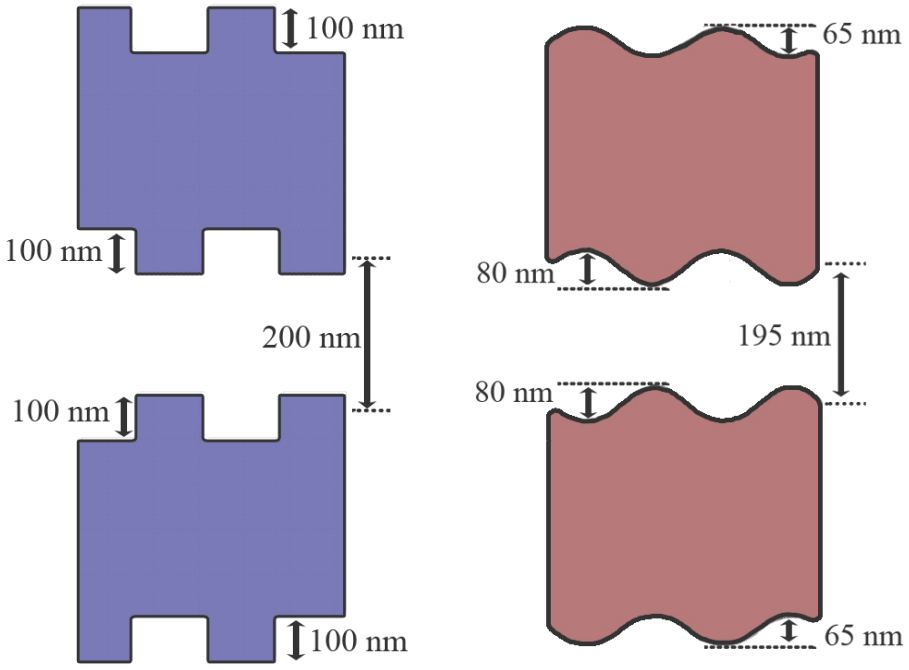


Figure 3.9: The schematic of a contra-DC, with the design parameters and the four ports labeled. A single segment block of the Bragg grating with a pitch (Λ) is repeated to obtain a desired length. There are two corrugation widths (ΔWs), which will often be affected differently by the fabrication process.

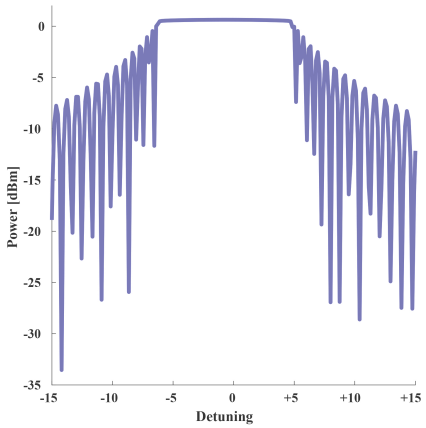
Table 3.1: Contra-DC Parameters

Device Name	Λ (nm)	Width 1 (nm)	Width 2 (nm)	Gap (nm)	ΔW 1 (nm)	ΔW 2 (nm)	Length (μm)
CDC1	270	370	270	175	60	50	270
CDC2	270	370	270	178	60	50	270
CDC3	325	370	270	185	60	50	325
CDC4	325	370	270	182	60	44	325

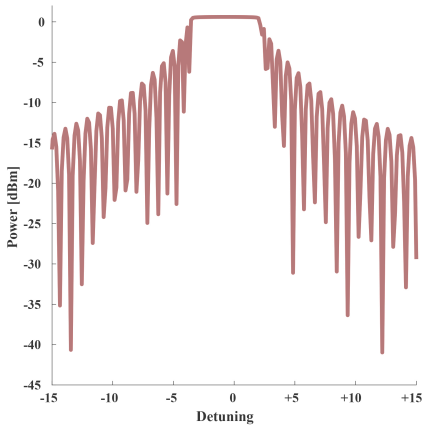


(a) Ideal Mask (b) As-Predicted Mask

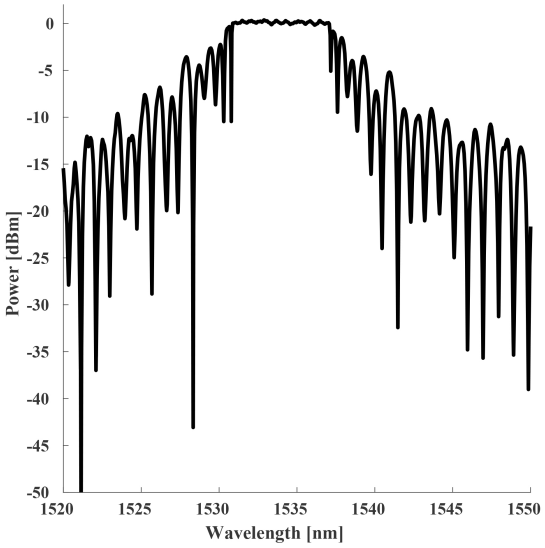
Figure 3.10: (a) A simplified contra-DC design, with symmetrical waveguide widths and ΔWs to demonstrate the smoothing and the proximity effects of photolithography. (b) The post-fabrication changes in the gap, ΔW_{inner}, and ΔW_{outer} dimensions are depicted, showing a large asymmetry between the ΔWs. The size reduction of ΔW_{inner} is due to both the smoothing, and proximity effects, where as the size reduction of ΔW_{outer} is only due to the smoothing effect.



(a) Simulated main band response of the as-drawn contra-DC

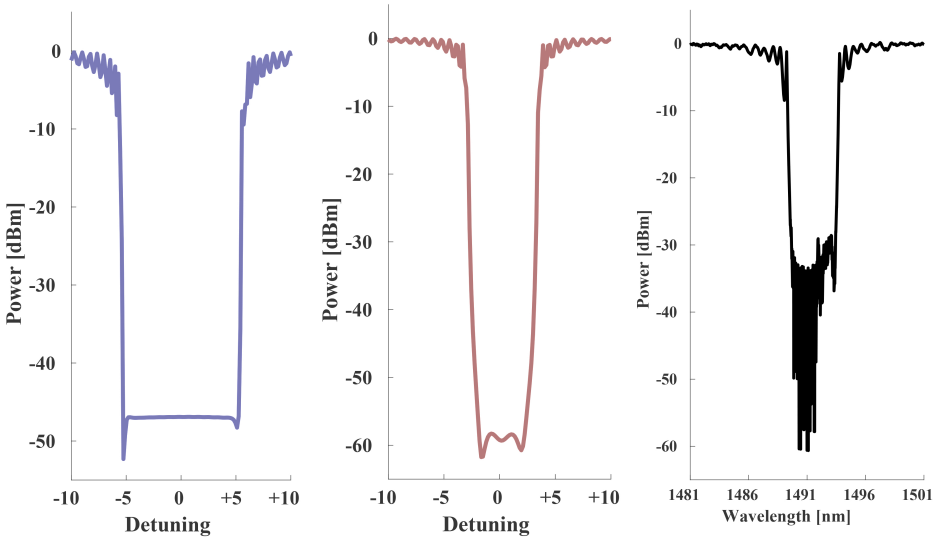


(b) Simulated main band response of the as-predicted contra-DC



(c) Measured main band response of the fabricated contra-DC

Figure 3.11: The main band nulls bandwidths of CDC3. (a) The as-drawn layout, (b) the lithography model as-predicted, and (c) the DUV as-fabricated, are depicted. The as-drawn simulated nulls bandwidth is 11.5 nm, the as-predicted nulls simulated bandwidth is 5.6 nm, and the as-fabricated measured nulls bandwidth is 6.4 nm. The noise floor of c) is due to instrument measurement limitations.



(a) As-drawn (b) As-predicted (c) Fabricated

Figure 3.12: The SR nulls bandwidths of (a) the as-drawn, (b) the as-predicted, and (c) the as-fabricated, are depicted. The as-drawn simulated bandwidth is 11.1 nm, the as-predicted simulated bandwidth is 6.0 nm, and the as-fabricated measured bandwidth is 5.4 nm.

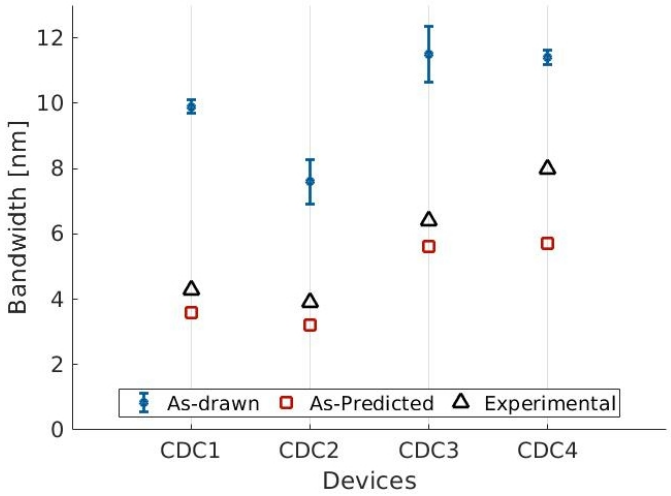


Figure 3.13: The contra-DC main band nulls bandwidths for the as-drawn (blue I-bars), the as-predicted (red squares), and experimentally measured (black triangles) contra-DC devices are plotted. The data values can be found in Table 3.2.

Table 3.2: Contra-DC main band Bandwidths

Device Name	Ideal As-Drawn (nm)	Lithography As-Predicted (nm)	Experimental (nm)
CDC1	9.9 ± 0.22	3.6	4.3
CDC2	7.6 ± 0.68	3.2	3.9
CDC3	11.5 ± 0.85	5.6	6.4
CDC4	11.4 ± 0.22	5.7	8.0

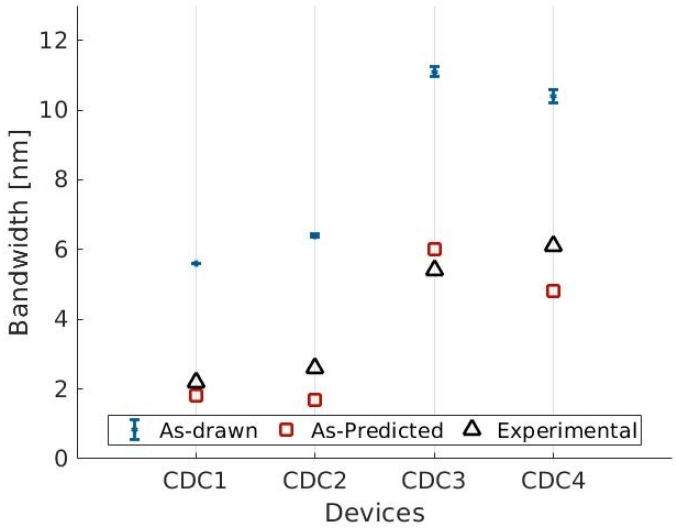


Figure 3.14: The contra-DC self-reflection band nulls bandwidths for the as-drawn (blue I-bars), the as-predicted (red squares), and experimentally measured (black triangles) contra-DC devices are plotted. The data values can be found in Table 3.3.

Table 3.3: Contra-DC SR-band Bandwidths

Device Name	Ideal As-Drawn (nm)	Lithography As-Predicted (nm)	Experimental (nm)
CDC1	5.6 ± 0.009	1.8	2.2
CDC2	6.4 ± 0.051	1.7	2.6
CDC3	11.1 ± 0.134	6.0	5.4
CDC4	10.4 ± 0.190	4.8	6.1

Chapter 4

Designing for Manufacturability

Here, we demonstrate the application of the lithography model for preemptive compensation of fabrication changes and present two ideas for improving manufacturability on the deep-ultra violet (DUV) process are explored. First, the potential for using the Electron Beam Lithography (EBL) process in conjunction with the lithography model to emulate a DUV lithography process is discussed. The method takes advantage of the small feature size capabilities of EBL to precisely fabricate the predicted shapes from the lithography model. Second, the designer-side compensation for lithography effects is presented. Using a contra-directional coupler (contra-DC) design presented previously for verification, the lithography effects predicted by the model are analyzed and the contra-DC design is modified to counteract the lithography changes.

4.1 DUV-Emulation using EBL

EBL is a popular fabrication process well-suited for rapid-prototyping with features such as fast fabrication cycles, small minimum feature sizes, and low cost. However, given the nature of the EBL process, it has a longer patterning time and is unsuitable when the production volume is large. To make the leap to commercialization, silicon photonic devices would need to rely on optical lithography processes, such as DUV, which are capable of handling large volume fabrications. Unfortunately, DUV lithography has different limitations than EBL such as lithography effects which makes devices difficult to produce with the DUV process. Furthermore, DUV has high production costs and longer fabrication cycles than EBL, effectively inhibiting its use as a rapid-prototyping process.

However, with the lithography model demonstrated in the previous chapters, the EBL process has the potentially to be used as an intermediate step for the DUV emulation method. The method uses the lithography model

to simulate a DUV fabrication outcome. The simulated result is then fabricated via EBL. Alterations can be considered after obtaining measurements and the iteration cycle can then be repeated. Ultimately, when there is confidence in the device's success, designers can then decide to invest in a DUV process, consequently, reducing the overall cost of prototyping for device to be fabricated using the DUV process.

To evaluate our emulation method, we compared the bandwidths of multiple Bragg filter and contra-DC devices. We fabricated the devices using the EBL and DUV processes. We also fabricated our lithography predictions using the EBL process (which we will be referring to as EMU). The Bragg filters have parameters: W=500 nm, Λ=318 nm, and a sweep of the corrugation ΔW from 20 to 105 nm. The contra-DCs used have parameters: $W_{1,2}$=560, 440 nm, Λ= 318 nm, $\Delta W_{1,2}$= 50, 30 nm, G = 220 nm.

Figure 4.1 shows the bandwidths of the Bragg filter devices. The EBL measurements are plotted in blue, the DUV measurements are plotted in purple, and the EMU measurements are plotted in orange. Using the EBL bandwidths as a baseline for comparison, the DUV bandwidths are noticeably smaller. This is expected as the corrugation widths of gratings are characteristically reduced in the DUV process. The EMU bandwidths show good agreement with the DUV results, verifying that the emulation method can recreate the DUV lithography effects on the EBL process.

Figure 4.2 shows the SEM images of a device from the Bragg filter set comparing the three fabrications. We can see in the EBL image that the gratings are square-like as previously mentioned. Furthermore, we can see very similar results in the smoothed profile of the gratings in the EMU and DUV sets.

Figure 4.3 plots the main bandwidths versus the $\Delta\Delta W_2$ of the contra-DC designs. The three fabrications are compared here to evaluate the validity of the emulation when proximity effects affect the device. Once again, the EBL results are shown in blue, the DUV results are shown in purple, and the DUV-emulation (EMU) are shown in orange. From the plot, we can see that the EMU results closely match the DUV results, indicating that the emulation is also properly emulating the proximity effects.

Figure 4.4 shows the SEM images of the contra-DC throughout the three fabrications. Here, we can see that the EBL fabrication (left) yielded ideal gratings that are nearly square. The EMU device (center) shows that the gratings are reduced significantly, rounded, and a mismatch occurs between the outer and inner gratings. The DUV fabrication (right) matches up very closely with the EMU and also shows the fabrication variations predicted for the EMU device. Note that there are differences between the EMU and DUV

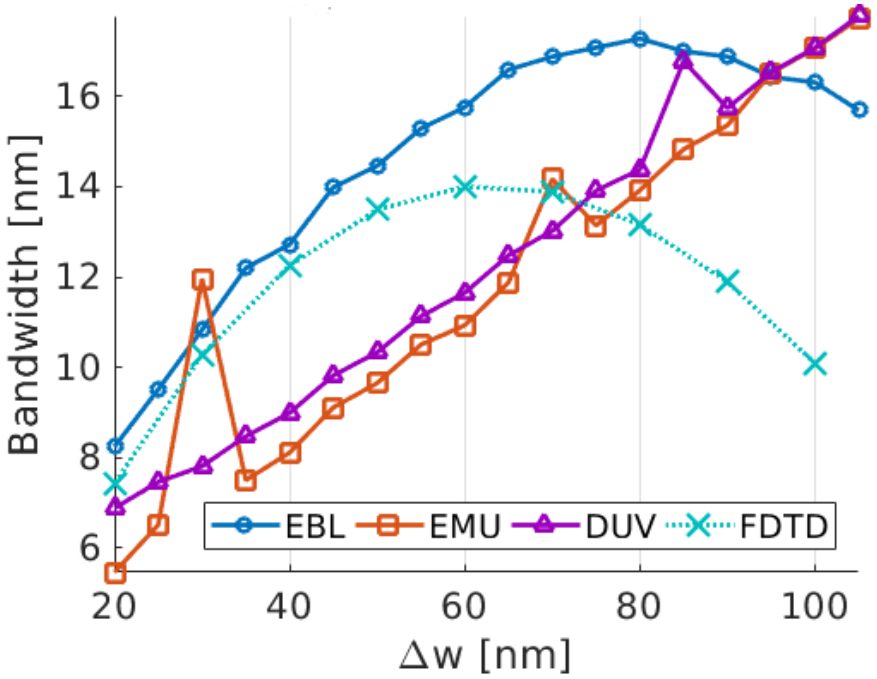


Figure 4.1: The bandwidths vs. corrugation width of a Bragg filter device comparing the difference between fabrications and the emulation of the DUV fabrication process (EMU).

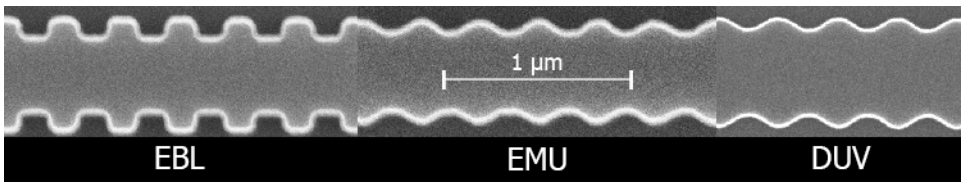


Figure 4.2: SEM images of the EBL fabrication (left), DUV-emulation (EMU) (center), and DUV fabrication (right) is shown. The EMU shows high similarity with the actual DUV fabrication. The EBL and EMU images were taken using 13,900x magnification, voltage of 15 kV, and a working distance of 6.7 mm. The DUV image was taken using 25,000x magnification, voltage of 15 kV, current of 50 pA, with secondary electron mode. The images were resized to the same scale using the pixel distance provided.

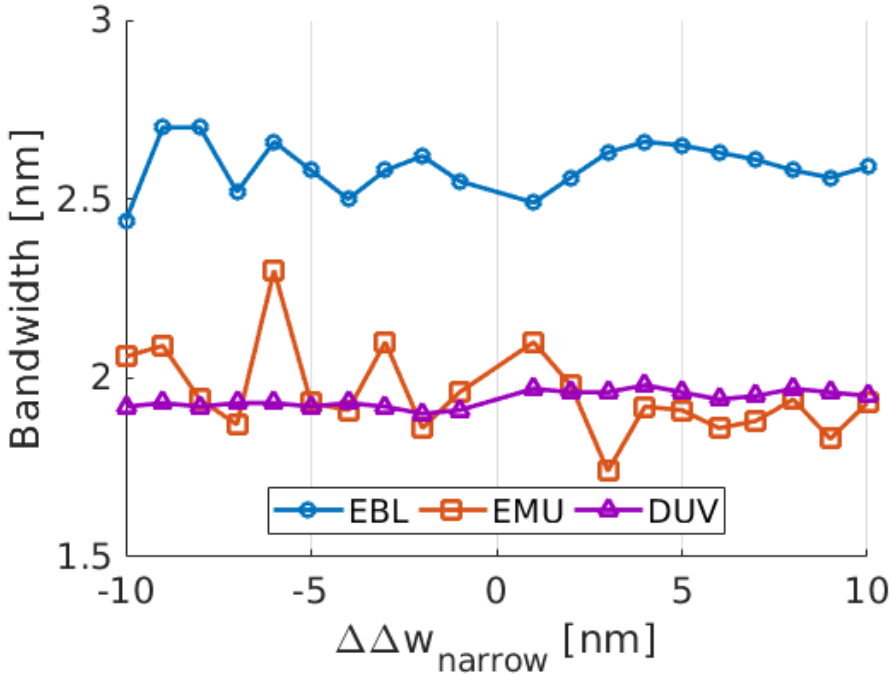


Figure 4.3: The main bandwidth versus mismatch corrugation width is plotted. The main bandwidth is expected to remain negligibly unchanged as the corrugation mismatch increases. The EBL fabrication design (blue) shows this stable trend. The DUV fabrication (purple) also shows this trend with a reduction in bandwidth due to the fabrication variations. The emulation fabrication (EMU) (orange) closely follows the DUV results, demonstrating good agreement between the emulation and the actual DUV fabrication.

devices near the inner corrugation, indicating potential for improvement.

Our comparisons show that DUV-emulation using EBL fabrication is a viable method. The method provides a substantial improvement for the rapid-prototyping process of DUV devices. Using this method, designers are able to obtain measurement data of their devices at a low cost.

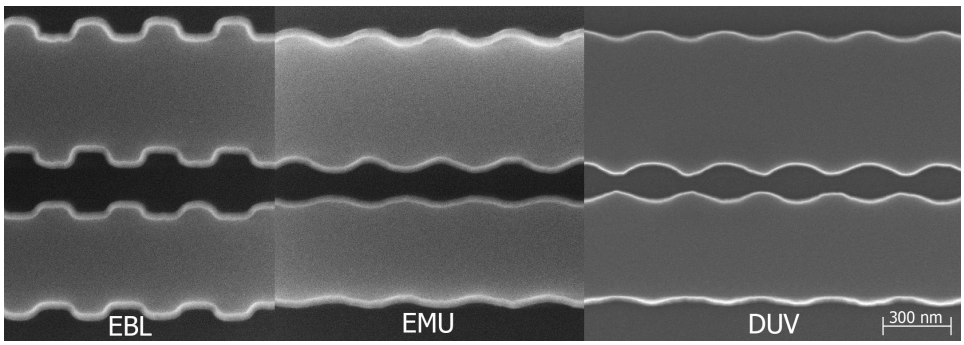


Figure 4.4: The SEM images of the three fabrications of the contra-DC devices are shown. The EBL contra-DC (left) shows balanced corrugations, and orthogonal corrugation profiles. The emulation (EMU) of the DUV-process (center) shows smoothed and reduced corrugations with mismatched corrugations. The DUV fabrication (right) is closely resembles by the EMU, demonstrating smoothed & reduced corrugations, and an obvious mismatch between the inner and outer corrugations. However the EMU still slightly differs from the DUV, specifically between the inner corrugations, and requires further investigation and improvement. The EBL and EMU SEM images are taken at a magnification of 37,720x, voltage of 15 kV, and a working distance of 6.7mm. The DUV SEM simage was taken at a magnification of 65,000x, voltage of 15 kV, current of 50 pA, using secondary electron mode. The images were adjusted to the same scale using the pixel measurement provided by the images.

4.2 Self-reflection Surpression via Mismatched Corrugations

The contra-directional coupler (contra-DC) exhibits side-bands known as "self-reflections" which are wavelengths innately supported by each individual grating waveguide in the contra-DC system. The side-bands are a limiting factor to the contra-directional coupler's capabilities as described in Section 1.1.2. Anti-reflection gratings [50] have been demonstrated with success in reducing the self-reflection and are used in many recently proposed grating devices [54][55][45].

It is speculated that the reduction of the self-reflection bandwidth can be further reduced, or perhaps even eliminated completely. During measurements of contra-DC devices fabricated using DUV, it was noticed that mismatches in corrugations ($\Delta\Delta W = \Delta W_{outer} - \Delta W_{inner}$) cause the bandwidths to change. A diagram of the definition for ΔW_{outer} and ΔW_{inner} is shown in Fig. 4.5, 3D-FDTD simulation sweeps were performed to investigate the effects of $\Delta\Delta W$. Figure 4.6 shows that the bandwidth changes with mismatched corrugations as observed experimentally. However, an interesting phenomenon in which the self-reflection bandwidth is minimized to beyond detection of the FDTD simulations (being on the orders of picometers) was illustrated. This minimization is simulated to occur when $\Delta\Delta W_2$=-10 nm for a contra-DC with parameters: Λ = 318 nm, G = 160 nm, W_1 = 560 nm, W_2 = 440 nm, ΔW_1 = 50 nm, and ΔW_2 = 30 nm. In this case, the $\Delta\Delta W$ was applied only to the smaller waveguide to reduce the self-reflection bandwidth at the lower wavelength. This is due the measurement equipment limitations only being capable of capturing the self-reflection bandwidth at the lower wavelength. Simulations of the the $\Delta\Delta W$ being applied to the larger waveguide are included in Fig. 4.7, but measurements were unable to be obtained for comparison due to equipment limitations.

The designs were fabricated using EBL and the main bandwidth and self-reflection bandwidth were measured. Figure 4.8 shows the FDTD simulated self-reflection bandwidth alongside the experimental measurement. When $\Delta\Delta W_2$ = -10 nm, the simulation and measurement are in agreement, showing a complete suppression of the self-reflection bandwidth. Figure 4.9 shows the measured bandwidth of the as-drawn layout and the DUV-emulated layout. When DUV lithography effects are added, a shift in the trend towards the right is observed, indicating that the maximum suppression exists at $\Delta\Delta W_2$ = 0 nm. The optical response showing full self-reflection suppres-

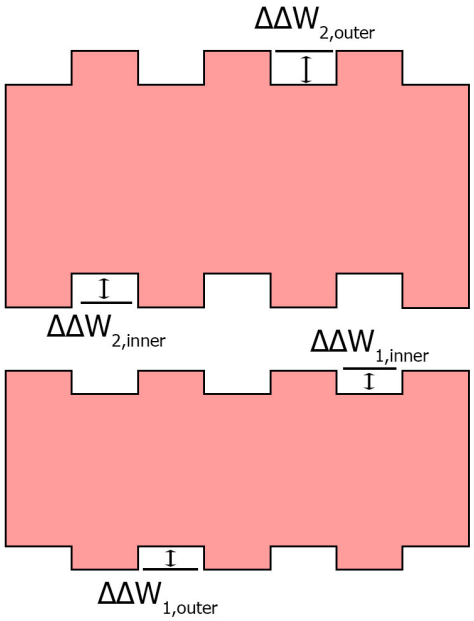


Figure 4.5: The layout with the definitions for W_{outer} and W_{inner} for the narrow waveguide (W_1) and the wide waveguide (W_2).

sion can be found in Fig. 4.11b for the $\Delta\Delta W_2$ = -10 nm, and Fig. 4.12 for its lithography emulated counterpart.

Figure 4.10 plots the main bandwidth of the FDTD simulation, the as-drawn layout, and the emulated layout. It is observed that the main bandwidth remains stable throughout the $\Delta\Delta W_2$ sweep. The addition of DUV lithography effects reduces the overall bandwidth across the devices, but the trend of a stable main bandwidth remains.

In conclusion, the experimental measurements confirm the simulation results of an optimized design in which the self-reflection can be fully suppressed. The simulations also demonstrate that the method can be used on both waveguides simultaneously to reduce the self-reflection of each waveguide with minimal losses to the main bandwidth; This remains to be confirmed experimentally. Lastly, it should be noted that the amount of $\Delta\Delta W$ suppression is dependent on the parameters chosen for the contra-DC.

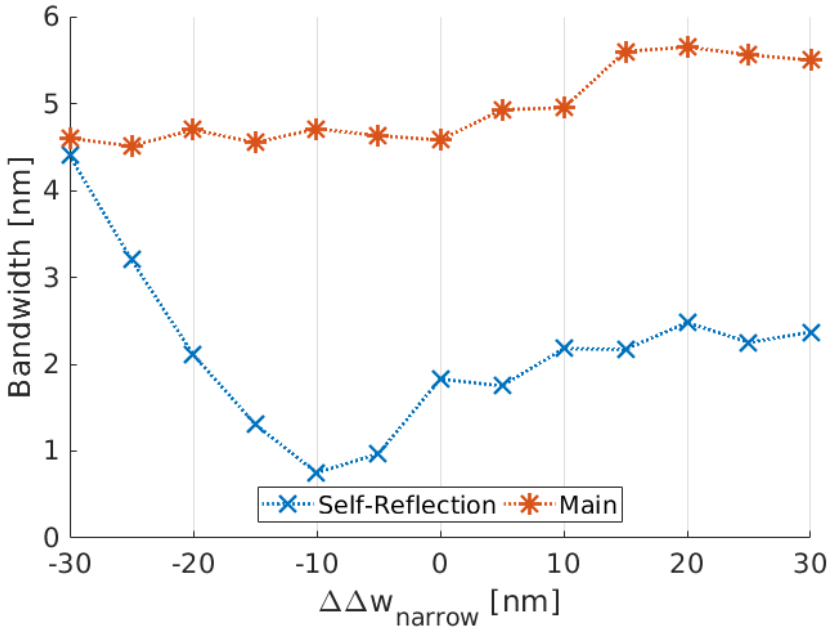


Figure 4.6: The simulated bandwidths of $\Delta\Delta W_2$ from -30 to 30 nm is depicted. The main band bandwidth (orange) shows a horizontal trend indicating minimal influence from $\Delta\Delta W_2$. The self-reflection bandwidth (blue) shows a decrease as the outer corrugations becomes smaller than the inner corrugations. A minimum is observable around $\Delta\Delta W_2$ = -10 nm.

4.3 Compensating for Lithography Effects

Using the predicted lithography effects obtained from the lithography model, we perform a redesign of CDC3. Our aim is to produce a predicted result in which the gap and the ΔWs match the intended parameters. First, we decrease the distance between the two waveguides, as we know that the lithography effects will widen gap. Next, we increase ΔW_{inner} while taking note that our changes will also effect the gap. Finally, we increase ΔW_{outer} until the predicted result for ΔW_{outer} is equal in size to the predicted ΔW_{inner}. This process is repeated until the prediction achieves our objective, i.e., the gap=185 nm and ΔW=50, 60 nm for the top and bottom waveguides, respectively.

Figure 4.13c shows the CDC3 redesign with parameters: gap=179 nm, top waveguide corrugations of ΔW_{inner}=67 nm & ΔW_{outer}=78 nm, and

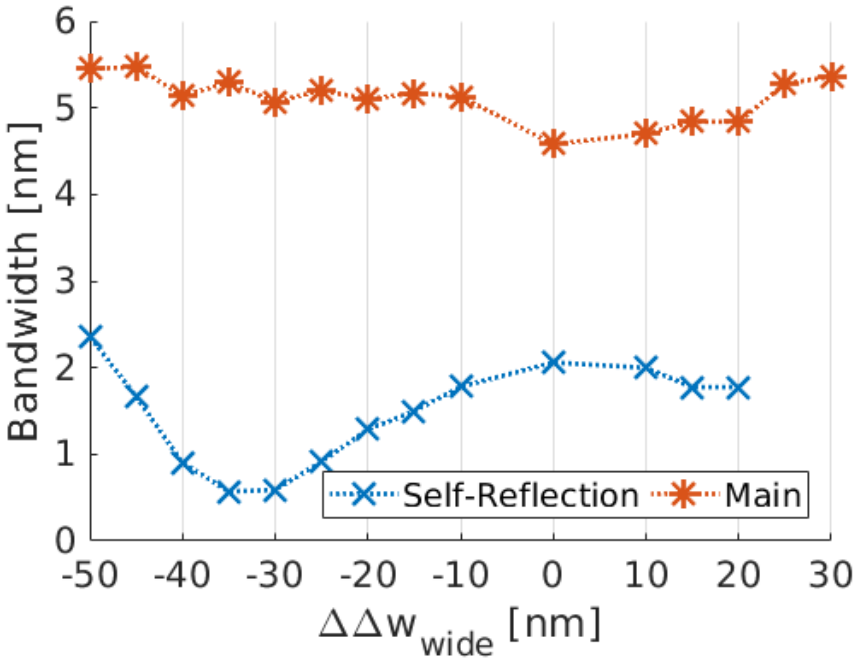


Figure 4.7: The simulated bandwidths of $\Delta\Delta W_1$ from -50 to 30 nm is depicted. The main band bandwidth (orange) shows horizontal trend. The self-reflection bandwidth (blue) shows a gradual decrease in bandwidth. A minimum bandwidth below 1 nm occurs around $\Delta\Delta W_1$ = -30 nm

bottom waveguide corrugations of ΔW_{inner}=80 nm & ΔW_{outer}=88 nm. The predicted result for this redesign shows that the gap and ΔWs will have the originally intended values, see Fig. 4.13d.

The main bandwidth response of the original device and the redesigned device are shown in Fig. 4.14a and Fig. 4.14b respectively. Comparison of the two bandwidths indicate that the bandwidth will be improved and closer to the ideal simulation when the redesign method is applied.

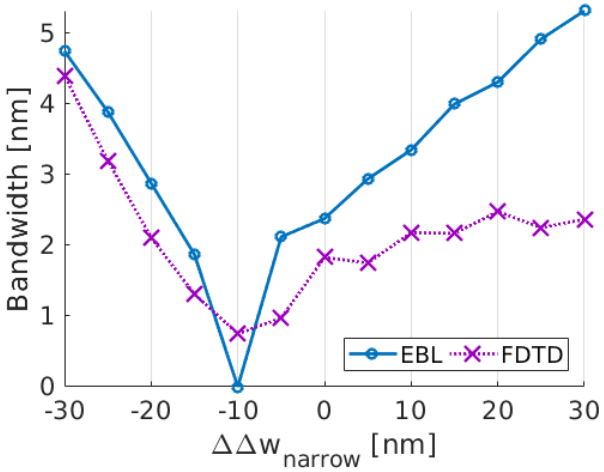


Figure 4.8: The simulated results (purple) are compared against the measured bandwidths (blue) of the devices using as-drawn layouts. The trend follows closely with the simulations, demonstrating as suppressed self-reflection when $\Delta\Delta W_2$ = -10 nm.

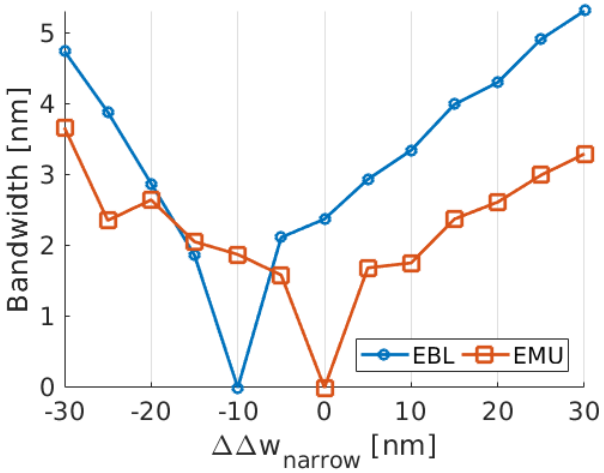


Figure 4.9: The responses of the as-drawn layout (blue) and the lithography-emulated (EMU) (orange) devices are compared. The complete suppression is visible in both measurement results. The lithography-emulated devices also show a rightwards shift.

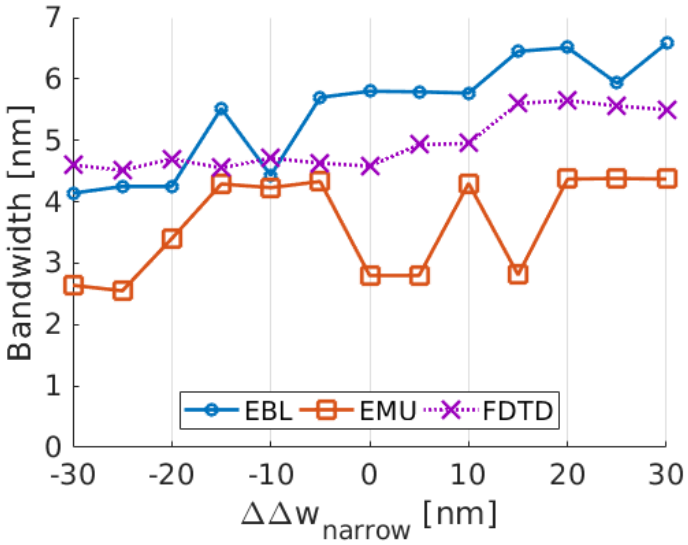
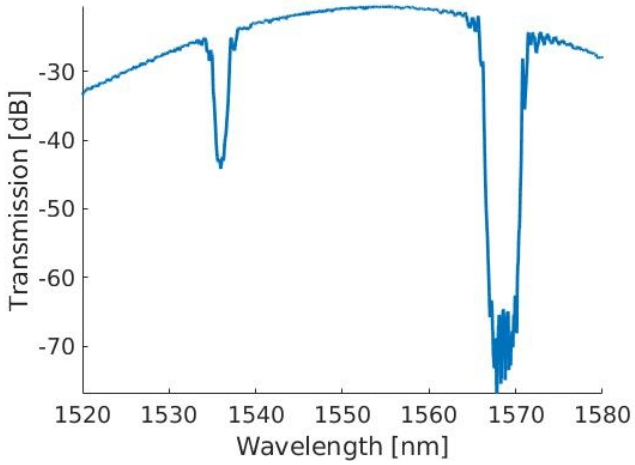
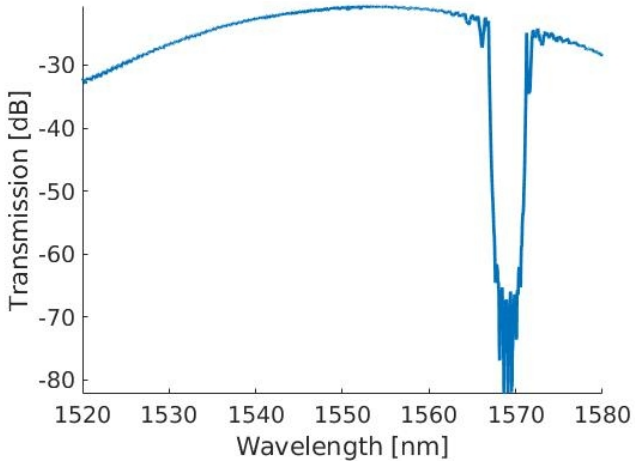


Figure 4.10: The main band bandwidths of the FDTD simulation (purple), as-drawn layout (blue), and lithography-emulated (EMU) layout (orange) are shown. The as-drawn bandwidths agree with the FDTD simulations, confirming that the main band bandwidths have not changed when using mismatched corrugations. The EMU results indicate that the main band-width will be reduced by around 2 nm when DUV-lithography effects are introduced.



(a) $\Delta\Delta W$ = 0 nm



(b) $\Delta\Delta W$ = -10 nm

Figure 4.11: The measured spectrum of the EBL fabricated corrugation mismatched contra-DC devices. The control for the experiment ($\Delta\Delta W_2$ = 0 nm) is depicted in (a) and the device demonstrating successful bandwidth suppression is depicted in (b).

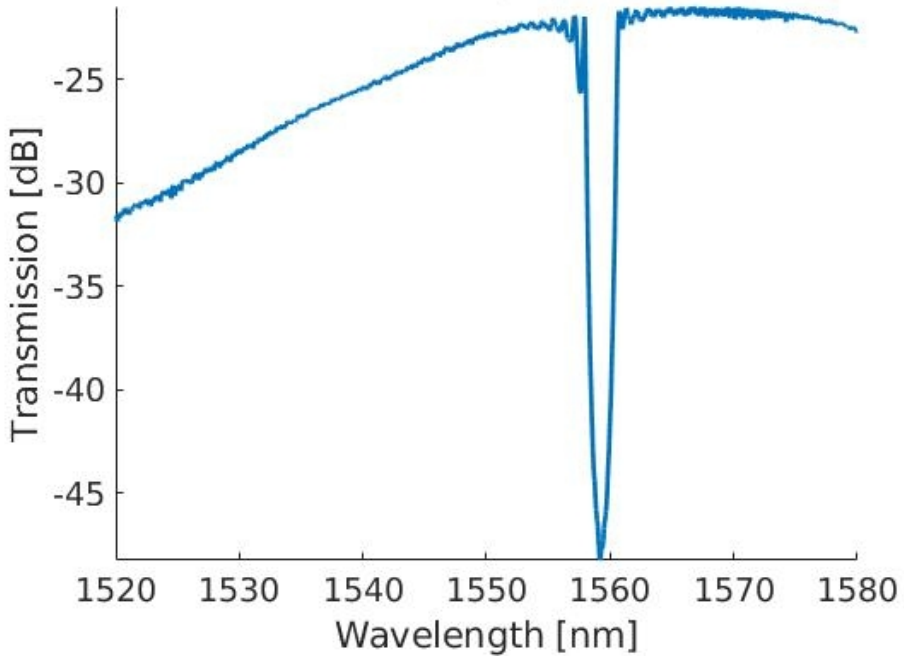
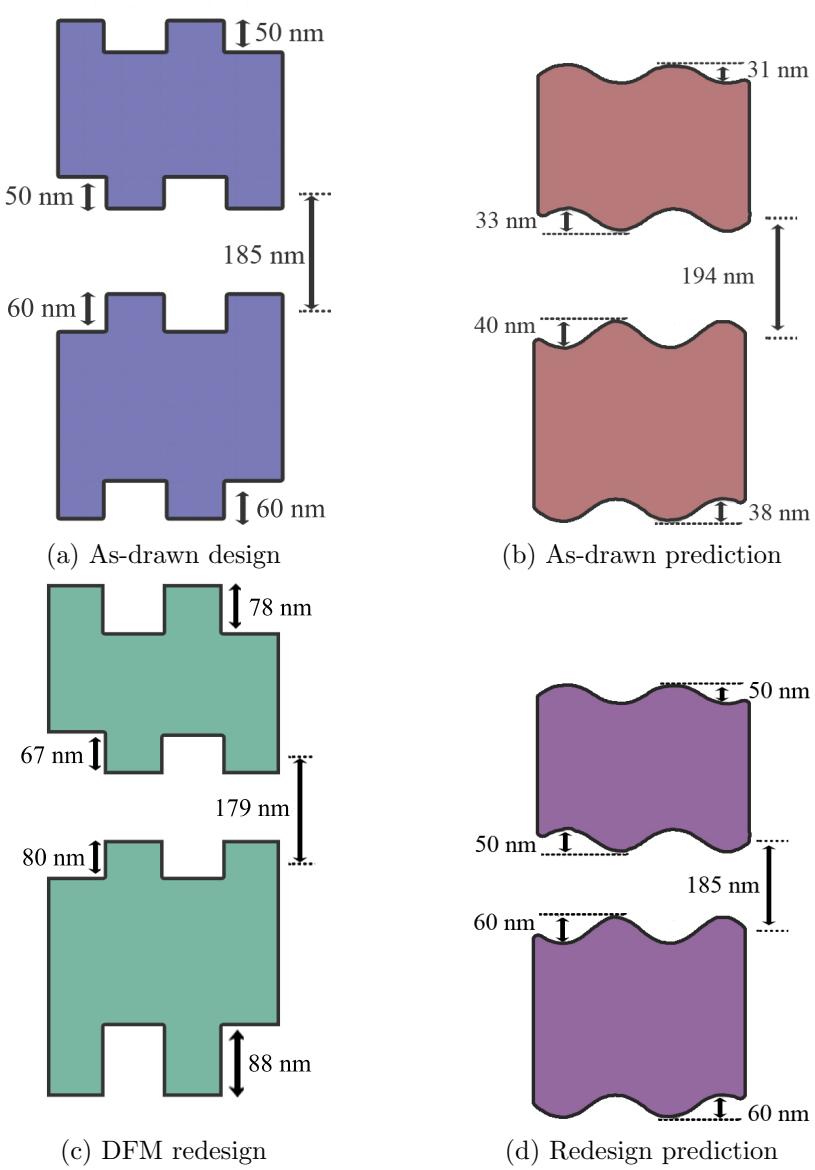


Figure 4.12: The DUV-lithography emulation (EMU) response of $\Delta\Delta W_2 = 0$ is shown. The measured response indicates that when smoothing is considered, the suppression of the self-reflection will occur with the nominal design parameters.



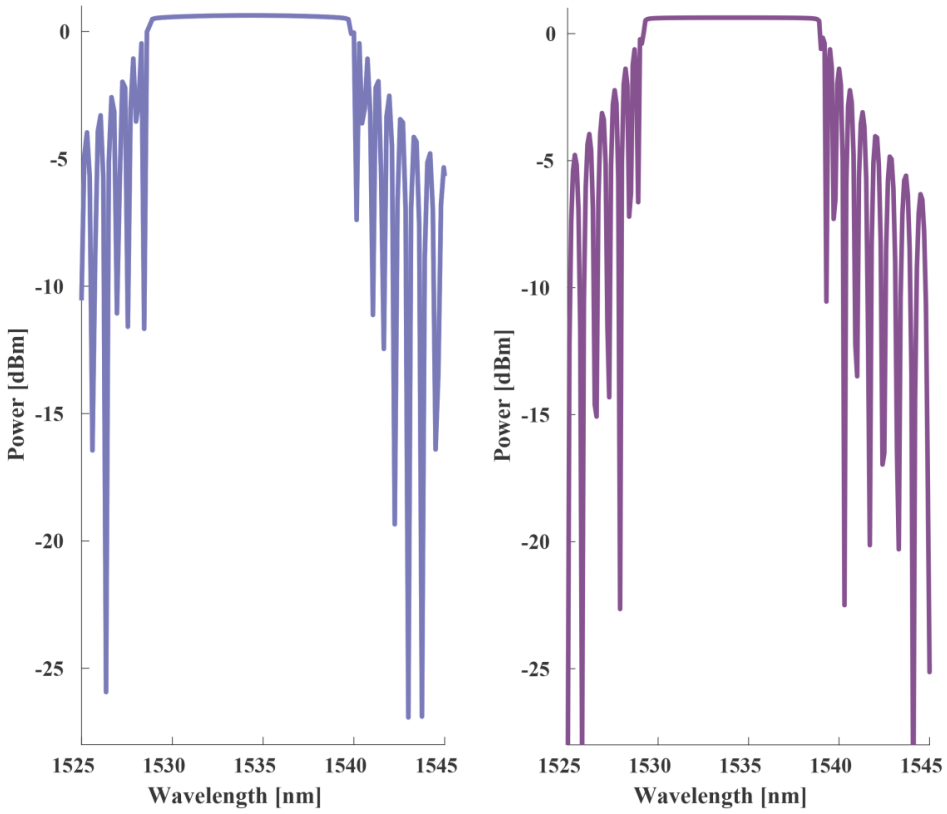
(a) As-drawn design

(b) As-drawn prediction

(c) DFM redesign

(d) Redesign prediction

Figure 4.13: (a) The as-drawn gap and ΔW parameters of CDC3 is shown. (b) A lithography prediction of the as-drawn parameters. The results show asymmetry for the ΔWs and a larger gap. (c) A redesign of CDC3 using the information obtained from (b). (d) The lithography prediction of the redesigned CDC3. The results indicate that the ΔWs and gap sizes will match the original as-drawn values.



(a) Ideal

(b) Redesign

Figure 4.14: The simulated main bandwidth response of the CDC3 ideal design (Fig. 4.13a) and redesign (Fig. 4.13d) using 3D-FDTD. The bandwidth of the ideal design is 11.5 nm and the bandwidth of the redesign is 9.8 nm. A significant improvement over the as-fabricated bandwidth of 6.4 nm (demonstrated in Fig. 3.11c) when the device undergoes a redesign to compensate for lithography effects.

Chapter 5

Summary, Conclusions, and Suggestions for Future Work

A lithography model was built from test patterns fabricated using a 193nm DUV process. The model demonstrated good agreement with experimental results and is able to predict lithography effects for any input shape. Methods to improve prototyping of DUV devices enabled by the model such as DUV-emulation and lithography compensation were demonstrated. The DUV-emulation method would provide designers with measurement data prior to investing in a DUV fabrication. The lithography compensation method is a feedback design loop allowing designers to iterate their devices to become fabrication tolerant. Both methods are cost efficient and compatible with standard simulation methods such as FDTD.

5.1 Conclusion

The results presented in this thesis demonstrated that a lithography model for a 193 nm DUV fabrication process can be built using fabricated test patterns. The lithography model's predictions are accurate in both visual comparisons to SEMs of the test patterns it was built from and optical response comparisons with a benchmark contra-DC device.

It should be noted that the lithography model presented in this thesis analyzes the lithography effects through an aerial top-down perspective. In reality, designers will find that the lithography effects are more complex as it is the 3-dimensional geometry that changing. Thus, it is crucial to consider the cross sectional shape as well, namely sidewall angles and wafer height variations.

For this thesis, a cross-sectional analysis for the benchmark contra-DC device was performed and it was determined the bandwidth response of the contra-DC device is highly resilient towards the cross-sectional lithography changes. A simplified explanation to this is that the waveguide widths used are sufficiently wide allowing the light to remain fully confined even when

sidewalls are extreme and/or the waveguide widths are at their extremes. The detailed analysis of the sidewall angles and wafer height variation can be found in Chapter 2. As such, when using the lithography model, it is important perform a separate optical analysis for the sidewall angles and thicknesses variations.

Additionally, when designing devices containing cavities, larger cavity sizes are more likely to be fabricated successfully. In a second fabrication of the same 193 nm DUV process use to build the lithography model, devices containing cavities were not fabricated properly. The devices analyzed were contra-DCs with a cavity design [26] and are shown in Fig. 5.1. Figure 5.1a shows the layout of the contra-DC which has a cavity size of 160 nm. This width is within the safe limit of the DUV fabrication. The lithography prediction, as shown in Fig. 5.1b, predicts a hole of 88 nm to be fabricated. However, as shown in Fig. 5.1c, the fabrication did not produce any cavities of the contra-DC.

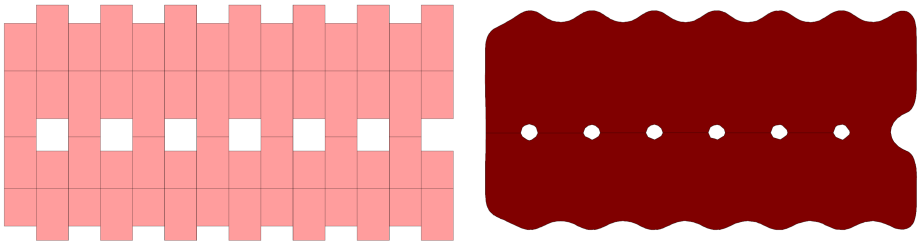
The cavity test pattern was subsequently analyzed. The layout is shown in Fig. 5.2a has a gap of 180 nm which is also within the safe limits of the fabrication. Figure 5.2b shows the fabricated test pattern on the first DUV fabrication (of which the lithography model was built from). The cavity was properly produced on this run with a size of 83 nm. Figure 5.2c shows the same pattern from the second fabrication. Here, the test pattern did not have a cavity. Further investigations with support from the foundry would be required to properly draw any conclusions.

Designers looking to use the lithography model should compensate for the model's limitations by conducting cross-sectional analysis of their devices similar to what is shown in chapter 2. For devices with cavities, including a test pattern and/or a small section of the device can provide more information of the lithography effects via SEM imaging.

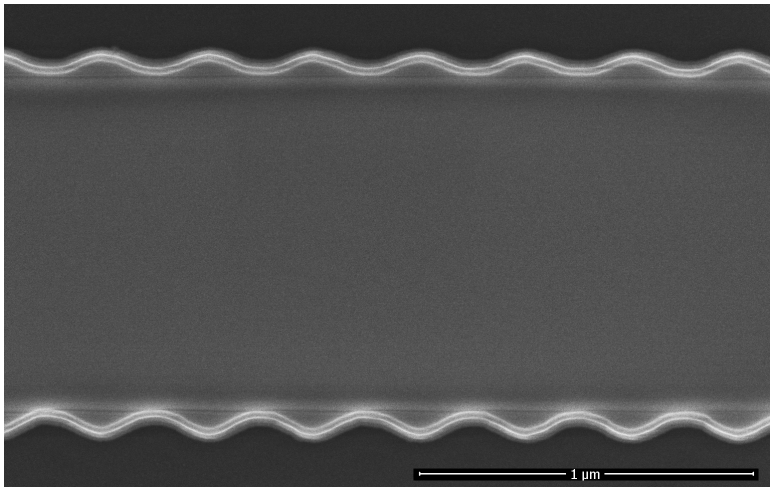
5.2 Suggestions for Future Work

The lithography model demonstrated in this thesis has potential for further improvement. The following are three suggestions of future work: 1) increase the number of data sets the model is built from, 2) automating the SEM CD extraction process, and 3) developing a 3D lithography model by combining the cross-sectional variations and the lithography model predictions. These suggestions would greatly improve the accuracy of the lithography predictions and usability of the model.

First, the amount of data provided to the model should be increased.

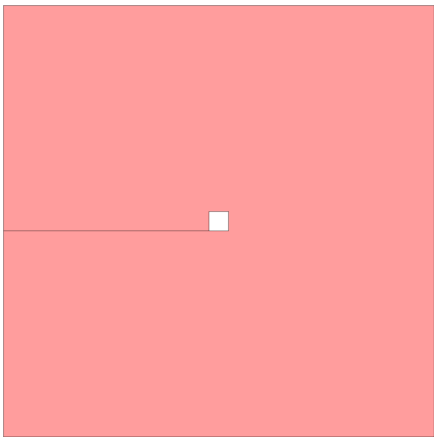


(a) GDS Schematic (b) Lithography Simulation

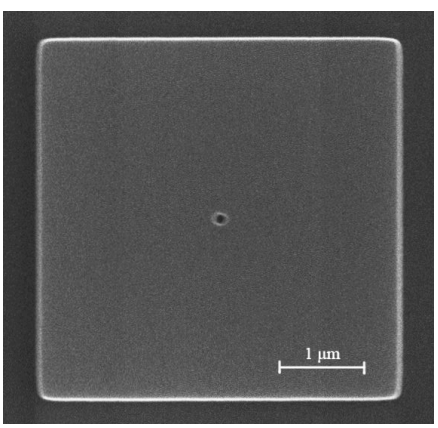


(c) SEM Image

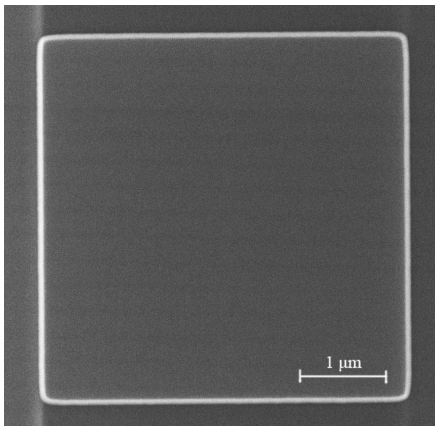
Figure 5.1: (a) The schematic of a contra-DC using a cavity design is depicted. The cavity has a size of 160 nm which is within the fabrication's guaranteed ranges. (b) A lithography simulation of the schematic showing that the cavities should be fabricated with a size of approximately 88 nm. (c) An SEM of the cavity-based contra-DC. The image was taken with 65,000x magnification, voltage of 15 kV, current of 50 pA, using secondary electron mode. The image shows that the cavities of the contra-DC were unresolved despite the schematic using conservative feature sizes and the lithography simulation indicating resolving of cavities.



(a) GDS Schematic



(b) First DUV Fabrication

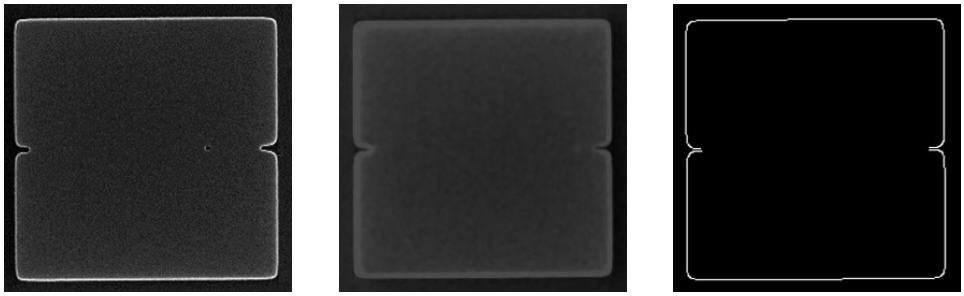


(c) Second DUV Fabrication

Figure 5.2: (a) The GDS schematic of the "inverse contact" test pattern, aimed at capturing the fabrication of cavity structures. The cavity has a size of 180 nm. (b) A SEM of the test pattern from which the lithography model was built upon. The cavity is successfully resolved at 83 nm. (c) A SEM of the test pattern from a second run of the same process in which cavity has failed to resolve.

Currently, the model is built from a single data set from one fabrication of the 193 DUV process. Additional data from test patterns could improve the accuracy of the predictions. A collaboration with the foundry would provide an even greater improvement via the sharing of process parameters. If provided with the process parameters, the model could more accurately simulate the optical and resist process, resulting in improved lithography effect predictions. It should be noted that the turn-around time for a DUV fabrication can be a limiting factor. Furthermore, for accurate CD measurements, the test patterns require an open-oxide area which might require a dedicated chip.

Second, the extraction of CD measurements is currently a very time consuming task. A method should be developed by combing image processing with edge-finding algorithms to extract the measurements automatically. This would reduce the data collection time, standardize the data collection method, and remove potential for human error. Figure 5.3 shows a mock up of the automatic extraction process. The challenge of this task occurs in image processing. Either all the SEM images would need to have similar exposure, hence allowing the software to easily determined a threshold value and find the edges of the patterns, or a dynamic thresholding algorithm can be developed to process SEMs that differ in contrast and pixel noise.



(a) SEM Image (b) Threshold Corrected (c) Edge Finding

Figure 5.3: A mock up of an automatic CD extraction procedure. The input image a) is processed by a thresholding algorithm to clean up the contrast and pixel artifacts. The output is shown in b). Finally, an edge-finding is performed to map out the shape and obtain the CD measurement, as shown in c).

Lastly, a 3D lithography method/model should be developed combining the methodologies presented in this Chapter 2 and Chapter 3. The cross-section information can be obtained using a Focused Ion Beam machine.

With the cross-section width, height, and sidewall angle known, devices can be simulated using the lithography model, and then created in 3D using the cross-section information. The realistic 3D geometry would allow accurate Finite-Difference-Time-Domain (FDTD) simulations using software such as Lumerical FDTD.

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Appendix A

Publications

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