Circuit Group Hierarchy for Mosel-Vitalic 128D14 DDR/SDR DRAM Project
(after J. Faue)

	Circuit Name	Parent Circuit	Schematic Title
1)	Z14FULL	simulation	128D14 dram FULL chip simulation
	ZMAP	none	MAP OF SPICE SENSE-AMPS/DATA PATTERN
	Z14FULL	none	FULL CHIP SPICE - 128M DDR/SDR (S14)
	ZLAINB	Z14FULL	SPICE - AIN PARAS FOR SETUP LINES
	ZLCONAB	Z14FULL	CONBLK>>RABLK PARA’S
	ZLCONIO	Z14FULL	CONBLK>>IOBLK PARA’S
	ZLRA	Z14FULL	SPICE-ARRAY SELECT (11,10) PARASITICS
	ZLRX	Z14FULL	SPICE-NORMAL ROW ADDS (0-9) PARASITICS
2)	ZBANK	simulation	32meg array BANK
	ZBANK	Z14FULL	SPICE-32M BANK (ARRAY PLUS BOT32M LOGIC)
	ZFPAR	ZBANK	F-LINE (ACROSS ARRAY) Parasitics
	ZWL	ZBANK	WORD LINE SPICE MODEL
	ZYPAR	ZBANK	Y-LINE (ACROSS ARRAY) Parasitics
	ZROW1K	ZBANK	SPICE VERSION OF 1K ROW BLOCK
	ZRDARY	ZROW1K	SPICE-RDEC ARRAY
	ZLPHIX	ZRDARY	SPICE LOADS FOR PHIX AND PXB
	ZSABAND	ZBANK	SPICE-1 SABAND (2K SAs)
	ZBL512	ZSABAND	BIT LINE PAIR (512 CELLS/BL=1024WL/BL)
	ZDPAR	ZSABAND	LOCAL D-LINE (IN Sense Amp) Parasitics
	ZSAPAR	ZSABAND	Sense Amp Band Parasitics (SPICE)
3)	ZIOBLK	simulation	Input/Output BLocK
	ZIOBLK	Z14FULL	SPICE-I/O SIDE PERIPHERY BLOCK
	ZLIRF	ZIOBLK	SPICE-IR/IF LINE PARAS
	ZLOT	ZIOBLK	SPICE-OTR and OTF LOADS
	ZLPHIZ	ZIOBLK	SPICE-PHIZ/DQS/DQSEN LOADS
4)	ZCOL	simulation	COLumn circuits
	ZCOL	Z14FULL	COLUMN CIRCUIT (2X-TOP AND BOTTOM)
	ZCPRDEC	ZCOL	COLUMN PRE-DECODERS
	ZCPRDEC2	ZCPRDEC	COLUMN PRE-DECODER LOGIC
	ZLCOL	ZCOL	COL ADDRESS PARAS (OTHER THAN CA)
	ZLC1EV	ZCOL	COL ADDRESS PARAS (C1) EVEN
	ZLC1OD	ZCOL	COL ADDRESS PARAS (C1) ODD
	ZLC32EV	ZCOL	C32 COL ADDRESS PARAS-EVEN CASE
	ZLC32OD	ZCOL	C32 COL ADDRESS PARAS-ODD LINES
	ZLCXX	ZCOL	C54/C76 COL ADDRESS PARAS (NO ODD/EVEN)
	ZLG	ZCOL	G LINE PARAS IN COL
	ZCHLF	ZCOL	COLUMN HALF-SPICE
5)	OTHER SPICE		
	ZF1K	N/A	SEMI-FULL CHIP, + 1K ROWS (SIMULATION)
	ZFBNKBOT	N/A	SEMI-FULL CHIP, + 1 BNK BOT
	ZFCOL	N/A	SEMI-FULL CHIP, + COL LVS
	ZFIO	N/A	SEMI-FULL CHIP, + COL LVS
	ZSFC	N/A	SEMI-FULL CHIP (SIMULATION)
6)	CHIP/ESD		
	D14CHIP	none	DDR/SDR - S14 TECH - FULLCHIP LVS
	CHIPCAP	D14CHIP	TOP LEVEL FILTER CAPS
	D14PER	D14CHIP	FULL PERIPHERY
	ESDIN	RABLK	INPUT PAD ESD (ADDRESS/CONTROL)
	ESDIO	DQSCON	

	Circuit Name	Parent Circuit	Schematic Title
7)	LEFT/LMISC		
	LEFT	D14PER	LEFT
	LMISC	LEFT	LEFT SIDE MISCELLANEOUS
	FIDBLK	LMISC	FUSE IDENTIFICATION BLOCK
	FIDBIT	FIDBLK	FUSE IDENTIFICATION BIT
	OSC	LMISC	SRM OSCILLATOR
	PUGEN	LMISC	PWRUP GENERATOR
	VREFBG	LMISC	VOLTAGE REFERENCE BAND GAP
	VSRLDR	RMISC	VSR LOAD CONTROL W/COUNTER
8)	RMISC		
	RMISC	D14PER	RIGHT SIDE MISCELLANEOUS
	VSRLDRR	RMISC	RIGHT SIDE - VSR LOAD CONTROL W/COUNTER
9)	COUNTER/VSR FUSE		
	COUNTER	TKCOM	COUNTER
	TMVSBIT	N/A	TEST MODE VSR BIT
	VSR FUSE	N/A	VOLTAGE SET REGISTER FUSE CIRCUITRY
10)	BANK/ARY		
	BANK	D14CHIP	FULL 32M Bank (ARRAY PLUS BOT32M LOGIC)
	ARY32M	BANK	32 MEG ARRAY-9X SABAND
	SABAND	ARY32M	SA BAND-8X HQSA
	HQSA	SABAND	H-QUAD SA AREA
	SHMUX	HQSA	SH CONTROLLED DATA MUX (1 PER QUAD)
	SA2	HQSA	SENSE AMP-TWO
11)	BNKBOT		
	BNKBOT	BANK	ROW/SA DRIVE LOGIC FOR BOTTOM OF BANK
	LNPBGEN	BNKBOT	LNB AND LPB GENERATOR
	SAEQCON	BNKBOT	EQ CONTROL FOR SENSE AMP LINES
	YDELB	BNKBOT	YDELB DRIVER (1X PER BANK)
12)	ROW1K		
	ROW1K	BNKBOT	SUPPORT CIRCUIT FOR 1K ROWS
	ASEL	ROW1K	4M ROW ARRAY SELECT
	BLKRBUF	ROW1K	ROW ADDRESS DRIVERS/PER BLOCK
	DISB	ASEL	DISABLE ROW SELECT FOR SPARE ENABLE
	DWLGEN	ROW1K	DUMMY WORDLINE GENERATOR
	FCHECK	ASEL	FCHECK TIMER GENERATOR
	FSETB	ROW1K	SPARE ROW - SET PULSE STROBE (BASED ON BAB)
	ISOEN	ROW1K	ISOEN GENERATOR
	ISOGEN	ROW1K	ISO GENERATOR
	PHIX	ROW1K	PHIX GENERATOR (0:3)
	PXSEL	ROW1K	PXSEL GENERATOR(0:3)-(PHIX FRONT END)
	SENSH	ROW1K	SEN AND SH GENERATOR
13)	RDARY/SPR		
	RDARY	ROW1K	RDEC ARRAY
	BLTWIST	RDARY	BIT LINE TWIST - EXTRA RDEX DEVICES
	RDEC	RDARY	Row Decoder
	RP32	RDARY	ROW PRE-DECODER (2 INPUT) R32(0:3)
	RP987	RDARY	ROW PRE-DECODER (3 INPUT) R987,R654
	SPRBLK	ROW1K	SPARE ROW BLOCK (1X/4 MEG)
	RFUSE	SPRBLK	ROW FUSES PER 4M ARRAY
	SPRDEC	SPRBLK	SPARE ROW DECODER (8X/4MEG)
	SPREN	SPRDEC	SPARE ROW FUSE SET ENABLE
	SPRSEL	SPRDEC	SPARE ROW ADDRESS SELECT-1 PER R0-R9

	Circuit Name	Parent Circuit	Schematic Title
14)	RABLK		
	RABLK	LEFT	ROW ADDRESS LOGIC BLOCK
	APBUF	RABLK	ADDRESS INPUT BUFFER (1X SIZE)
	APBUFC	RABLK	Y COUNTING ADDRESS INPUT BUFFER (2X SIZE)
	BABUF	RABLK	BANK ADDRESS BUFFER
	RAB1110	RABLK	SPECIAL ROW ADDRESS BUF-FOR R11/R10
	RABUF	RABLK	ROW ADDRESS BUFFER
	PDI_A	RABLK	PAD DIODES FOR DM PINS
	TINB7	RABLK	TINB DRIVER/LATCH FOR A7
	TUNAD	RABLK	TUNING CIRCUIT FOR 13 ADDRESS INPUTS
	TX10L	RABLK	TX10 LATCH
	TXDRIVER	RABLK	PROVIDE ROW ADDRESS TO TDATA GENERATOR
15)	DPATH		
	DPATH	D14PER	DATA PATH (READ/WRITE)
	CTMDAT	HMUX2	Compression Test Mode Data Generator
	DMMUX	DPATH	DATA MASK MUX POINT (X4/X8 VS. X16)
	HMUX0	DPATH	HCLK MUX C119=0 (X4/X8/16)
	HMUX13	DPATH	HCLK MUX C119=1,3 (X4/X8/16)
	HMUX2	DPATH	HCLK MUX C119=2 (X4/X8/16)
	IMUX	DPATH	READ (I-LINE) DATA SORT CIRCUIT
	WDSORT	DPATH	WRITE DATA SORT CIRCUIT
	WMUX	DPATH	WRITE DATA MUX POINT (X4/X8/16) (Ir and If)
	WMUXCON	DPATH	WMUX CONTROL LOGIC
16)	IOBLK		
	IOBLK	D14PER	I/O SIDE PERIPERHY BLOCK
	DQSBLK	IOBLK	DQS BLOCK
	DQSBUF	DQSBLK	DQS OUTPUT BUFFER
	DQSIN	DQSBLK	DQS INPUT BUFFER-SSTL
	DQSSEL	IOBLK	SELECTION FOR DQS (L ONLY USED FOR X16)
	IOCFG	IOBLK	I/O CONFIGURATION (X16/X8)
	IOMISC	IOBLK	IO MISC CKTS
	PHIOT	IOBLK	PHIOT-RISING AND FALLING-GENERATION
	PDI_D	IOBLK	IO AND DQS PAD DIODES
	SDRCONF	IOBLK	SDRVCC/LPSDR GENERATION
	STUNDIN	IOBLK	TUNING CIRCUIT FOR DATA - SDR MODE
	TUNDIN	IOBLK	TUNING CIRCUIT FOR DATA/DQS INPUTS
	VHQBIAS	IOBLK	HALF VCCQ FCAP BIAS
	QBLK	IOBLK	BLK AROUND I/O PAD
	DINBUF	QBLK	DATA INPUT BUFFER-SSTL
	DINFF	QBLK	FLIP FLOP USED FOR LATCHING INPUT DATA
	OUTBUF	QBLK	DATA OUTPUT BUFFER
	OUTDRV	OUTBUF	DATA OUTPUT DRIVER

Circuit Name	Parent Circuit	Schematic Title
17) COL		
COL	D14CHIP	COLUMN CIRCUIT (2X-TOP AND BOTTOM)
COLC8	COL	COLUMN CIRCUIT (2X-TOP AND BOTTOM)
CPRDEC	COL	COLUMN PRE-DECODERS
CPRDEC2	CPRDEC	COLUMN PRE-DECODER LOGIC
FSR	CPRDEC	R11 FUSE SELECT FOR COLUMNS
CHLF	COLC8	COLUMN HALF
CDEC	CHLF	COLUMN DECODER
COLCLK	CHLF	COLUMN CLOCK CIRCUIT
SPCDEC	CHLF	SPARE COLUMN DECODE
COLFUS1	SPCDEC	COLUMN REDUNDANCY FUSE-1 FUSE
COLFUS2	SPCDEC	COLUMN REDUNDANCY FUSE-2 FUSES
QFUSE	CHLF	COLUMN FUSES PER HQUAD
D119BLK	CHLF	DATA PAIR FOR C119
D119SEL	D119BLK	DATA PAIR SELECT FOR C119 ADDRESS
DAMP	D119BLK	DATA SENSE AMP
DDRV	D119BLK	INPUT DATA DRIVE
GMUX	D119BLK	DATA SLAVE AND OUTPUT MUX
18) CONBLK		
CONBLK	D14PER	CHIP CONtrol BLocK
ACTIVE	CONBLK	ACTIVE/READ/WRITE GENERATION
BST	CONBLK	BURST STOP DETECT
COMDEC	CONBLK	COMMAND DECODER
CONMISC	CONBLK	VOLTAGE DOWN CONVERTER PASS - CENTER CASE
CPBUF	CONBLK	CONTROL INPUT BUFFER (3X SIZE)
CYDELB	ROWCON	CONBLK - YDELB DRIVER
DPD	CONBLK	DEEP POWER DOWN (DPD) GENERATION
MRSCLK	CONBLK	MRS/TMRS/EMRS/RSDLL GENERATION
REFCLK	CONBLK	REF/SELF GENERATION
REFDEL	CONBLK	REFRESH DELAY TIMER
ROWCON	CONBLK	ROW ADDRESS MAIN CONTROL
SEAGAT	CONBLK	EXTRA TRANSISTORS (SEA OF GATES)
TKCOM	CONBLK	TKCOM
TUNC	CONBLK	TUNING CIRCUIT FOR 4 CONTROL SIGNALS
19) CLKGEN		
CLKGEN	CONBLK	CLOCK GENERATOR
CKEBUF	CLKGEN	CKE INPUT BUFFER
CKEBX	CLKGEN	CKEBX/CKEX/CKETTL/ GENERATION
CKEFF	CLKGEN	CKE FLIP-FLOP
CLKBUF	CLKGEN	CLK BUFFERING LOGIC
CLKBVREF	CLKGEN	CLKB=VREF FOR SDR AND RPAD MODE
CLKDRV	CLKGEN	DRIVER FOR LATCH CLOCKS
CLKSS	CLKGEN	SSTL CLK INPUT BUFFER
CPDLOG	CLKGEN	CPDLOG
QCLK	CLKGEN	QCLK DRIVER/ SOURCE MUX
20) POWCON		
POWCON	CONBLK	POWER CONTROL-REGULATORS/BUFFERS/HIZ
REGV	POWCON	VBLH(1.8V)/VINT(2.5V) + VPP REG ENABLE
REGSHOT	REGV	BAB ONE-SHOT FOR VBLH/VPP REGULATOR CONTROL

	Circuit Name	Parent Circuit	Schematic Title
21)	MR/SRM		
	MRBLK	CONBLK	MODE REGISTER BLOCK
	MRBIT	MRBLK	MODE REGISTER BIT (NORMAL & EXTENDED)
	MRBLDEC	MRBLK	MODE REGISTER BURST LENGTH DECODER
	MRCLDEC	MRBLK	CAS-LATENCY DECODER
	MRSRCDEC	MRBLK	SELF REFRESH CONTROL DECODER
	SRMBIT	SMRBLK	SELF REFRESH MODE BIT COUNTER
	SRMBLK	CONBLK	Self-Refresh Mode Block
22)	BNKCON		
	BNKCON	CONBLK	BANK CONTROLLER-READS/WRITES
	APSET	BNKCON	AUTO-PRECHARGE SET/CONTROL
	BAB	BNKCON	BANK ACTIVE CONTROL
	GCLK	BNKCON	GCLK GENERATION
	LREAD	BNKCON	LATCHED READ COMMAND GENERATION
	LWRITE	BNKCON	LATCHED WRITE COMMAND GENERATION
	PREDEC	BNKCON	BANK PRECHARGE COMMAND GENERATION
	SW	BNKCON	SHIFTED WRITE GENERATION
	YRGCLK	BNKCON	YR/GCLKB GENERATION
	YCLKW	BNKCON	YCLK-WRITE GENERATION
23)	BCCON		
	BCCON	CONBLK	Burst Count CONtrol
	BCSTATE	BCCON	Burst Counter STATE counter
	BCSBIT	BCSTATE	Burst Counter State counter BIT
	BCCLK	BCCON	Burst Counter CLocK
	BCEND	BCCON	Burst Counter END of count
	DDRCO	BCCON	C0 (ODD-EVEN) LATCH/BUFFER
	KBCEND	BCCON	SHIFTED BURST END DETECT
24)	CABLK		
	CABLK	CONBLK	COL. ADDR. BUFFER FOR TOP OR BOTTOM ARRAY
	ALRAWB	CABLK	ANY LATCHED READ/ANY WRITE BAR
	BCBIT	C21BLK	Burst Counter Register BIT-FOR C0 AND C1
	BCTGL	CABLK	Burst Counter ToGgLe page 2
	CAEBAE	CABLK	COLUMN ADDRESS BUFFER ADDRESS ENABLE
	CALAT	CABLK	COLUMN ADDRESS BUFFER (NON-COUNTING)
	CALAT0	CABLK	COLUMN ADDRESS BUFFER - SDR C0
	CALAT119	CABLK	COLUMN ADDRESS BUFFER - C11 & C9
	C119PD	CABUF	C11 & C9 COLUMN PREDECODER (1X)
	CNTCON	CABLK	INCB/CNTLD GENERATION
	TKC1	CABLK	SHIFTED C1 FOR COMPRESSION
	WP2	CABLK	WRITE COMMAND PULSE-DELAYED 2 CYCLES
	C21BLK	CABLK	CIRCUITS FOR C2 & C1 (COUNTING ADDR)
	BCTGL21	C21BLK	Burst Counter ToGgLe page 1
	CALAT21	C21BLK	A2,A1 COLUMN ADDRESS BUFFER (COUNTING)
	CBUF21LD	CALAT21	COLUMN COUNT LOGIC
25)	DQSCON		
	DQSCON	CONBLK	QFC/DQS/MASK/X16-X8-X4 CONTROL
	DQSEN	DQSCON	DQS- WRITE CONTROL
	GLW	DQSCON	GLOBAL LATCHED WRITE-DQS WRITE CONTROL
	PDI_DM	DQSCON	PAD DIODE FOR DM PINS
	STUNDM	DQSCON	SDR TUNING CIRCUIT FOR 2 DATA MASK SIG.
	TMVM	DSQCON	VOLTAGE MEASURING CIRCUIT/VDM PAD
	VMSELX	TMVM	SELECT CIRCUIT FOR V-MEAS MODES
	TUNDM	DSQCON	TIMING CIRCUIT FOR 2 DATA MASK SIGNLALS

Circuit Name	Parent Circuit	Schematic Title
26) DCON		
DCON	CONBLK	DATA CONTROLLER (H/I/X CLKS & WEN)
FKOT	DCON	FAKE OT CLK (FKOT)/DATA SORT CLK (DSCLK)
HCLK	DCON	HCLK<0:3>/TCLK GENERATION
ICLK	DCON	ICLK R AND F GENERATION
S0SHFT	DCON	S0 (ODD-EVEN) SHIFTER
S119	DCON	C11 C9 SHIFTER (4X) <0:3>
SHIFTR	DCON	SHIFT READ CONTROL
WDCON	DCON	WRITE DATA CONTOL (C0 SORTING)
WEN119	DCON	WEN119<0:3> GENERATION
XCLKF	DCON	XCLKF GENERATION
27) VPL		
VHBLH	VPL	Voltage Half vBLH
VHREF	VHBLH	Voltage HALF vblh REFerence
VHALF	VHBLH	Voltage HALF vblh
VCMP	VHBLH	Voltage Current Mirror P-type
ZVHBLH	NONE	Spice Voltage Half vBLH
ZVHCNET	VHBLH	VHblh Capacitor NETwork
28) VBB/NWL		
VBBGEN	VBB	VBB GENerator
VBBCLK	VBBGEN	VBB Pump Clocks
VBBPUMP	VBBGEN	Pump for Vbb Generator
VNWLGEN	LMISC	VNWL GENerator
VNREF	VNWLGEN	Voltage Negative REFerence
VNREG	VNWLGEN	REGULATOR FOR NEGATIVE VOLTAGE GENERATOR
VNOSC	VNWLGEN	Negative Voltage generator OSCillator
VNWLCLK	VNWLGEN	VNWLL PUMP CLOCK
VNWLPUMP	VNWLGEN	Pump for VNWLL Generator
ZPSMA	N/A	SPICE POWER SUPPLIES FOR MEMORY ARRAY
ZVBBCNET	ZPSMA	SPICE VBB CAPACITOR NETWORK
29) VPP		
VPP	LMISC	Voltage Positive Pump
VPCKDEC	VPPCLK	Voltage Positive Pump Clock Decode
VPPDLY	VPPCLK	Voltage Positive Pump DeLaY
VPPREG	VPP	Voltage Positive Pump REGulator
VPPUMP	VPP	Voltage Positive PUMP
VPPCLK	VPP	Voltage Positive Pump CLocK
VPPCLK2	VPPCLK	Voltage Positive Pump CLocK #2
30) VDC		
VDC	LMISC	VCCI/VCC VOLTAGE DOWN CONVERTERS
COUNTER	REFRATLD	COUNTER
REFRATLD	VDC	REF/RAT LOAD CONTROL W/COUNTER
TMVSBIT	REFRATLD	TEST MODE VSR BIT
VBLHLD	VDC	VBLH LOAD CONTROL W/COUNTER
VBLHTRM	VDC	VBLH TRIM
VDCA	VDC	ACTIVE VINT REG
VDCB	VDC	STANDBY VINT/VBLH REG
VDCRAT	VDC	VDC RATIO CIRCUIT
VINTLD	VDC	VINT LOAD CONTROL W/COUNTER
VINTTRM	VDC	VINT TRIM
VREF	VDC	VREF GENERATOR

Circuit Name	Parent Circuit	Schematic Title
31) DLL		
DLL	LMISC	Delay Locked Loop
CLKOFF	DLL	DLL CLOCK OFF
DLLR2	DLL	DLL RESET2
FDEL	DLL	Fixed Delay Line
FSLAT	DLL	FAST/SLOW signal latch
HVDEL	DLL	ONE-HALF Voltage Controlled Delay LINE
PD	DLL	Phase Detector
VCON	DLL	Delay Voltage generator (DLL)
VDEL	HVDEL	Voltage Controlled Delay Element
32) TMBLK		
D14TREG	N/A	INSTRUCTIONS FOR SETTING TEST MODE REGISTERS
TMBLK	CONBLK	COMPLETE TESTMODE
TINDRV	TMBLK	TIN DRIVERS <7,10:12>
TKACT	TMBLK	TESTMODE - ACTIVE, XINC, AND BKXINC
TKCON	TMBLK	TEST CLOCK CONTROL
TKFS	TMBLK	TEST MODE RESET - FUSE ID SET/SHIFT
TKRES	TMBLK	TEST MODE RESET - X,Y,BKC,ALL
TKYINCB	TMBLK	TEST MODE Y AND BANK - COL INCREMENT CONTROL
TMBIT	TMBLK	TEST MODE BIT
TMINVREV	TMBLK	TMINV/TMXREV/TMYREV SELECT
TMRPAD	TMBLK	GENERATE TMRPAD
TMRSCLK	TMBLK	TMRS GENERATION
TMSAOFB	TMBLK	TEST MODE - SENSE AMP OFF BAR (VPP LEVELS)
33) TDATA		
TDATA	TMBLK	TEST MODE DATA
DSCRAM	TDATA	TEST MODE SCRAMBLE
EXOR2	TDATA	2 INPUT EXOR
EXOR3	DSCRAM	3 INPUT EXOR
MUX1	TDATA	2 TO 1 MUX - TRANSFER
MUX2	TDATA	2 TO 1 MUX - TRANSFER WITH DECODER
TDBIT	TDATA	TDATA - BIT

Mosel-Vitac 128Meg DDR DRAM Circuit Hierarchy

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D14CHIP--|--BANK----|--ARY32M---|--SABAND---|--HQSA--------|--SA2
         |          |                                     |--SHMUX
         |          |
         |          |--BNKBOT---|--LNPBGEN
         |          |           |--ROW1K----|--ASEL--------|--DISB
         |                      |           |              |--FCHECK
         |                      |           |--BLKRBUF
         |                      |           |--DWLGEN
         |                      |           |--FSETB
         |                      |           |--ISOEN
         |                      |           |--ISOGEN
         |                      |           |--PHIX
         |                      |           |--PXSEL
         |                      |           |--RDARY-------|--BLTWST
         |                      |           |              |--RDEC
         |                      |           |              |--RP32
         |                      |           |              |--RP987
         |                      |           |
         |                      |           |--SENSH
         |                      |           |--SPRBLK------|--RFUSE
         |                      |                          |--SPRDEC---|--SPREN
         |                      |                                      |--SPRSEL
         |                      |--LNPBGEN
         |                      |--SAEQCON
         |                      |--YDELB
         |
         |--CHIPCAP
         |--COL-----|--COLC8----|--CHLF-----|--CDEC
         |          |                       |--COLCLK
         |          |                       |--D119BLK-----|--D119SEL
         |          |                       |              |--DAMP
         |          |                       |              |--DDRV
         |          |                       |              |--GMUX
         |          |                       |
         |          |                       |--QFUSE
         |          |                       |--SPCDEC------|--COLFUS1
         |          |                                      |--COLFUS2
         |          |
         |          |--CPRDEC---|--CPRDEC2
         |                      |--FSR
         |
         |--D14PER--|--CONBLK---|--ACTIVE
         |          |           |--BCCON----|--BCCLK
         |          |           |           |--BCEND
         |          |           |           |--BCSTATE-----|--BCSBIT
         |          |           |           |--DDRC0
         |          |           |           |--KBLEND
         |          |           |
         |          |           |--BNKCON---|--APSET
         |          |           |           |--BAB
         |          |           |           |--GCLK
         |          |           |           |--LREAD
         |          |           |           |--LWRITE
         |          |           |           |--PREDEC
         |          |           |           |--SW
         |          |           |           |--YCLKW
         |          |           |           |--YRGCLK
         |          |           |--BST
         |          |           |--CABLK----|--ALRAWB
         |          |           |           |--BCBIT
         |          |           |           |--CAEBAE
         |          |           |           |--CALAT
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D14CHIP--|--D14PER--|--CONBLK---|--CABLK----|--CALAT0
         |           |           |           |--CALAT119
         |           |           |           |--C119PD--|--BCBIT
         |           |           |           |--CNTCON
         |           |           |           |--C21BLK------|--BCBIT
         |           |           |           |              |--BCTGL
         |           |           |           |              |--CALAT21--|--CBUF21LD
         |           |           |           |--TKC1
         |           |           |           |--WP2
         |           |           |
         |           |           |--CLKGEN---|--CKEBUF
         |           |           |           |--CKEBX
         |           |           |           |--CKEFF
         |           |           |           |--CLKBUF
         |           |           |           |--CLKBVREF
         |           |           |           |--CLKDRV
         |           |           |           |--CLKSS
         |           |           |           |--CPDLOG
         |           |           |           |--QCLK
         |           |           |           |--VMSELX
         |           |           |
         |           |           |--COMDEC
         |           |           |--CONMISC
         |           |           |--CPBUF
         |           |           |--DPD
         |           |           |--DQSCON---|--DINBUF
         |           |           |           |--DINFF
         |           |           |           |--DQSEN
         |           |           |           |--ESDIO
         |           |           |           |--GLW
         |           |           |           |--PDI_DM
         |           |           |           |--STUNDM
         |           |           |           |--TMVM--------|--VMSELX
         |           |           |           |--TUNDM
         |           |           |
         |           |           |--ESDIN
         |           |           |--MRBLK----|--MRBIT
         |           |           |           |--MRBLDEC
         |           |           |           |--MRCLDEC
         |           |           |           |--MRSRCDEC
         |           |           |
         |           |           |--MRSCLK
         |           |           |--POWCON---|--REGV--------|--REGSHOT
         |           |           |
         |           |           |--REFCLK
         |           |           |--REFDEL
         |           |           |--ROWCON---|--CYDELB
         |           |           |
         |           |           |--SEAGAT
         |           |           |--SRMBLK---|--SRMBIT
         |           |           |
         |           |           |--TKCOM
         |           |           |--TKCON----|--COUNTER
         |           |           |
         |           |           |--TMBLK----|---TDATA------|--DSCRAM---|EXOR3
         |           |           |           |              |--EXOR2
         |           |           |           |              |--EXOR3
         |           |           |           |              |--MUX1
         |           |           |           |              |--MUX2
         |           |           |           |              |--TDBIT
         |           |           |           |--TINDRV
         |           |           |           |--TKACT
         |           |           |           |--TKCON
         |           |           |           |--TKFS
         |           |           |           |--TKRES
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D14CHIP--|--D14PER--|--CONBLK---|--TMBLK----|--TKYINCB
         |          |           |           |--TMBIT
         |          |           |           |--TMINVREV
         |          |           |           |--TMRPAD
         |          |           |           |--TMRSCLK
         |          |           |           |--TMAOFB
         |          |           |--TUNC
         |          |
         |          |--DCON---- |--FKOT
         |          |           |--HCLK
         |          |           |--ICLK
         |          |           |--S0SHFT
         |          |           |--S119
         |          |           |--SHIFTR
         |          |           |--WDCON
         |          |           |--WEN119
         |          |           |--XCLKF
         |          |
         |          | --DPATH---|--DMMUX
         |          |           |--HMUX0
         |          |           |--HMUX13
         |          |           |--HMUX2----|--CTMDAT------|--EXOR2
         |          |           |--IMUX
         |          |           |--WDSORT
         |          |           |--WMUX
         |          |           |--WMUXCON
         |          |
         |          |--IOBLK--- |--DQSBLK---|--ESDIO
         |          |           |           |--DQSBUF------|--OUTDRV
         |          |           |           |--DQSIN
         |          |           |
         |          |           |--DQSSEL
         |          |           |--IOCFG
         |          |           |--IOMISC
         |          |           |--PDI_D
         |          |           |--PHIOT
         |          |           |--QBLK-----|--DINBUF
         |          |           |           |--DINFF
         |          |           |           |--ESDIO
         |          |           |           |--OUTBUF------|--OUTDRV
         |          |           |--SDRCONF
         |          |           |--STUNDIN
         |          |           |--TUNDIN
         |          |           |--VHQBIAS
         |          |           |
         |          |           |
         |          |--LEFT---- |--LMISC----|--DLL---------|--CLKOFF
         |          |           |           |              |--DLLR2
         |          |           |           |              |--FDEL
         |          |           |           |              |--FSLAT
         |          |           |           |              |--HVDEL-----|--VDEL
         |          |           |           |              |--PD
         |          |           |           |              |--VCON
         |          |           |           |--FIDBLK------|--FIDBIT
         |          |           |           |--OSC
         |          |           |           |--PUGEN
         |          |           |           |--VDC---------|--DLLDPD
         |          |           |           |              |--REFRATLD--|COUNTER
         |          |           |           |              |            |TMVSBIT
         |          |           |           |              |
         |          |           |           |              |--VBLHLD----|COUNTER
         |          |           |           |              |            |TMVSBIT
         |          |           |           |              |
         |          |           |           |              |--VBLHTRM
         |          |           |           |              |--VDCA
         |          |           |           |              |--VDCB
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D14CHIP--|--D14PER--|--LEFT---- |--LMISC----|--VDC---------|--VDCRAT
         |           |           |           |              |--VINTLD----|COUNTER
         |           |           |           |              |            |TMVBIT
         |           |           |           |              |
         |           |           |           |              |--VINTRM
         |           |           |           |              |--VREF
         |           |           |           |              |--VSRFUSE
         |           |           |           |
         |           |           |           |--VHBLH-------|--VCMP
         |           |           |           |              |--VHALF
         |           |           |           |              |--VHREF
         |           |           |           |
         |           |           |           |--VNWLGEN-----|--VNOSC
         |           |           |           |              |--VNREF
         |           |           |           |              |--VNREG
         |           |           |           |              |--VNWLCLK
         |           |           |           |              |--VSRFUSE
         |           |           |           |
         |           |           |           |--VPP---------|--VPPCLK----|--VPCKDEC
         |           |           |           |              |            |--VPPCLK2
         |           |           |           |              |            |--VPPDLY
         |           |           |           |              |--VPPREG
         |           |           |           |              |--VPPUMP
         |           |           |           |--VREFBG
         |           |           |           |--VSRLDR------|--COUNTER
         |           |           |           |              |--TMVSBIT
         |           |           |           |
         |           |           |
         |           |           |--RABLK----|--APBUF
         |           |                       |--APBUFC
         |           |                       |--BABUF
         |           |                       |--ESDIN
         |           |                       |--RAB1110
         |           |                       |--RABUF
         |           |                       |--PDI_A
         |           |                       |--TINB7
         |           |                       |--TUNAD
         |           |                       |--TX10L
         |           |                       |--TXDRIVER
         |           |
         |           |--RMISC----|--VBBGEN---|--VBBCLK
         |           |           |           |--VBBPUMP
         |           |           |           |--VNOSC
         |           |           |           |--VNREF
         |           |           |           |--VNREG
         |           |           |           |--VSRFUSE
         |           |           |
         |           |           |--VPP------|--VPPCLK------|--VPCKDEC
         |           |           |           |              |--VPPCLK2
         |           |           |           |              |--VPPDLY
         |           |           |           |--VPPREG
         |           |           |           |--VPPUMP
         |           |           |           |--VSRFUSE
         |           |           |
         |           |           |--VSRLDRR--|--COUNTER
         |           |           |           |--TMVSBIT
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Circuit Name Index 128M DDR

Circuit Name	Parent Circuit	Book Section	Schematic Title
-A-			
ACTIVE	CONBLK	CONBLK	ACTIVE/READ/WRITE GENERATION
ALRAWB	CABLK	CABLK	ANY LATCHED READ/ANY WRITE BAR
APBUF	RABLK	RABLK	ADDRESS INPUT BUFFER (1X SIZE)
APBUFC	RABLK	RABLK	Y COUNTING ADDRESS INPUT BUFFER (2X SIZE)
APSET	BNKCON	BNKCON	AUTO-PRECHARGE SET/CONTROL
ARY32M	BANK	BANK/ARY	32 MEG ARRAY-9X SABAND
ASEL	ROW1K	ROW1K	ROW ARRAY SELECT
-B-			
BAB	BNKCON	BNKCON	BANK ACTIVE CONTROL
BABUF	RABLK	RABLK	BANK ADDRESS BUFFER
BANK	D14CHIP	CHIP/ESD	FULL 32M Bank (ARRAY PLUS BOT32M LOGIC)
BCBIT	C21BLK	CABLK	Burst Counter Register BIT-FOR C0 AND C1
BCCLK	BCCON	BCCON	Burst Counter CLocK
BCCON	CONBLK	CONBLK	Burst Count CONtrol
BCEND	BCCON	BCCON	Burst Counter END of count
BCSBIT	BCSTATE	BCCON	Burst Counter State counter BIT
BCSTATE	BCCON	BCCON	Burst Counter STATE counter
BCTGL	CABLK	CABLK	Burst Counter ToGgLe page 2
BCTGL21	C21BLK	CABLK	Burst Counter ToGgLe page 1
BLKRBUF	ROW1K	ROW1K	ROW ADDRESS DRIVERS/PER BLOCK
BLTWST	RDARY	RDARY	BIT LINE TWIST - EXTRA RDEC DEVICES
BNKBOT	BANK	BANK/ARY	ROW/SA DRIVE LOGIC FOR BOTTOM OF BANK
BNKCON	CONBLK	CONBLK	BANK CONTROLLER-READS/WRITES
BST	CONBLK	CONBLK	BURST STOP DETECT
-C-			
C119PD	CABLK	CABLK	C11 & C9 COLUMN PREDECODER (1X)
C21BLK	CABLK	CABLK	CIRCUITS FOR C2 & C1 (COUNTING ADDR)
CABLK	CONBLK	CONBLK	COL. ADDR. BUFFER FOR TOP OR BOTTOM ARRAY
CAEBAE	CABLK	CABLK	COLUMN ADDRESS BUFFER ADDRESS ENABLE
CALAT	C21BLK	CABLK	COLUMN ADDRESS BUFFER (NON-COUNTING)
CALAT0	C21BLK	CABLK	COLUMN ADDRESS BUFFER - SDR C0
CALAT119	C21BLK	CABLK	COLUMN ADDRESS BUFFER - C11 & C9
CALAT21	C21BLK	CABLK	A2,A1 COLUMN ADDRESS BUFFER (COUNTING)
CBUF21LD	CALAT21	CABLK	COLUMN COUNT LOGIC
CDEC	CHLF	COL	COLUMN DECODER
CHIPCAP	D14CHIP	CHIP/ESD	TOP LEVEL FILTER CAPS
CHLF	COLC8	COL	COLUMN HALF
CKEBUF	CLKGEN	CLKGEN	CKE INPUT BUFFER
CKEBX	CLKGEN	CONBLK	CKEBX/CKEX/CKETTL GENERATION
CKEFF	CLKGEN	CLKGEN	CKE FLIP-FLOP
CLKBUF	CLKGEN	CLKGEN	CLK BUFFERING LOGIC
CLKBVREF	CLKGEN	CLKGEN	CLKB=VREF FOR SDR AND RPAD MODE
CLKDRV	CLKGEN	CLKGEN	DRIVER FOR LATCH CLOCKS
CLKGEN	CONBLK	CONBLK	CLOCK GENERATOR
CLKOFF	DLL	DLL	DLL CLOCK OFF
CLKSS	CLKGEN	CLKGEN	SSTL CLK INPUT BUFFER
CNTCON	CABLK	CABLK	INCB/CNTLD GENERATION
COL	D14CHIP	CHIP/ESD	COLUMN CIRCUIT (2X-TOP AND BOTTOM)
COLC8	COL	COL	COLUMN CIRCUIT (2X-TOP AND BOTTOM)
COLCLK	CHLF	COL	COLUMN CLOCK CIRCUIT
COLFUS1	SPCDEC	COL	COLUMN REDUNDANCY FUSE-1 FUSE
COLFUS2	SPCDEC	COL	COLUMN REDUNDANCY FUSE-2 FUSES
COMDEC	CONBLK	CONBLK	COMMAND DECODER
CONBLK	D14PER	CHIP/ESD	CHIP CONtrol BLocK
CONMISC	CONBLK	CONBLK	VOLTAGE DOWN CONVERTER PASS - CENTER CASE
COUNTER	TKCON	CONBLK	COUNTER

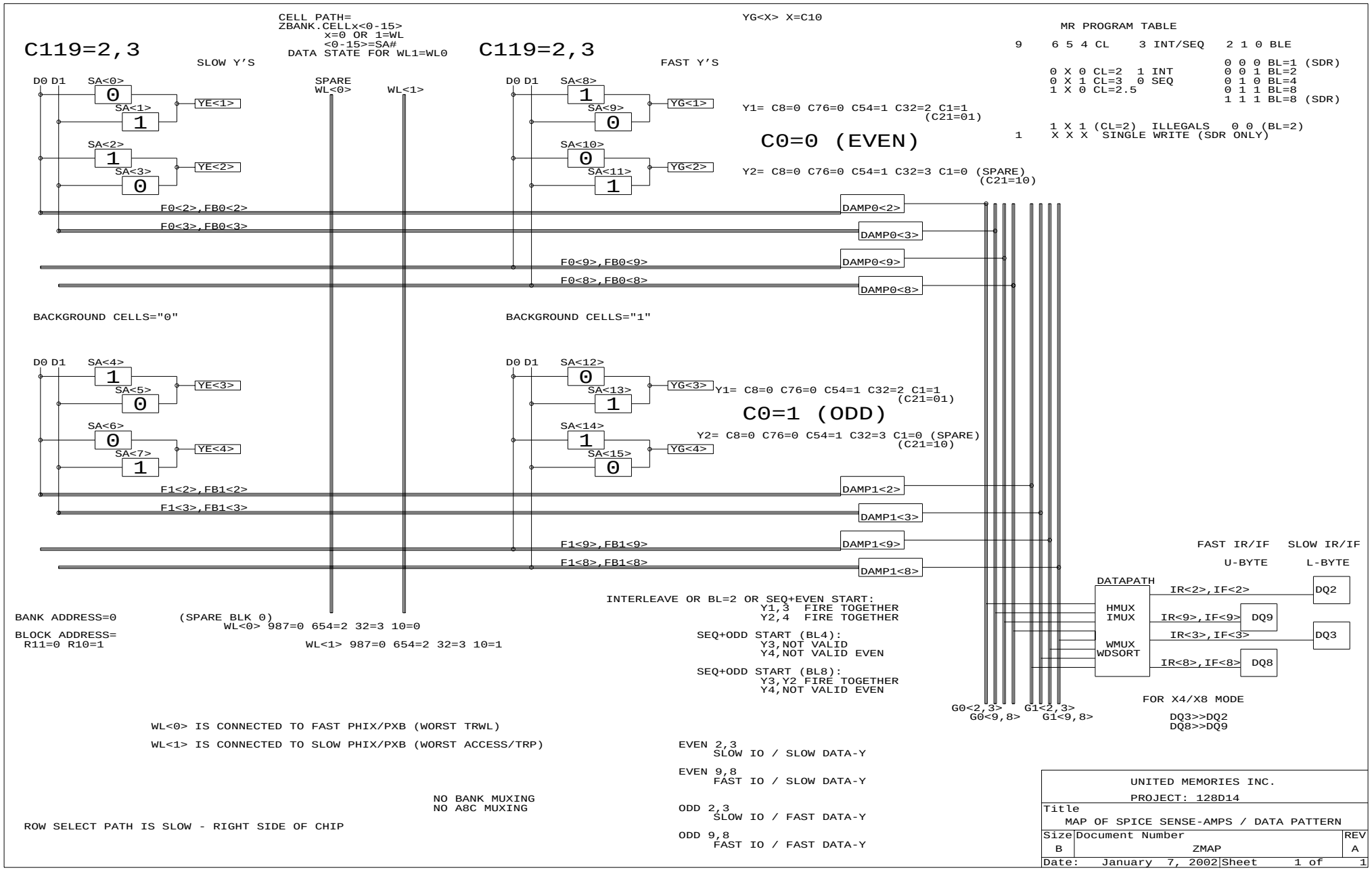
Circuit Name	Parent Circuit	Book Section	Schematic Title
CPBUF	CONBLK	CONBLK	CONTROL INPUT BUFFER (3X SIZE)
CPDLOG	CLKGEN	CLKGEN	CPDLOG
CPRDEC	COL	COL	COLUMN PRE-DECODERS
CPRDEC2	CPRDEC	COL	COLUMN PRE-DECODER LOGIC
CTMDAT	HMUX2	DPATH	Compression Test Mode Data Generator
CYDELB	ROWCON	CONBLK	CONBLK - YDELB DRIVER
-D-			
D119BLK	CHLF	COL	DATA PAIR FOR C119
D119SEL	D119BLK	COL	DATA PAIR SELECT FOR C119 ADDRESS
D14CHIP	none	CHIP/ESD	DDR/SDR - S14 TECH - FULLCHIP LVS
D14PER	D14CHIP	CHIP/ESD	FULL PERIPHERY
D14TREG	N/A	N/A	INSTRUCTIONS FOR SETTING TEST MODE REGISTERS
DAMP	D119BLK	COL	DATA SENSE AMP
DCON	CONBLK	CONBLK	DATA CONTROLLER (H/I/X CLKS & WEN)
DDRCO	BCCON	BCCON	C0 (ODD-EVEN) LATCH/BUFFER
DDRV	D119BLK	COL	INPUT DATA DRIVE
DINBUF	QBLK	IOBLK	DATA INPUT BUFFER-SSTL
DINFF	QBLK	IOBLK	FLIP FLOP USED FOR LATCHING INPUT DATA
DISB	ASEL	ROW1k	DISABLE ROW SELECT FOR SPARE ENABLE
DLL	LMISC	DLL	Delay Locked Loop
DLLDPD	VDC	VDC	SPECIAL POWER DOWN FOR VINT-DLL
DLLR2	DLL	DLL	DLL RESET2
DMMUX	DPATH	DPATH	DATA MASK MUX POINT (X4/X8 VS. X16)
DPATH	D14PER	CHIP/ESD	DATA PATH (READ/WRITE)
DPD	CONBLK	CONBLK	DEEP POWER DOWN (DPD) GENERATION
DQSBLK	IOBLK	IOBLK	DQS BLK
DQSBUF	DQSBLK	IOBLK	DQS OUTPUT BUFFER
DQSCON	CONBLK	CONBLK	QFC/DQS/MASK/X16-X8-X4 CONTROL
DQSEN	DQSCON	DQSCON	DQS- WRITE CONTROL
DQSIN	DQSBLK	IOBLK	DQS INPUT BUFFER-SSTL
DQSSEL	IOBLK	IOBLK	SELECTION FOR DQS (L ONLY USED FOR X16)
DSCRAM	TDATA	TDATA	TEST MODE SCRAMBLE
DWLGEN	ROW1K	ROW1K	DUMMY WORDLINE GENERATOR
-E-			
ESDIN	RABLK	RABLK	INPUT PAD ESD (ADDRESS/CONTROL)
ESDIO	DQSCON	IOBLK	IO ESD
EXOR2	TDATA	DPATH	2 INPUT EXOR
EXOR3	DSCRAM	TDATA	3 INPUT EXOR
-F-			
FCHECK	ASEL	ROW1K	FCHECK TIMER GENERATOR
FDEL	DLL	DLL	Fixed Delay Line
FIDBIT	FIDBLK	LEFT/LMISC	FUSE IDENTIFICATION BIT
FIDBLK	LMISC	LEFT/LMISC	FUSE IDENTIFICATION BLOCK
FKOT	DCON	DCON	FAKE OT CLK (FKOT)/DATA SORT CLK (DSCLK)
FSETB	ROW1K	ROW1K	SPARE ROW - SET PULSE STROBE (BASED ON BAB)
FSLAT	DLL	DLL	FAST/SLOW signal latch
FSR	CPRDEC	COL	R11 FUSE SELECT FOR COLUMNS
-G-			
GCLK	BNKCON	CONBLK	GCLK GENERATION
GLW	DQSCON	DQSCON	GLOBAL LATCHED WRITE-DQS WRITE CONTROL
GMUX	D119BLK	COL	DATA SLAVE AND OUTPUT MUX
-H-			
HCLK	DCON	DCON	HCLK<0:3>/TCLK GENERATION
HMUX0	DPATH	DPATH	HCLK MUX C119=0 (X4/X8/16)
HMUX13	DPATH	DPATH	HCLK MUX C119=1,3 (X4/X8/16)
HMUX2	DPATH	DPATH	HCLK MUX C119=2 (X4/X8/16)

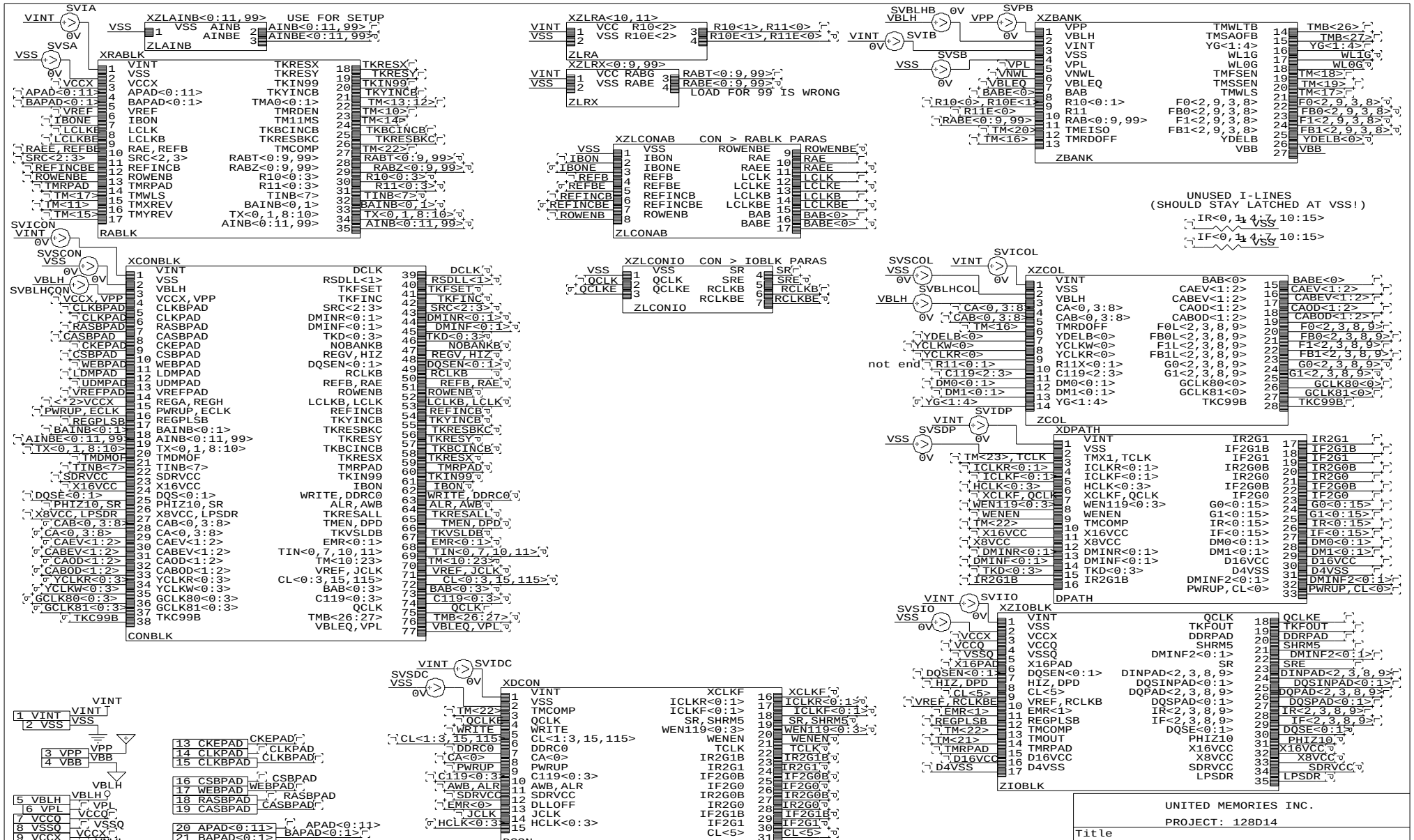
Circuit Name	Parent Circuit	Book Section	Schematic Title
HQSA	SABAND	BANK/ARY	H-QUAD SA AREA
HVDEL	DLL	DLL	ONE-HALF Voltage Controlled Delay LINE
-I-			
ICLK	DCON	DCON	ICLK R AND F GENERATION
IMUX	DPATH	DPATH	READ (I-LINE) DATA SORT CIRCUIT
IOBLK	D14PER	CHIP/ESD	I/O SIDE PERIPERHY BLOCK
IOCFG	IOBLK	IOBLK	I/O CONFIGURATION (X16/X8)
IOMISC	IOBLK	IOBLK	IO MISC CKTS
ISOEN	ROW1K	ROW1k	ISOEN GENERATOR
ISOGEN	ROW1K	ROW1k	ISO GENERATOR
-K-			
KBCEND	BCCON	BCCON	SHIFTED BURST END DETECT
-L-			
LEFT	D14PER	CHIP/ESD	LEFT
LMISC	LEFT	LEFT/LMISC	LEFT SIDE MISCELLANEOUS
LNPBGEN	BNKBOT	BNKBOT	LNB AND LPB GENERATOR
LREAD	BNKCON	BNKBOT	LATCHED READ COMMAND GENERATION
LWRITE	BNKCON	BNKBOT	LATCHED WRITE COMMAND GENERATION
-M-			
MRBIT	MRBLK	MR/SRM	MODE REGISTER BIT (NORMAL & EXTENDED)
MRBLDEC	MRBLK	MR/SRM	MODE REGISTER BURST LENGTH DECODER
MRBLK	CONBLK	CONBLK	MODE REGISTER BLOCK
MRCLDEC	MRBLK	MR/SRM	CAS-LATENCY DECODER
MRSCLK	CONBLK	CONBLK	MRS/TMRS/EMRS/RSDLL GENERATION
MRSRCDEC	MR/SRM	MR/SRM	SELF REFRESH CONTROL DECODER
MUX1	TDATA	TMBLK	2 TO 1 MUX - TRANSFER
MUX2	TDATA	TMBLK	2 TO 1 MUX - TRANSFER WITH DECODER
-O-			
OSC	LMISC	LEFT/LMISC	R11 FUSE SELECT FOR COLUMNS
OUTBUF	QBLK	IOBLK	DATA OUTPUT BUFFER
OUTDRV	OUTBUF	IOBLK	DATA OUTPUT DRIVER
-P-			
PD	DLL	DLL	Phase Detector
PDI_A	RABLK	RABLK	PAD DIODES FOR DM PINS
PDI_D	IOBLK	IOBLK	IO AND DQS PAD DIODES
PDI_DM	DSQCON	DSQCON	PAD DIODE FOR DM PINS
PHIOT	IOBLK	IOBLK	PHIOT-RISING AND FALLING-GENERATION
PHIX	ROW1K	ROW1K	PHIX GENERATOR (0:3)
POWCON	CONBLK	CONBLK	POWER CONTROL-REGULATORS/BUFFERS/HIZ
PREDEC	BNKCON	BNKCON	BANK PRECHARGE COMMAND GENERATION
PUGEN	LMISC	LEFT/LMISC	PWRUP GENERATOR
PXSEL	ROW1K	ROW1K	PXSEL GENERATOR (0:3)-(PHIX FRONT END)
-Q-			
QBLK	IOBLK	IOBLK	BLK AROUND I/O PAD
QCLK	CLKGEN	CONBLK	QCLK DRIVER/SOURCE MUX
QFUSE	CHLF	ZCOL	COLUMN FUSES PER HQUAD
-R-			
RAB1110	RABLK	RABLK	SPECIAL ROW ADDRESS BUF-FOR R11/R10
RABLK	LEFT	D14PER	ROW ADDRESS LOGIC BLOCK
RABUF	RABLK	RABLK	ROW ADDRESS BUFFER
RDARY	ROW1K	ROW1k	RDEC ARRAY
RDEC	RDARY	RDARY/SPR	Row Decoder
REFCLK	CONBLK	CONBLK	REF/SELF GENERATION
REFDEL	CONBLK	CONBLK	REFRESH DELAY TIMER
REFRATLD	VDC	VDC	REF/RAT LOAD CONTROL W/COUNTER
REGSHOT	REGV	POWCON	BAB ONE-SHOT FOR VBLH/VPP REGULATOR CONTROL
REGV	POWCON	POWCON	VBLH(1.8V)/VINT(2.5V) + VPP REG ENABLE
RFUSE	SPRBLK	RDARY/SPR	ROW FUSES PER 4M ARRAY
RMISC	D14PER	CHIP/ESD	RIGHT SIDE MISCELLANEOUS

Circuit Name	Parent Circuit	Book Section	Schematic Title
ROW1K	BNKBOT	BNKBOT	SUPPORT CIRCUIT FOR 1K ROWS
ROWCON	CONBLK	CONBLK	ROW ADDRESS MAIN CONTROL
RP32	RDARY	RDARY/SPR	ROW PRE-DECODER (2 INPUT) R32(0:3)
RP987	RDARY	RDARY/SPR	ROW PRE-DECODER (3 INPUT) R987,R654
-S-			
S0SHFT	DCON	DCON	S0 (ODD-EVEN) SHIFTER
S119	DCON	DCON	C11 C9 SHIFTER (4X) <0:3>
SA2	HQSA	BNK/ARY	SENSE AMP-TWO
SABAND	ARY32M	BNK/ARY	SA BAND-8X HQSA
SAEQCON	BNKBOT	BNKBOT	EQ CONTROL FOR SENSE AMP LINES
SDRCONF	IOBLK	IOBLK	SDRVCC/LPSDR GENERATION
SEAGAT	CONBLK	CONBLK	EXTRA TRANSISTORS (SEA OF GATES)
SENSH	ROW1K	ROW1K	SEN AND SH GENERATOR
SHIFTR	DCON	DCON	SHIFT READ CONTROL
SHMUX	HQSA	BNK/ARY	SH CONTROLLED DATA MUX (1 PER QUAD)
SPCDEC	CHLF	COL	SPARE COLUMN DECODER
SRMBIT	SRMBLK	MR/SRM	SELF REFRESH MODE BIT COUNTER
SPRBLK	ROW1K	ROW1K	SPARE ROW BLOCK (1X/4 MEG)
SPRDEC	SPRBLK	RDARY/SPR	SPARE ROW DECODER (8X/4MEG)
SPREN	SPRDEC	RDARY/SPR	SPARE ROW FUSE SET ENABLE
SPRSEL	SPRDEC	RDARY/SPR	SPARE ROW ADDRESS SELECT-1 PER R0-R9
SRMBLK	CONBLK	MR/SRM	Self-Refresh Mode Block
STUNDIN	IOBLK	IOBLK	TUNING CIRCUIT FOR DATA - SDR MODE
STUNDM	DQSCON	DQSCON	SDR TUNING CIRCUIT FOR 2 DATA MASK SIG.
SW	BNKCON	BNKCON	SHIFTED WRITE GENERATION
-T-			
TDATA	TMBLK	TMBLK	TEST MODE DATA
TDBIT	TDATA	TMBLK	TDATA - BIT
TINB7	RABLK	RABLK	TINB DRIVER/LATCH FOR A7
TINDRV	TMBLK	TMBLK	TIN DRIVERS <7,10:12>
TKACT	TMBLK	CONBLK	TESTMODE - ACTIVE, XINC, AND BKXINC
TKC1	CABLK	CABLK	SHIFTED C1 FOR COMPRESSION
TKCOM	CONBLK	CONBLK	TKCOM
TKCON	TMBLK	TMBLK	TEST CLOCK CONTROL
TKFS	TMBLK	TMBLK	TEST MODE RESET - FUSE ID SET/SHIFT
TKRES	TMBLK	CONBLK	TEST MODE RESET - X,Y,BKC,ALL
TKYINCB	TMBLK	CONBLK	TEST MODE Y AND BANK - COL INCREMENT CONTROL
TMBIT	TMBLK	TMBLK	TEST MODE BIT
TMBLK	CONBLK	CONBLK	COMPLETE TESTMODE
TMINVREV	TMBLK	TMBLK	TMINV/TMXREV/TMYREV SELECT
TMRPAD	TMBLK	TMBLK	GENERATE TMRPAD
TMRSCLK	CONBLK	CONBLK	TMRS GENERATION
TMSAOFB	TMBLK	TMBLK	TEST MODE - SENSE AMP OFF BAR (VPP LEVELS)
TMVM	DSQCON	DSQCON	VOLTAGE MEASURING CIRCUIT/VDM PAD
TMVSBIT	RAFRATLD	VDC	TEST MODE VSR BIT
TUNAD	RABLK	RABLK	TUNING CIRCUIT FOR 13 ADDRESS INPUTS
TUNC	CONBLK	CONBLK	TUNING CIRCUIT FOR 4 CONTROL SIGNALS
TUNDIN	IOBLK	IOBLK	TUNING CIRCUIT FOR DATA/DQS INPUTS
TUNDM	DSQCON	DSQCON	TIMING CIRCUIT FOR 2 DATA MASK SIGNLALS
TX10L	IOBLK	IOBLK	TX10 LATCH
TXDRIVER	RABLK	RABLK	PROVIDE ROW ADDRESS TO TDATA GENERATOR
-V-			
VBBCLK	VBBGEN	VBB/VNWL	VBB Pump Clocks
VBBGEN	VBB	VBB/VNWL	VBB GENerator
VBBPUMP	VBBGEN	VBB/VNWL	Pump for Vbb Generator
VBLHLD	VDC	VDC	VBLH LOAD CONTROL W/COUNTER
VBLHTRM	VDC	VDC	VBLH TRIM
VCMP	VHBLH	VPL	Voltage Current Mirror P-type
VCON	DLL	DLL	Delay Voltage generator (DLL)

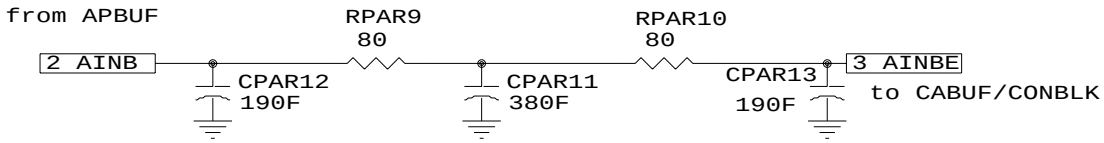
Circuit Name	Parent Circuit	Book Section	Schematic Title
VDC	LMISC	LEFT/LMISC	VCCI/VCC VOLTAGE DOWN CONVERTERS
VDCA	VDC	VDC	ACTIVE VINT REG
VDCB	VDC	VDC	STANDBY VINT/VBLH REG
VDCRAT	VDC	VDC	VDC RATIO CIRCUIT
VDEL	HVDEL	DLL	Voltage Controlled Delay Element
VHALF	VHBLH	VPL	Voltage HALF vblh
VHBLH	VPL	VPL	Voltage Half vBLH
VHQBIAS	IOBLK	IOBLK	HALF VCCQ FCAP BIAS
VHREF	VHBLH	VPL	Voltage HALF vblh REFerence
VINTLD	VDC	VDC	VINT LOAD CONTROL W/COUNTER
VINTTRM	VDC	VDC	VINT TRIM
VMSELX	TMVM	DSQCON	SELECT CIRCUIT FOR V-MEAS MODES
VNOSC	VNWLGEN	VBB/VNWL	Negative Voltage generator OSCillator
VNREF	VNWLGEN	VBB/VNWL	Voltage Negative REFerence
VNREG	VNWLGEN	VBB/VNWL	REGULATOR FOR NEGATIVE VOLTAGE GENERATOR
VNWLCLK	VNWLGEN	VBB/VNWL	VNWLL PUMP CLOCK
VNWLGEN	LMISC	LEFT/LMISC	VNWL GENerator
VNWLPUMP	VNWLGEN	VBB/VNWL	Pump for VNWLL Generator
VPCKDEC	VPPCLK	VPP	Voltage Positive Pump Clock Decode
VPP	LMISC	LEFT/LMISC	Voltage Positive Pump
VPPCLK	VPP	VPP	Voltage Positive Pump CLocK
VPPCLK2	VPPCLK	VPP	Voltage Positive Pump CLocK #2
VPPDLY	VPPCLK	VPP	Voltage Positive Pump DeLaY
VPPREG	VPP	VPP	Voltage Positive Pump REGulator
VPPUMP	VPP	VPP	Voltage Positive PUMP
VREF	VDC	VDC	VREF GENERATOR
VREFBG	LMISC	LEFT/LMISC	VOLTAGE REFERENCE BAND GAP
VSR FUSE	N/A	N/A	VOLTAGE SET REGISTER FUSE CIRCUITRY
VSRLDR	RMISC	RMISC	VSR LOAD CONTROL W/COUNTER
VSRLDRR	RMISC	RMISC	RIGHT SIDE - VSR LOAD CONTROL W/COUNTER
-W-			
WDCON	DCON	DCON	WRITE DATA CONTOL (C0 SORTING)
WDSORT	DPATH	DPATH	WRITE DATA SORT CIRCUIT
WEN119	DCON	DCON	WEN119<0:3> GENERATION
WMUX	DPATH	DCON	WRITE DATA MUX POINT (X4/X8/16) (Ir and If)
WMUXCON	DPATH	DPATH	WMUX CONTROL LOGIC
WP2	CABLK	CABLK	WRITE COMMAND PULSE-DELAYED 2 CYCLES
-X-			
XCLKF	DCON	DCON	XCLKF GENERATION
-Y-			
YCLKW	BNKCON	BNKCON	YCLK-WRITE GENERATION
YDELB	BNKBOT	BNKBOT	YDELB DRIVER (1X PER BANK)
YRGCLK	BNKCON	BNKCON	YR/GCLKB GENERATION
-Z-			
Z14FULL	NONE	Z14FULL	FULL CHIP SPICE - 128M DDR/SDR (S14)
Z14FULL	sim.	Z14FUll	128D14 dram FULL chip simulation
ZBANK	Z14FULL	Z14FUll	32meg array BANK
ZBANK	Z14FULL	Z14FULL	SPICE-32M BANK (ARRAY PLUS BOT32M LOGIC)
ZBL512	ZSABAND	ZBANK	BIT LINE PAIR (512 CELLS/BL=1024WL/BL)
ZCHLF	ZCOL	ZCOL	COLUMN HALF-SPICE
ZCOL	sim.	ZCOL	COLumn circuits
ZCOL	Z14FULL	Z14FULL	COLUMN CIRCUIT (2X-TOP AND BOTTOM)
ZCPRDEC	ZCOL	ZCOL	COLUMN PRE-DECODERS
ZCPRDEC2	ZCPRDEC	ZCOL	COLUMN PRE-DECODER LOGIC
ZDPAR	ZSABAND	ZBANK	LOCAL D-LINE (IN Sense Amp) Parasitics
ZF1K	N/A	OTHER SPICE	SEMI-FULL CHIP, + 1K ROWS (SIMULATION)
ZFBNKBOT	N/A	OTHER SPICE	SEMI-FULL CHIP, + 1 BANK BOT
ZFCOL	N/A	OTHER SPICE	SEMI-FULL CHIP, + COL LVS
ZFIO	N/A	OTHER SPICE	SEMI-FULL CHIP, + COL LVS
ZFPAR	ZBANK	ZBANK	F-LINE (ACROSS ARRAY) Parasitics

Circuit Name	Parent Circuit	Book Section	Schematic Title
ZIOBLK	sim.	ZIOBLK	Input/Output BLocK
ZIOBLK	Z14FULL	Z14FUll	SPICE-I/O SIDE PERIPHERY BLOCK
ZLAINB	Z14FULL	Z14FUll	SPICE - AIN PARAS FOR SETUP LINES
ZLC1EV	ZCOL	ZCOL	COL ADDRESS PARAS (C1) EVEN
ZLC1OD	ZCOL	ZCOL	COL ADDRESS PARAS (C1) ODD
ZLC32EV	ZCOL	ZCOL	C32 COL ADDRESS PARAS-EVEN CASE
ZLC32OD	ZCOL	ZCOL	C32 COL ADDRESS PARAS-ODD LINES
ZLCOL	ZCOL	ZCOL	COL ADDRESS PARAS (OTHER THAN CA)
ZLCONAB	Z14FULL	Z14FULL	CONBLK>>RABLK PARA’S
ZLCONIO	Z14FULL	Z14FULL	CONBLK>>IOBLK PARA’S
ZLCXX	ZCOL	ZCOL	C54/C76 COL ADDRESS PARAS (NO ODD/EVEN)
ZLG	ZCOL	ZCOL	G LINE PARAS IN COl
ZLIRF	ZIOBLK	ZIOBLK	SPICE-IR/IF LINE PARAS
ZLOT	ZIOBLK	ZIOBLK	SPICE-OTR and OTF LOADS
ZLPHIX	ZRDARY	ZBANK	SPICE LOADS FOR PHIX AND PXB
ZLPHIZ	ZIOBLK	ZIOBLK	SPICE-PHIZ/DQS/DQSEN LOADS
ZLRA	Z14FULL	Z14FUll	SPICE-ARRAY SELECT (11,10) PARASITICS
ZLRX	Z14FULL	Z14FUll	SPICE-NORMAL ROW ADDS (0-9) PARASITICS
ZMAP	none	Z14FUll	MAP OF SPICE SENSE-AMPS/DATA PATTERN
ZPSMA	N/A	VBB/VNWL	SPICE POWER SUPPLIES FOR MEMORY ARRAY
ZRDARY	ZROW1K	ZBANK	SPICE-RDEC ARRAY
ZROW1K	ZBANK	ZBANK	SPICE VERSION OF 1K ROW BLOCK
ZSABAND	ZBANK	ZBANK	SPICE-1 SABAND (2K SAs)
ZSAPAR	ZSABAND	ZBANK	Sense Amp Band Parasitics (SPICE)
ZSFC	N/A	OTHR SPICE	SEMI-FULL CHIP (SIMULATION)
ZVBBCNET	ZPSMA	VBB/VNWL	SPICE VBB CAPACITOR NETWORK
ZVHBLH	NONE	VPL	Spice Voltage Half vBLH
ZVHCNET	VHBL	VPL	VHblh Capacitor NETwork
ZWL	ZBANK	ZBANK	WORD LINE SPICE MODEL
ZYPAR	ZBANK	ZBANK	Y-LINE (ACROSS ARRAY) Parasitics


CELL PATH=
ZBANK.CELLx<0-15>
x=0 OR 1=WL
<0-15>=SA#
DATA STATE FOR WL1=WL0
YG<X> X=C10
MR PROGRAM TABLE
9 6 5 4 CL 3 INT/SEQ 2 1 0 BLE
0 0 0 BL=1 (SDR)
0 X 0 CL=2 1 INT 0 0 1 BL=2
0 X 1 CL=3 0 SEQ 0 1 0 BL=4
1 X 0 CL=2.5 0 1 1 BL=8
1 1 1 BL=8 (SDR)
1 X 1 (CL=2) ILLEGALS 0 0 (BL=2)
1 X X X SINGLE WRITE (SDR ONLY)
C119=2,3
SLOW Y'S
SPARE
WL<0>
WL<1>
C119=2,3
FAST Y'S
D0 D1
SA<0>
SA<1>
SA<2>
SA<3>
YE<1>
YE<2>
SA<8>
SA<9>
SA<10>
SA<11>
YG<1>
YG<2>
Y1= C8=0 C76=0 C54=1 C32=2 C1=1
(C21=01)
C0=0 (EVEN)
Y2= C8=0 C76=0 C54=1 C32=3 C1=0 (SPARE)
(C21=10)
F0<2>,FB0<2>
F0<3>,FB0<3>
F0<9>,FB0<9>
F0<8>,FB0<8>
DAMP0<2>
DAMP0<3>
DAMP0<9>
DAMP0<8>
BACKGROUND CELLS="0"
BACKGROUND CELLS="1"
SA<4>
SA<5>
SA<6>
SA<7>
YE<3>
YE<4>
SA<12>
SA<13>
SA<14>
SA<15>
YG<3>
YG<4>
Y1= C8=0 C76=0 C54=1 C32=2 C1=1
(C21=01)
C0=1 (ODD)
Y2= C8=0 C76=0 C54=1 C32=3 C1=0 (SPARE)
(C21=10)
F1<2>,FB1<2>
F1<3>,FB1<3>
F1<9>,FB1<9>
F1<8>,FB1<8>
DAMP1<2>
DAMP1<3>
DAMP1<9>
DAMP1<8>
FAST IR/IF
SLOW IR/IF
U-BYTE
L-BYTE
DATAPATH
HMUX
IMUX
WMUX
WDSORT
IR<2>,IF<2>
IR<9>,IF<9>
IR<3>,IF<3>
IR<8>,IF<8>
DQ2
DQ9
DQ3
DQ8
INTERLEAVE OR BL=2 OR SEQ+EVEN START:
Y1,3 FIRE TOGETHER
Y2,4 FIRE TOGETHER
SEQ+ODD START (BL4):
Y3,NOT VALID
Y4,NOT VALID EVEN
SEQ+ODD START (BL8):
Y3,Y2 FIRE TOGETHER
Y4,NOT VALID EVEN
BANK ADDRESS=0
(SPARE BLK 0)
WL<0> 987=0 654=2 32=3 10=0
BLOCK ADDRESS=
R11=0 R10=1
WL<1> 987=0 654=2 32=3 10=1
G0<2,3>
G0<9,8>
G1<2,3>
G1<9,8>
FOR X4/X8 MODE
DQ3>>DQ2
DQ8>>DQ9
WL<0> IS CONNECTED TO FAST PHIX/PXB (WORST TRWL)
WL<1> IS CONNECTED TO SLOW PHIX/PXB (WORST ACCESS/TRP)
EVEN 2,3
SLOW IO / SLOW DATA-Y
EVEN 9,8
FAST IO / SLOW DATA-Y
NO BANK MUXING
NO A8C MUXING
ODD 2,3
SLOW IO / FAST DATA-Y
ODD 9,8
FAST IO / FAST DATA-Y
ROW SELECT PATH IS SLOW - RIGHT SIDE OF CHIP
UNITED MEMORIES INC.
PROJECT: 128D14
Title
MAP OF SPICE SENSE-AMPS / DATA PATTERN
Size B
Document Number
ZMAP
REV A
Date: January 7, 2002
Sheet 1 of 1

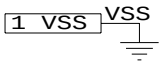

XZLAINB<0:11,99>
USE FOR SETUP
AINB<0:11,99>
AINBE<0:11,99>
ZLAINB
XRABLK
RABLK
XZLRA<10,11>
R10<1>,R11<0>
R10E<1>,R11E<0>
ZLRA
XZLRX<0:9,99>
RABT<0:9,99>
RABE<0:9,99>
LOAD FOR 99 IS WRONG
ZLRX
XZBANK
ZBANK
XZLCONAB
CON > RABLK PARAS
ZLCONAB
UNUSED I-LINES
(SHOULD STAY LATCHED AT VSS!)
XCONBLK
CONBLK
XZLCONIO
CON > IOBLK PARAS
ZLCONIO
XZCOL
ZCOL
XDPATH
DPATH
XZIOBLK
ZIOBLK
XDCON
DCON
UNITED MEMORIES INC.
PROJECT: 128D14
Title
FULL CHIP SPICE - 128M DDR/SDR (S14)
Size B
Document Number Z14FULL
REV A
Date: December 7, 2001
Sheet 1 of 1

AINB<10> USED FOR R/C-EXTRACT



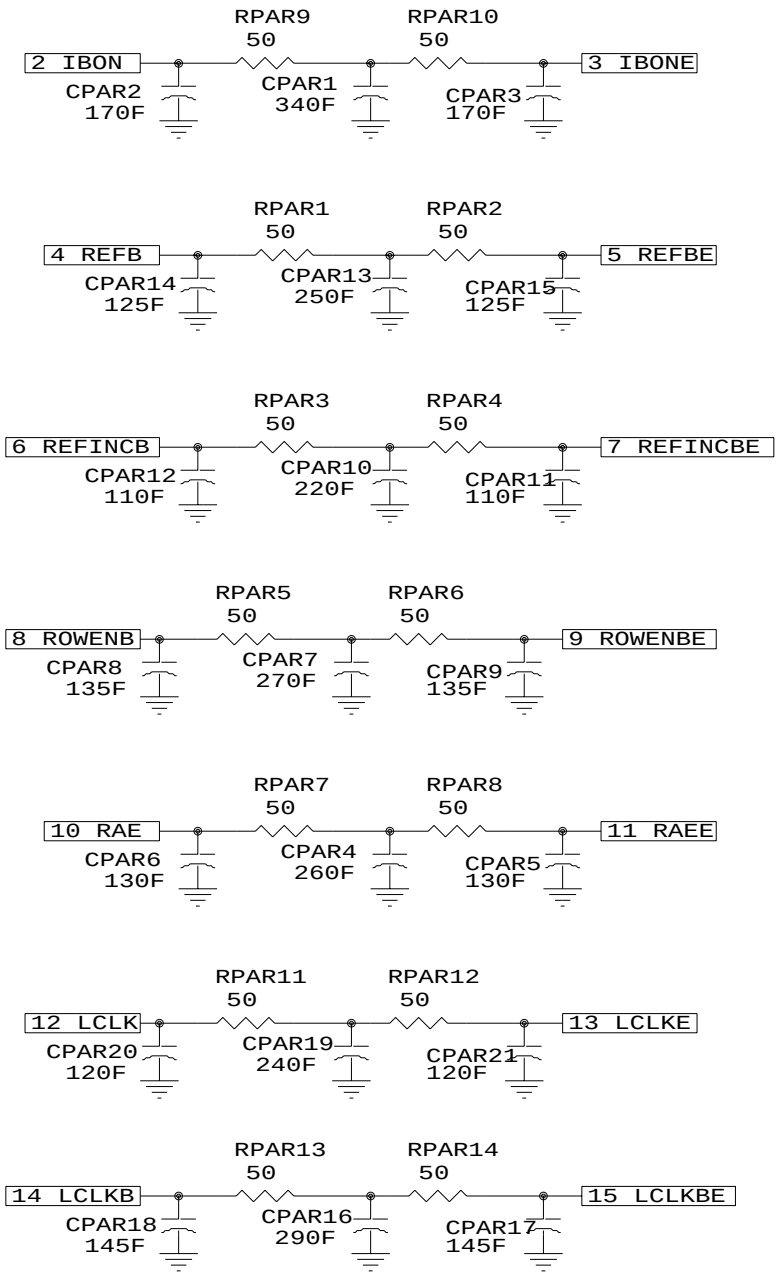
SLOW CASE, WC SETUP

ALL GATE LOADS ARE ACCOUNTED FOR DIRECTLY!



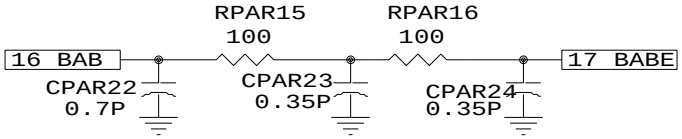
PLACED IN Z14FULL

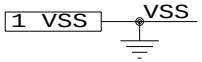
UNITED MEMORIES LTD PROJECT: 128D14		
Title SPICE - AIN PARAS FOR SETUP LINES		
Size A	Document Number ZLAINB	REV A
Date: October 12, 2001	Sheet 1 of 1	



FOR REFB,RAE,ROWENB,REFINCB
L~2000U
W=0.8U
=130 OHMS

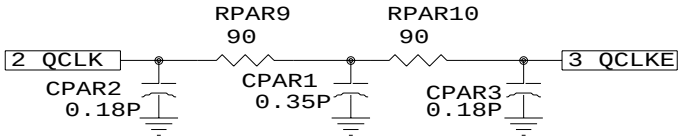
W=0.6 L=2681 FOR BANK SECTION

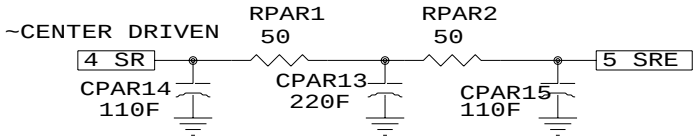


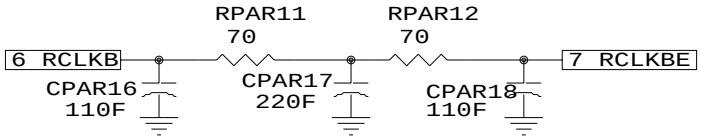


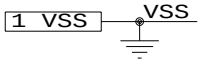
PLACED IN TOP LEVEL SPICE- Z14FULL

UNITED MEMORIES INC. PROJECT: 128D14		
Title CONBLK>>RABLK PARA'S		
Size A	Document Number ZLCONAB	REV A
Date: November 7, 2001	Sheet 1 of 1	





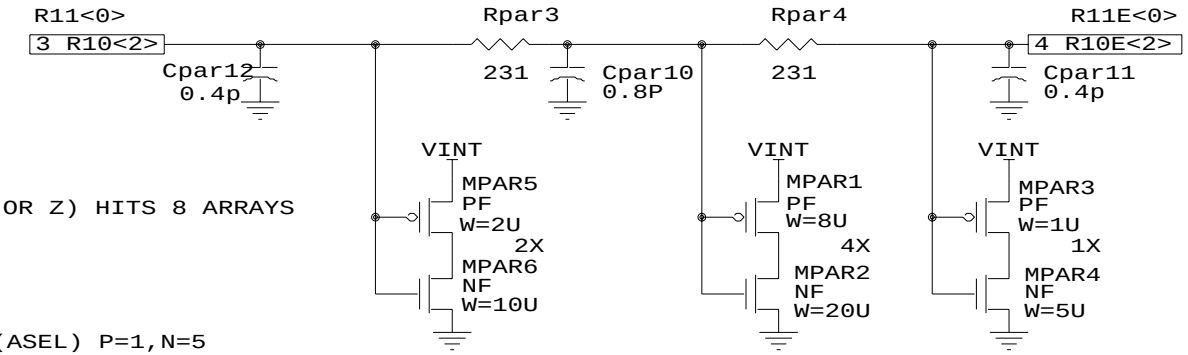




PLACED IN TOP LEVEL SPICE- Z14FULL

UNITED MEMORIES INC. PROJECT: 128D14		
Title CONBLK>>IOBLK PARA'S		
Size A	Document Number ZLCONIO	REV A
Date: November 21, 2001	Sheet 1 of 1	

asel addresses



W=0.6U
L=2681/BNKBOT

SP=.8

376 OHM

CENTER=46 OHM
START=40 OHM

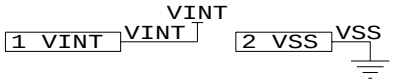
1X ALREADY IN SPICE

EACH SIDE (T OR Z) HITS 8 ARRAYS
(50%)

EACH ARRAY (ASEL) P=1,N=5

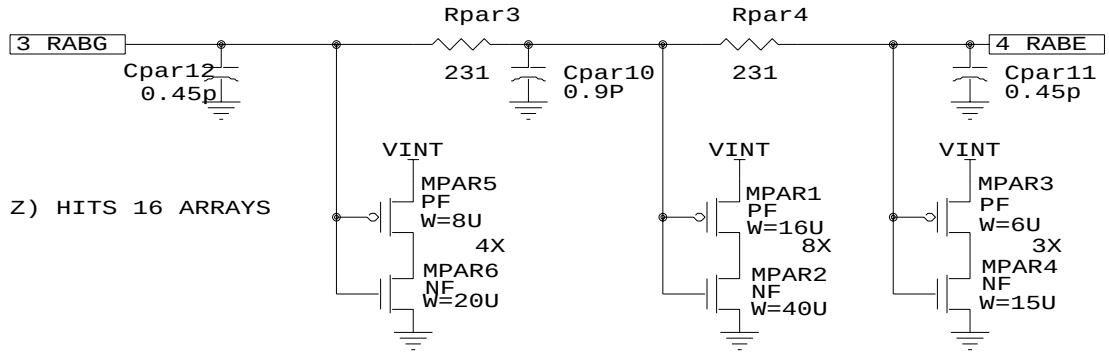
C~ 700F/BANK + 150 CENTER +50 RABLK=~1.6P

PLACED IN Z14FULL



UNITED MEMORIES LTD PROJECT: 128D14		
Title SPICE-ARRAY SELECT (11,10) PARASITICS		
Size A	Document Number ZLRA	REV A
Date: November 7, 2001	Sheet 1 of 1	

NORMAL ADDRESSES (RAB<0:9>)



W=0.8U
L=8050U

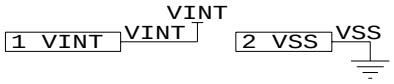
SP=.86U

EACH SIDE (T OR Z) HITS 16 ARRAYS
100% HIT

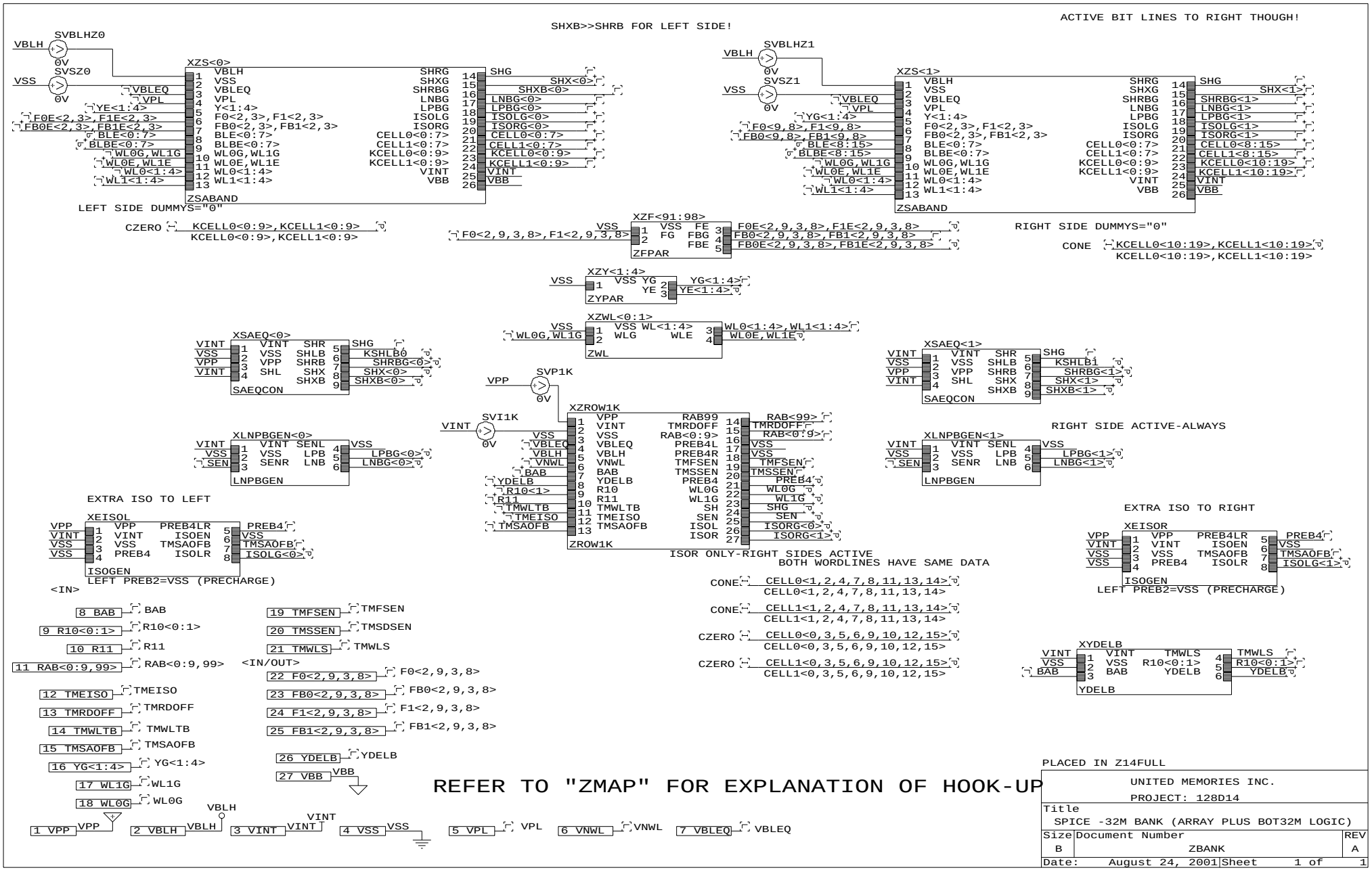
1X ALREADY IN SPICE

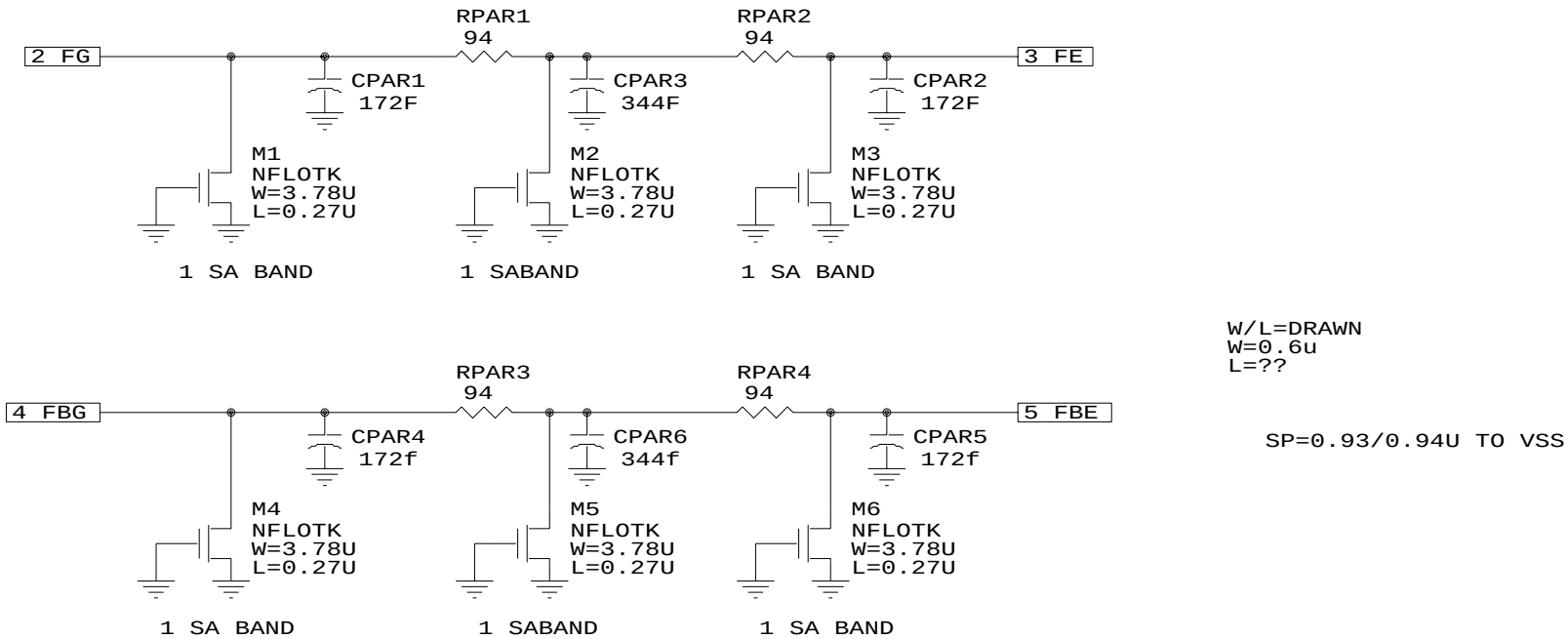
EACH ARRAY (BLKRBUF) P=2,N=5

PLACED IN Z14FULL



UNITED MEMORIES LTD PROJECT: 128D14		
Title SPICE-NORMAL ROW ADDS (0-9) PARASITICS		
Size A	Document Number ZLRX	REV A
Date: November 7, 2001	Sheet 1 of 1	

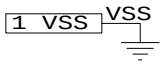

SHXB>>SHRB FOR LEFT SIDE!
ACTIVE BIT LINES TO RIGHT THOUGH!
SVBLHZ0
SVSZ0
SVBLHZ1
SVSZ1
XZS<0>
XZS<1>
ZSABAND
LEFT SIDE DUMMYS="0"
RIGHT SIDE DUMMYS="0"
CZERO
CONE
XZF<91:98>
ZFPAR
XZY<1:4>
ZYPAR
XZWL<0:1>
ZWL
XSAEQ<0>
XSAEQ<1>
SAEQCON
SVP1K
SVI1K
XZROW1K
ZROW1K
XLNPBGEN<0>
XLNPBGEN<1>
LNPBGEN
RIGHT SIDE ACTIVE-ALWAYS
EXTRA ISO TO LEFT
EXTRA ISO TO RIGHT
XEISOL
XEISOR
ISOGEN
LEFT PREB2=VSS (PRECHARGE)
ISOR ONLY-RIGHT SIDES ACTIVE
BOTH WORDLINES HAVE SAME DATA
XYDELB
<IN>
<IN/OUT>
REFER TO "ZMAP" FOR EXPLANATION OF HOOK-UP
PLACED IN Z14FULL
UNITED MEMORIES INC.
PROJECT: 128D14
Title
SPICE -32M BANK (ARRAY PLUS BOT32M LOGIC)
Size B
Document Number ZBANK
REV A
Date: August 24, 2001
Sheet 1 of 1



EACH F LINE HITS 5 SABANDS

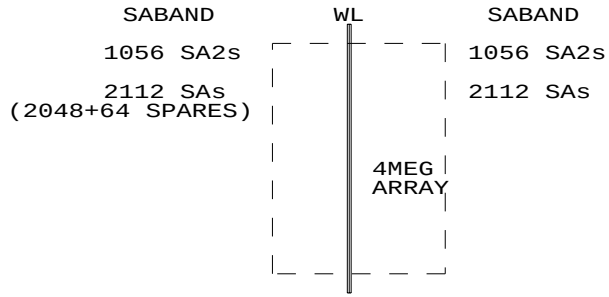
(2 ARE ALWAYS INACTIVE-WRONG SIDE)
2 ARE IN SPICE

PLACED IN ZBANK



UNITED MEMORIES INC. PROJECT: 128D14		
Title F-LINE (ACROSS ARRAY) Parasitics		
Size A	Document Number ZFPAR	REV A
Date: September 17, 2001	Sheet 1 of 1	

LVS ARRANGEMENT



NOTES: FOR M1 CAPACITANCE, ASSUME SOLID SHEET OF M0 AND SOLID SHEET OF M2 ON BOTH SIDES, AND WC OXIDE THICKNESSES (0.295FF/U)

FOR GC CAPACITANCE, ASSUME OVER FIELD, UNDER SOLID SHEET OF M0 (0.161FF/U)

FOR M1 RESISTANCE ASSUME W=0.14U, L=2416, R=0.14 OHMS/SQ.

FOR GC RESISTANCE, ASSUME W=0.14U, L=75.5U, R=14 OHMS/SQ.

WL M1 LENGTH = 2416U, 1GC SEGMENT = 151U

CPAR5=12.2FF + 44.5FF = 1/2 GC SEGMENT CAP + 1 M1 SEGMENT CAP
RPAR5=1 M1 SEGMENT RESISTANCE
RPAR6=1/2 GC SEGMENT RESISTANCE

PER BAND

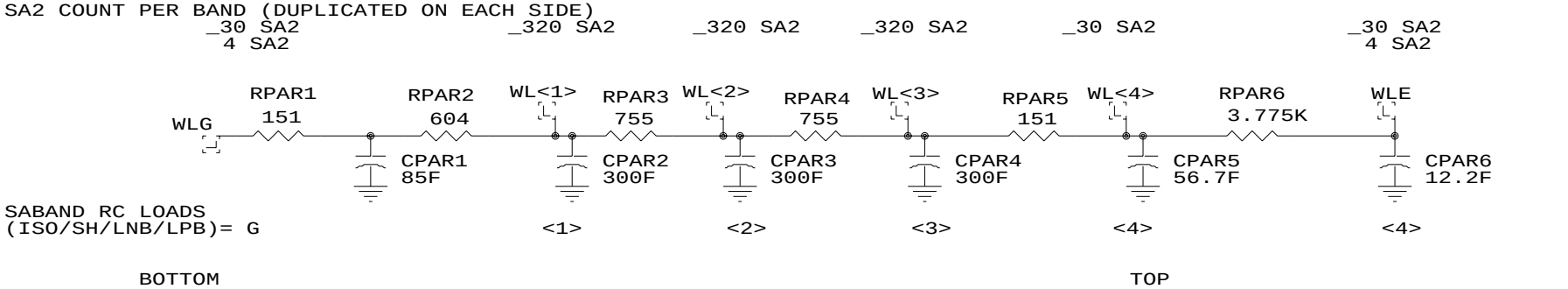
SA COUNT	SA2 COUNT
660	330
660	330
660	330
66	33
66	33
= 2112	= 1056

(1056=PRECISE)

1058 SA2/SIDE

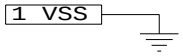
SPICE-SABAND PROGRAMMING

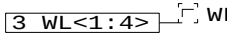
SA2 COUNT PER BAND (DUPLICATED ON EACH SIDE)



NOTE: 1280X ZBL512 PASS GATE CONNECTIONS AT WL<1,2,3>
120X ZBL512 PASS GATE CONNECTIONS AT WL<4>
136X ZBL128 PASS GATE CONNECTIONS AT WLG AND WLE

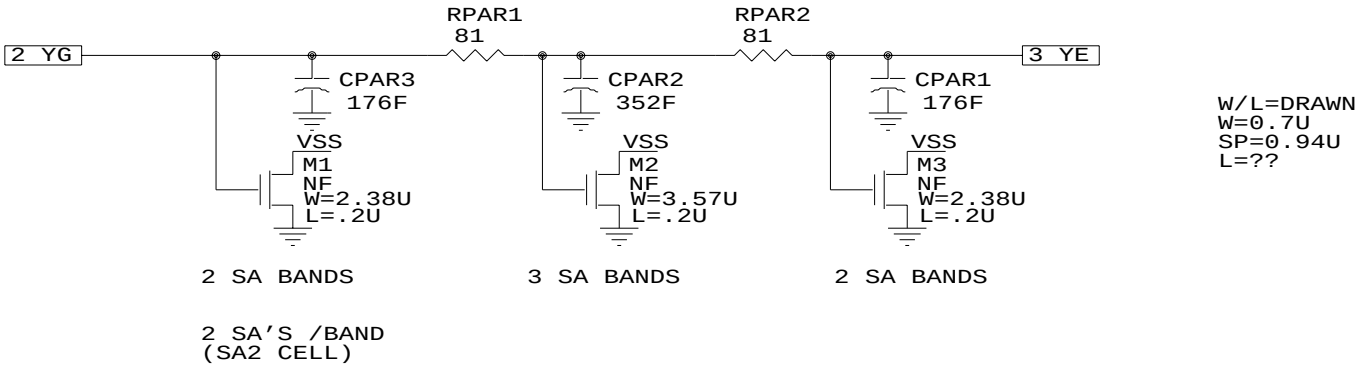
PLACED IN ZBANK





SEE ZSABAND FOR EXACT PLACEMENT OF SA/BITLINE MODELS

UNITED MEMORIES, INC. PROJECT: 128D14		
Title WORD LINE SPICE MODEL		
Size A	Document Number ZWL	REV A
Date: January 8, 2001	Sheet 1 of 1	

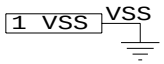


W/L=DRAWN
W=0.7U
SP=0.94U
L=??

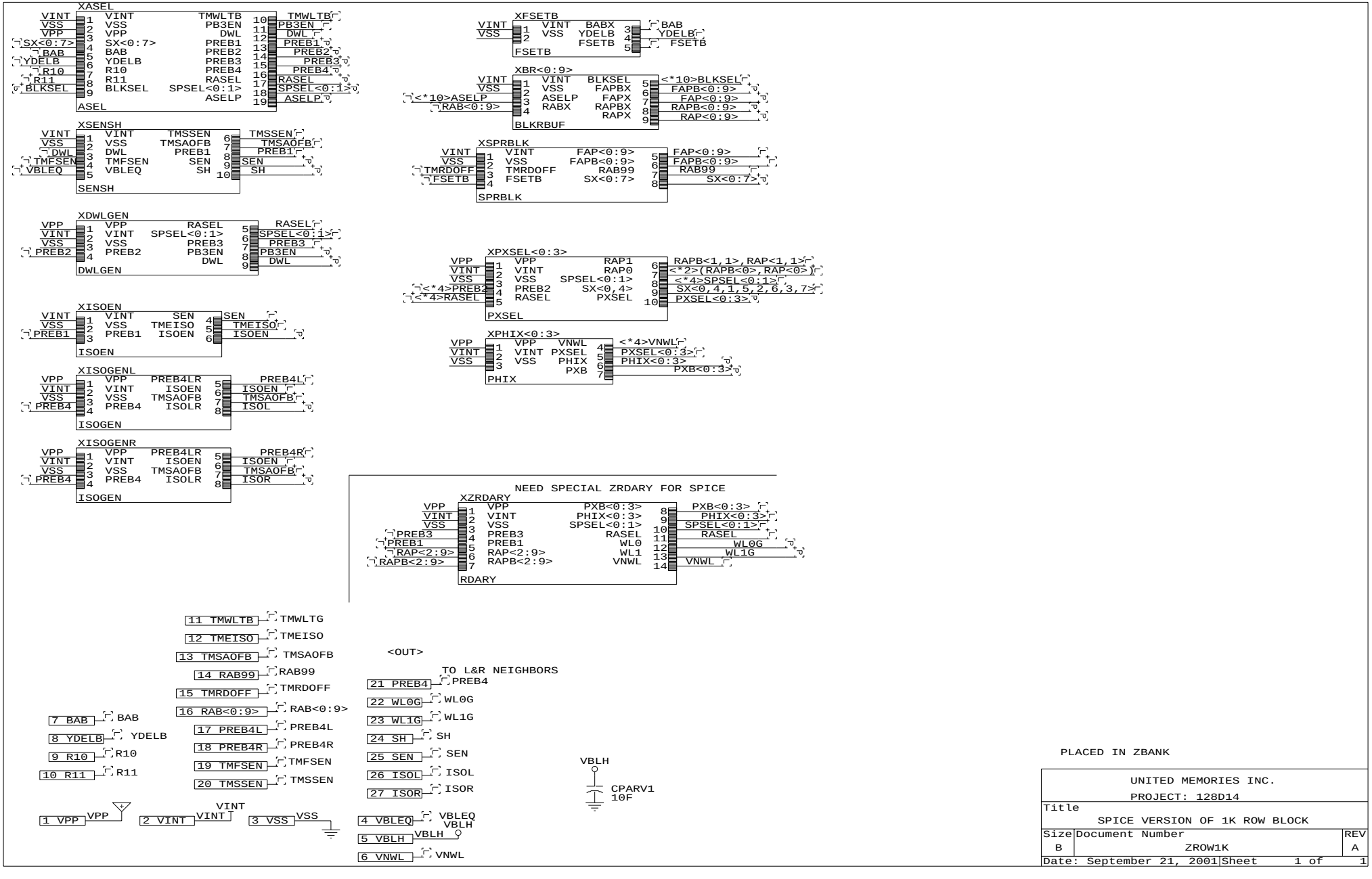
EACH Y LINE HITS 9 SABANDS
2 YSELS/SABAND
TOTAL F0=1.61X4=6.5U/BAND

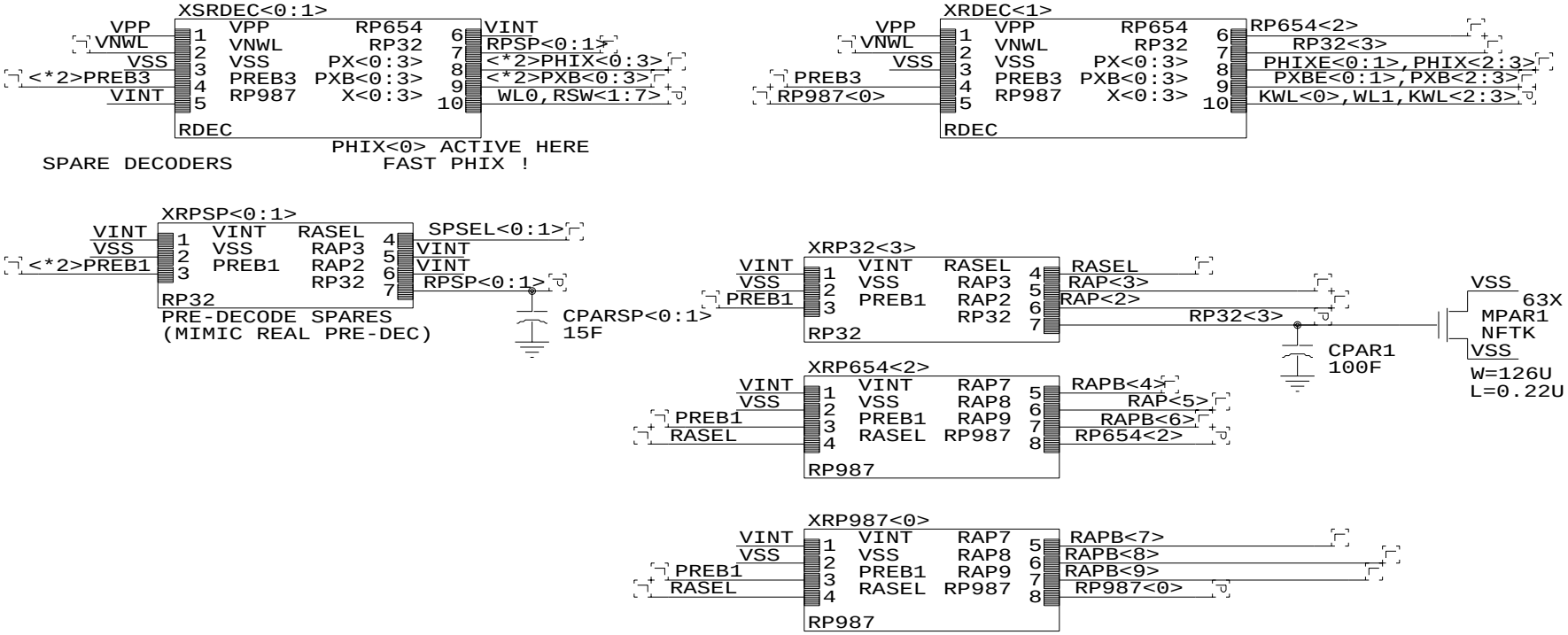
(2 ARE IN SPICE)

PLACED IN ZBANK



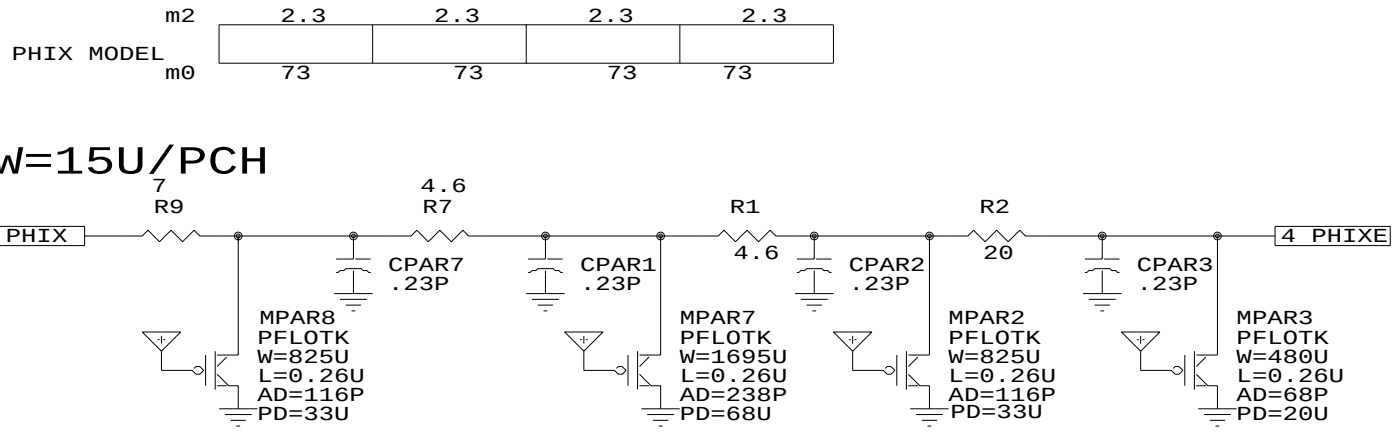
UNITED MEMORIES INC. PROJECT: 128D14		
Title Y-LINE (ACROSS ARRAY) Parasitics		
Size A	Document Number ZYPAR	REV A
Date: September 17, 2001	Sheet 1 of 1	


XASEL
VINT VSS VPP SX<0:7> BAB YDELB R10 R11 BLKSEL
VINT VSS VPP SX<0:7> BAB YDELB R10 R11 BLKSEL
TMWLTB PB3EN DWL PREB1 PREB2 PREB3 PREB4 RASEL SPSEL<0:1> ASELP
TMWLTB PB3EN DWL PREB1 PREB2 PREB3 PREB4 RASEL SPSEL<0:1> ASELP
ASEL
XSENSH
VINT VSS DWL TMFSEN VBLEQ
VINT VSS DWL TMFSEN VBLEQ
TMSSEN TMSAOFB PREB1 SEN SH
TMSSEN TMSAOFB PREB1 SEN SH
SENSH
XDWLGEN
VPP VINT VSS PREB2
VPP VINT VSS PREB2
RASEL SPSEL<0:1> PREB3 PB3EN DWL
RASEL SPSEL<0:1> PREB3 PB3EN DWL
DWLGEN
XISOEN
VINT VSS PREB1
VINT VSS PREB1
SEN TMEISO ISOEN
SEN TMEISO ISOEN
ISOEN
XISOGENL
VPP VINT VSS PREB4
VPP VINT VSS PREB4
PREB4LR ISOEN TMSAOFB ISOLR
PREB4L ISOEN TMSAOFB ISOL
ISOGEN
XISOGENR
VPP VINT VSS PREB4
VPP VINT VSS PREB4
PREB4LR ISOEN TMSAOFB ISOLR
PREB4R ISOEN TMSAOFB ISOR
ISOGEN
XFSETB
VINT VSS
VINT VSS
BABX YDELB FSETB
BAB YDELB FSETB
FSETB
XBR<0:9>
VINT VSS <*10>ASELP RAB<0:9>
VINT VSS ASELP RABX
BLKSEL FAPBX FAPX RAPBX RAPX
<*10>BLKSEL FAPB<0:9> FAP<0:9> RAPB<0:9> RAP<0:9>
BLKRBUF
XSPRBLK
VINT VSS TMRDOFF FSETB
VINT VSS TMRDOFF FSETB
FAP<0:9> FAPB<0:9> RAB99 SX<0:7>
FAP<0:9> FAPB<0:9> RAB99 SX<0:7>
SPRBLK
XPXSEL<0:3>
VPP VINT VSS <*4>PREB2 <*4>RASEL
VPP VINT VSS PREB2 RASEL
RAP1 RAP0 SPSEL<0:1> SX<0,4> PXSEL
RAPB<1,1>,RAP<1,1> <*2>(RAPB<0>,RAP<0>) <*4>SPSEL<0:1> SX<0,4,1,5,2,6,3,7> PXSEL<0:3>
PXSEL
XPHIX<0:3>
VPP VINT VSS
VPP VINT VSS
VNWL PXSEL PHIX PXB
<*4>VNWL PXSEL<0:3> PHIX<0:3> PXB<0:3>
PHIX
NEED SPECIAL ZRDARY FOR SPICE
XZRDARY
VPP VINT VSS PREB3 PREB1 RAP<2:9> RAPB<2:9>
VPP VINT VSS PREB3 PREB1 RAP<2:9> RAPB<2:9>
PXB<0:3> PHIX<0:3> SPSEL<0:1> RASEL WL0 WL1 VNWL
PXB<0:3> PHIX<0:3> SPSEL<0:1> RASEL WL0G WL1G VNWL
RDARY
11 TMWLTB TMWLTG
12 TMEISO TMEISO
13 TMSAOFB TMSAOFB
14 RAB99 RAB99
15 TMRDOFF TMRDOFF
16 RAB<0:9> RAB<0:9>
17 PREB4L PREB4L
18 PREB4R PREB4R
19 TMFSEN TMFSEN
20 TMSSEN TMSSEN
7 BAB BAB
8 YDELB YDELB
9 R10 R10
10 R11 R11
<OUT>
TO L&R NEIGHBORS
21 PREB4 PREB4
22 WL0G WL0G
23 WL1G WL1G
24 SH SH
25 SEN SEN
26 ISOL ISOL
27 ISOR ISOR
VBLH
CPARV1
10F
1 VPP VPP
2 VINT VINT VINT
3 VSS VSS
4 VBLEQ VBLEQ
5 VBLH VBLH
6 VNWL VNWL
PLACED IN ZBANK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
SPICE VERSION OF 1K ROW BLOCK
Size B
Document Number ZROW1K
REV A
Date: September 21, 2001
Sheet 1 of 1



PLACED IN ZBANK
PLACED IN ZROW1K

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	SPICE - RDEC ARRAY	
Size A	Document Number ZRDARY	REV A
Date: August 2, 2001	Sheet 1 of 1	



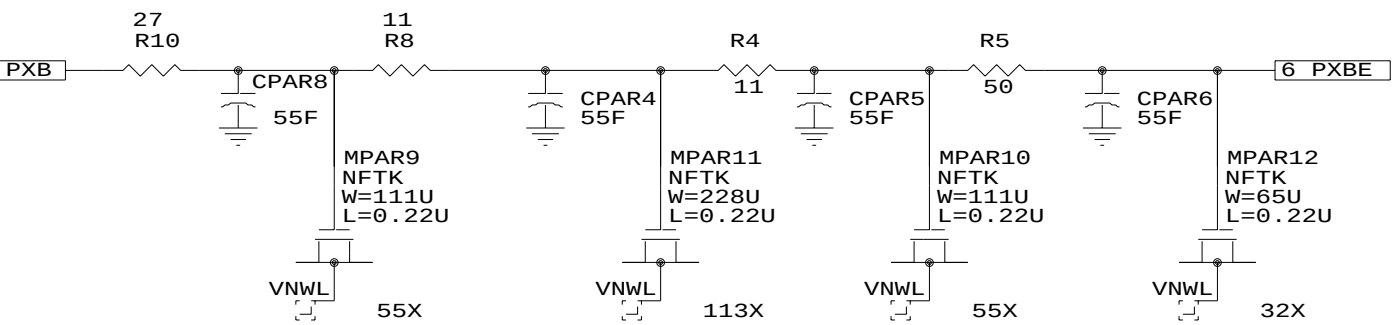
4 SEGMENTS
(SEG AT BL TWIST)

L=76 um/segment

M0=1.56 OHM/SQ
W=1.64U
R=~73 OHMS/seg ??

M2=.042 OHM/SQ
W=1.4U
R~2.3 OHMS/seg ??

AD=2.1P/RDEC
PD=0.6U/RDEC

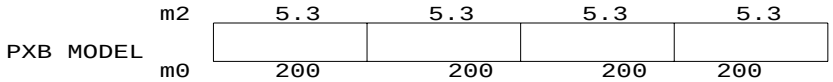


4 SEGMENTS
(SEG AT BL TWIST)

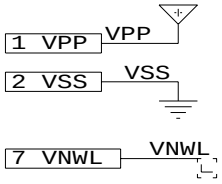
M0=1.56 OHM/SQ
W=0.6U
R=~200 OHMS/SEG ??

M2=.042 OHM/SQ
W=0.6U
R~5.3 OHMS/SEG ??

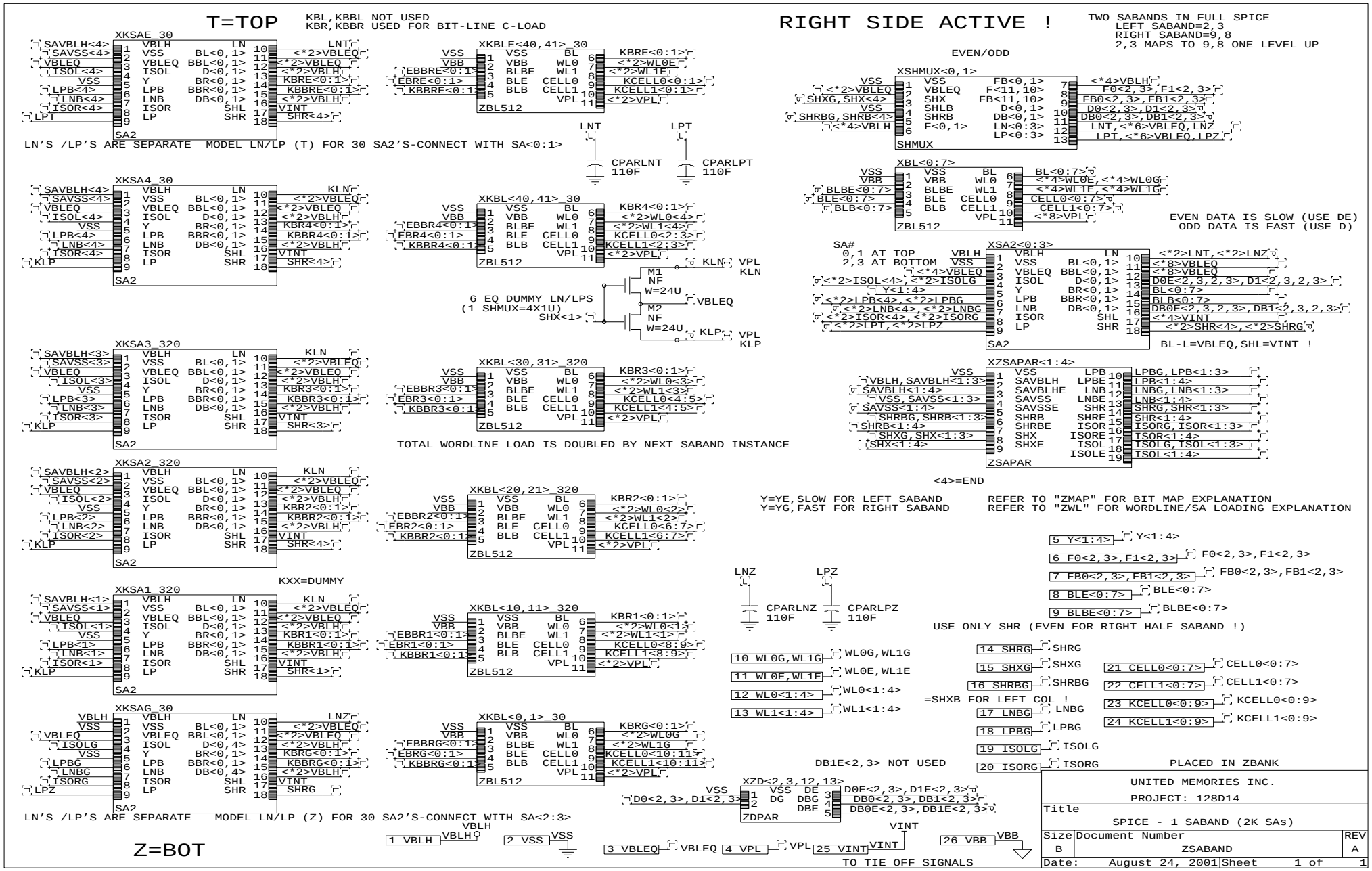
W=2.02U/PCH



PLACED IN ZBANK
PLACED IN ZROW1K
PLACED IN ZRDARY



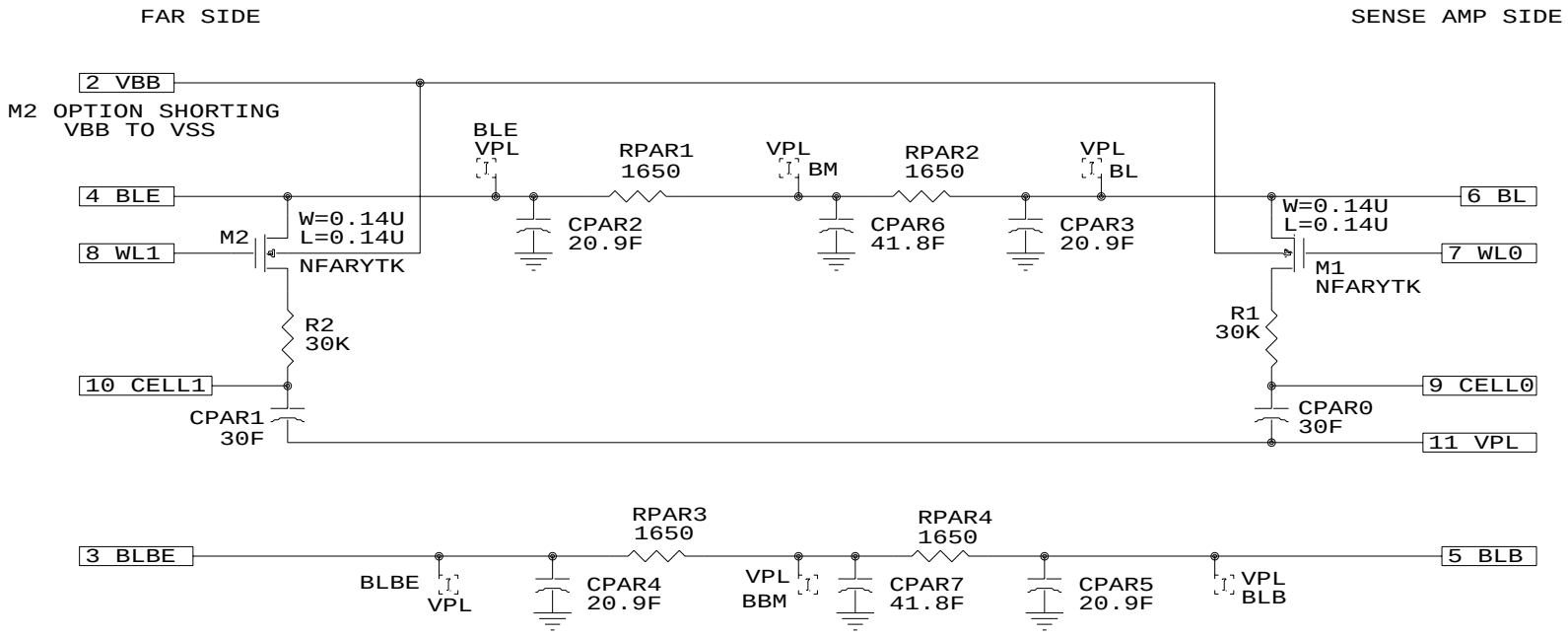
UNITED MEMORIES INC. PROJECT: 128D14		
Title SPICE LOADS FOR PHIX AND PXB		
Size A	Document Number ZLPHIX	REV A
Date: November 7, 2001	Sheet 1 of 1	


T=TOP
KBL,KBBL NOT USED
KBR,KBBR USED FOR BIT-LINE C-LOAD
RIGHT SIDE ACTIVE !
TWO SABANDS IN FULL SPICE
LEFT SABAND=2,3
RIGHT SABAND=9,8
2,3 MAPS TO 9,8 ONE LEVEL UP
EVEN/ODD
XKSAE_30
XKBLE<40,41>_30
XSHMUX<0,1>
LN'S /LP'S ARE SEPARATE MODEL LN/LP (T) FOR 30 SA2'S-CONNECT WITH SA<0:1>
CPARLNT 110F
CPARLPT 110F
XKSA4_30
XKBL<40,41>_30
XBL<0:7>
EVEN DATA IS SLOW (USE DE)
ODD DATA IS FAST (USE D)
SA#
0,1 AT TOP
2,3 AT BOTTOM
XSA2<0:3>
6 EQ DUMMY LN/LPS
(1 SHMUX=4X1U)
BL-L=VBLEQ,SHL=VINT !
XKSA3_320
XKBL<30,31>_320
XZSAPAR<1:4>
TOTAL WORDLINE LOAD IS DOUBLED BY NEXT SABAND INSTANCE
XKSA2_320
XKBL<20,21>_320
<4>=END
Y=YE,SLOW FOR LEFT SABAND
Y=YG,FAST FOR RIGHT SABAND
REFER TO "ZMAP" FOR BIT MAP EXPLANATION
REFER TO "ZWL" FOR WORDLINE/SA LOADING EXPLANATION
KXX=DUMMY
XKSA1_320
XKBL<10,11>_320
LNZ
LPZ
CPARLNZ 110F
CPARLPZ 110F
USE ONLY SHR (EVEN FOR RIGHT HALF SABAND !)
=SHXB FOR LEFT COL !
PLACED IN ZBANK
XKSAG_30
XKBL<0,1>_30
DB1E<2,3> NOT USED
XZD<2,3,12,13>
LN'S /LP'S ARE SEPARATE MODEL LN/LP (Z) FOR 30 SA2'S-CONNECT WITH SA<2:3>
Z=BOT
TO TIE OFF SIGNALS
UNITED MEMORIES INC.
PROJECT: 128D14
Title
SPICE - 1 SABAND (2K SAs)
Size B
Document Number ZSABAND
REV A
Date: August 24, 2001
Sheet 1 of 1

SET .IC=VPL FOR CONVERGENCE

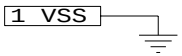
BL RESISTANCE USES 1.56 OHMS/SQ, (WORST CASE R) W=.14U, L=296U (512 CELLS/BL)

BL CAP ASSUMES SOLID SHEET OF M1 ON TOP AND SOLID SHEET OF
GC ON BOTTOM AND WC THICKNESSES (0.172FF/U) FOR INTERCONNECT
PASS GATE TRANSISTOR'S CAP ARE INCLUDED WITH THE INTERCONNECT CAP

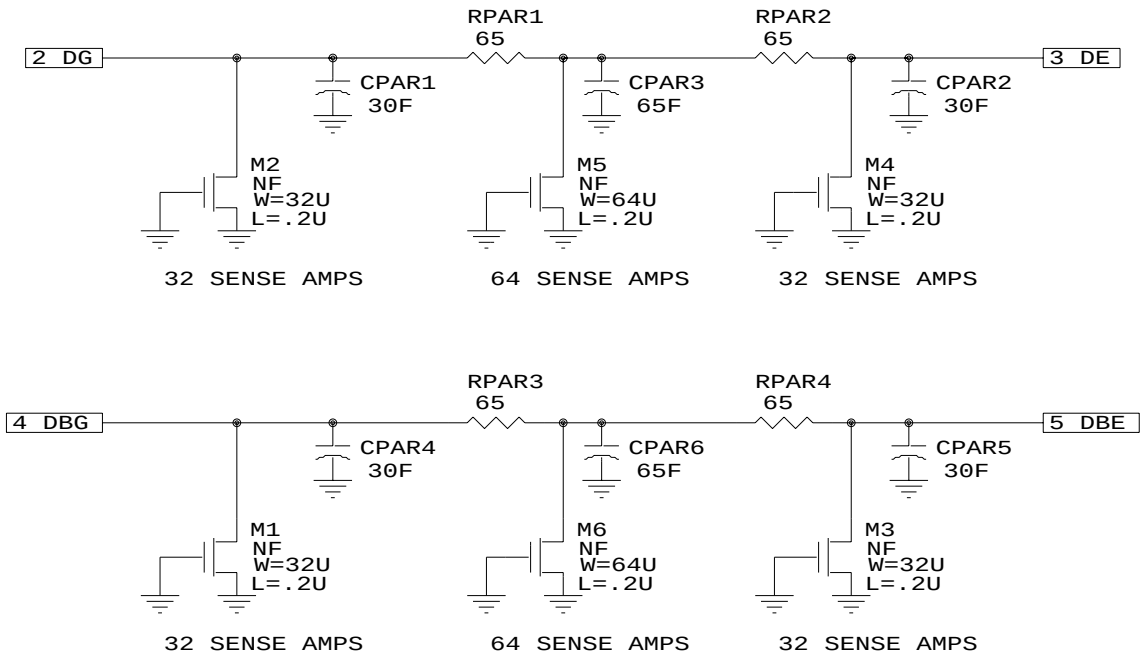


C JUNC, C OVERLAP, AND C PLUG ARE STILL PENDING S14 INFO

PLACED IN ZSABAND



United Memories Inc. PROJECT: 128D14		
Title BIT LINE PAIR (512 CELLS/BL= 1024WL/BL)		
Size A	Document Number ZBL512	REV A
Date: August 2, 2001	Sheet 1 of 1	



M1 LINES IN HQSA

W/L=DRAWN

W=0.34U
L=302U (1/8 OF ARRAY HEIGHT)
M1=.14 OHM/SQ

NEED PA AND PD?

D<0>=102FF
DB<0>=125FF

D<1>=90FF
DB<1>=90FF

IMBALANCE EXISTS TO REDUCE D/DB MUTUAL COUPLING.
THERFORE WORST CASE C (125FF) USED FOR SENSING.

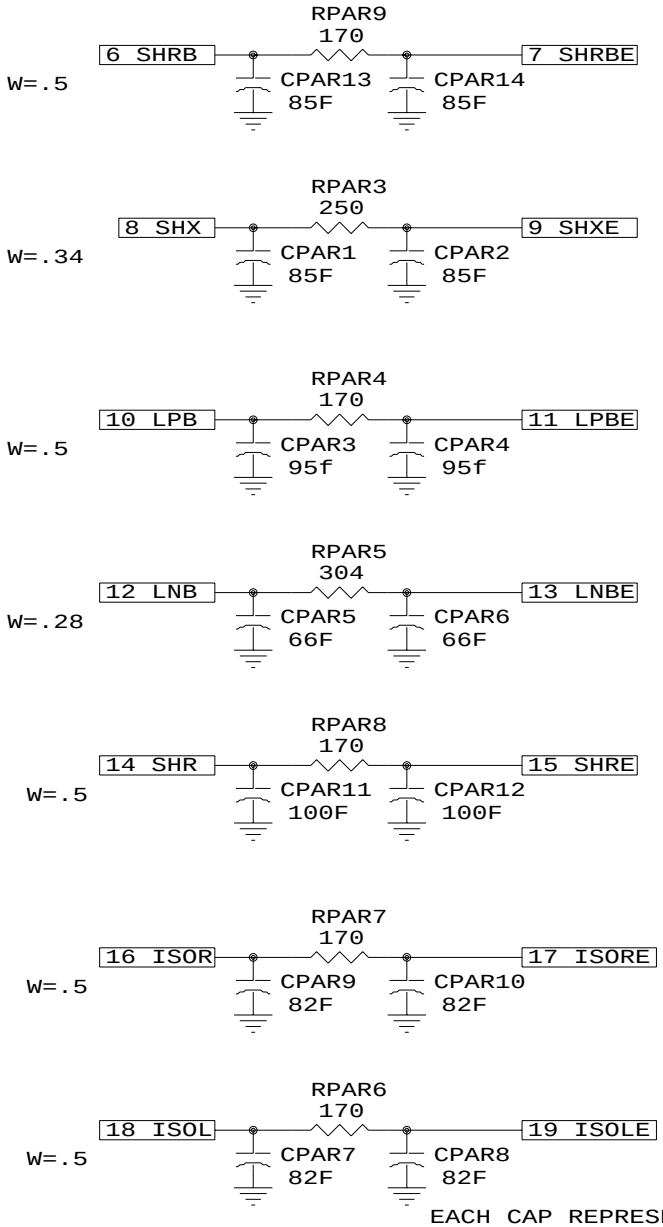
EACH D-LINE HAS 128 TOTAL SA'S

(ONLY 2 IN SPICE)

PLACED IN ZBANK
PLACED IN ZSABAND

1 VSS VSS

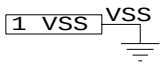
UNITED MEMORIES INC. PROJECT: 128D14		
Title LOCAL D-LINE (IN Sense Amp) Parasitics		
Size A	Document Number ZDPAR	REV A
Date: October 5, 2001	Sheet 1 of 1	

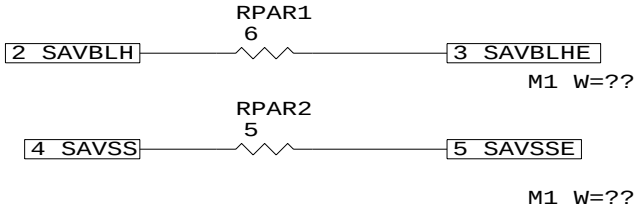


EACH CAP REPRESENTS 1/8 OF EXTRACTED VALUE

SHRB=SHXB FOR LEFT COL

SHRB=SHRB FOR RIGHT COL





EQUIVALENT NETWORK OF X&Y
HOPEFULLY BASED ON WORST CASE,ARRAY CENTER ACCES

M1 LINES IN FULL SABAND

W/L=DRAWN

L TOTAL=~ 304*8=2432

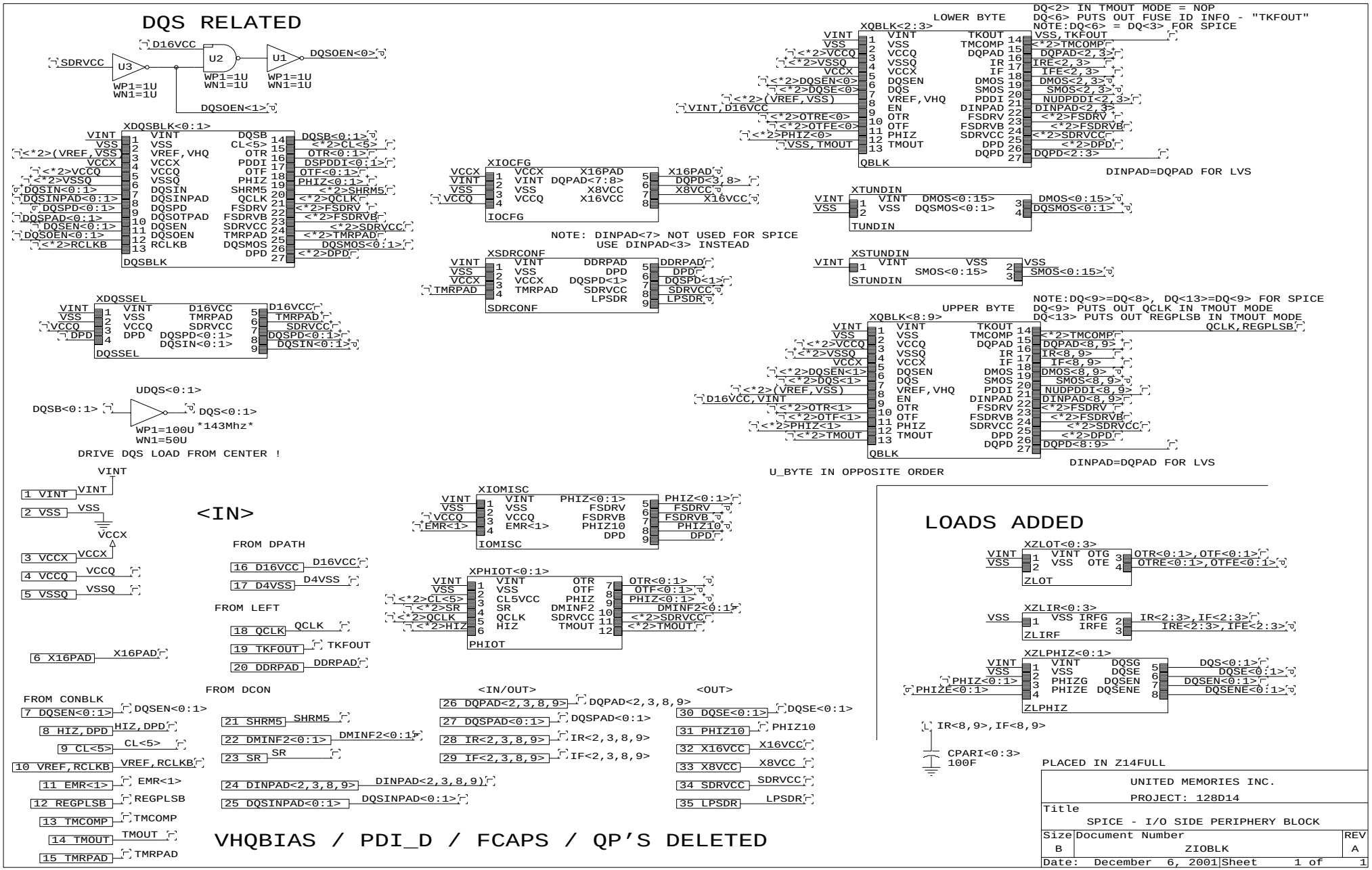
THEREFORE, L THIS PAGE=2432/4=608U

THIS IS PLACED FOUR TIMES FOR EACH SABAND !

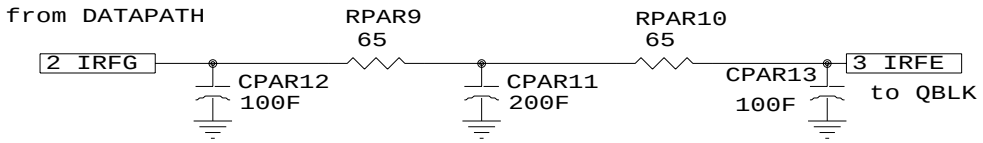
LN/LP BUSES NOT MODELED,LOCAL TO 64 SENSE-AMPS

PLACED IN ZBANK
PLACED IN ZSABAND

UNITED MEMORIES INC. PROJECT: 128D14		
Title Sense Amp Band Parasitics (SPICE)		
Size A	Document Number ZSAPAR	REV A
Date: October 5, 2001	Sheet 1 of 1	


DQS RELATED
D16VCC
SDRVCC
U3
U2
U1
DQSOEN<0>
WP1=1U
WN1=1U
DQSOEN<1>
XDQSBLK<0:1>
VINT
VSS
<*2>(VREF,VSS)
VCCX
<*2>VCCQ
<*2>VSSQ
DQSIN<0:1>
DQSINPAD<0:1>
DQSPD<0:1>
DQSPAD<0:1>
DQSEN<0:1>
DQSOEN<0:1>
<*2>RCLKB
VREF,VHQ
VCCQ
DQSOTPAD
RCLKB
DQSB
CL<5>
OTR
PDDI
OTF
PHIZ
SHRM5
QCLK
FSDRV
FSDRVB
SDRVCC
TMRPAD
DQSMOS
DPD
DQSB<0:1>
<*2>CL<5>
OTR<0:1>
DSPDDI<0:1>
OTF<0:1>
PHIZ<0:1>
<*2>SHRM5
<*2>QCLK
<*2>FSDRV
<*2>FSDRVB
<*2>SDRVCC
<*2>TMRPAD
DQSMOS<0:1>
<*2>DPD
DQSBLK
XIOCFG
VCCX
VINT
VSS
VCCQ
X16PAD
DQPAD<7:8>
X8VCC
X16VCC
DQPD<3,8>
IOCFG
NOTE: DINPAD<7> NOT USED FOR SPICE
USE DINPAD<3> INSTEAD
XSDRCONF
DDRPAD
DPD
DQSPD<1>
SDRVCC
LPSDR
TMRPAD
SDRCONF
XDQSSEL
D16VCC
TMRPAD
SDRVCC
DQSPD<0:1>
DQSIN<0:1>
DQSSEL
UDQS<0:1>
DQSB<0:1>
DQS<0:1>
WP1=100U
143Mhz
WN1=50U
DRIVE DQS LOAD FROM CENTER !
<IN>
FROM DPATH
16 D16VCC
17 D4VSS
FROM LEFT
18 QCLK
19 TKFOUT
20 DDRPAD
6 X16PAD
FROM CONBLK
7 DQSEN<0:1>
8 HIZ,DPD
9 CL<5>
10 VREF,RCLKB
11 EMR<1>
12 REGPLSB
13 TMCOMP
14 TMOUT
15 TMRPAD
FROM DCON
21 SHRM5
22 DMINF2<0:1>
23 SR
24 DINPAD<2,3,8,9>
25 DQSINPAD<0:1>
XIOMISC
EMR<1>
PHIZ<0:1>
PHIZ10
IOMISC
XPHIOT<0:1>
OTR
OTF
CL5VCC
DMINF2
SDRVCC
TMOUT
HIZ
PHIOT
<IN/OUT>
26 DQPAD<2,3,8,9>
27 DQSPAD<0:1>
28 IR<2,3,8,9>
29 IF<2,3,8,9>
<OUT>
30 DQSE<0:1>
31 PHIZ10
32 X16VCC
33 X8VCC
34 SDRVCC
35 LPSDR
VHQBIAS / PDI_D / FCAPS / QP'S DELETED
LOWER BYTE
XQBLK<2:3>
DQ<2> IN TMOUT MODE = NOP
DQ<6> PUTS OUT FUSE ID INFO - "TKFOUT"
NOTE:DQ<6> = DQ<3> FOR SPICE
TKOUT
VSS,TKFOUT
TMCOMP
DQPAD
IR
IF
DMOS
SMOS
PDDI
DINPAD
FSDRV
FSDRVB
SDRVCC
DPD
DQPD
QBLK
DINPAD=DQPAD FOR LVS
XTUNDIN
DMOS<0:15>
DQSMOS<0:1>
TUNDIN
XSTUNDIN
SMOS<0:15>
STUNDIN
NOTE:DQ<9>=DQ<8>, DQ<13>=DQ<9> FOR SPICE
DQ<9> PUTS OUT QCLK IN TMOUT MODE
DQ<13> PUTS OUT REGPLSB IN TMOUT MODE
UPPER BYTE
XQBLK<8:9>
QCLK,REGPLSB
DQ<8:9>
U_BYTE IN OPPOSITE ORDER
LOADS ADDED
XZLOT<0:3>
OTG
OTE
OTR<0:1>,OTF<0:1>
OTRE<0:1>,OTFE<0:1>
ZLOT
XZLIR<0:3>
IRFG
IRFE
IR<2:3>,IF<2:3>
IRE<2:3>,IFE<2:3>
ZLIRF
XZLPHIZ<0:1>
DQSG
DQSE
PHIZG
DQSEN
PHIZE
DQSENE
DQS<0:1>
DQSE<0:1>
DQSEN<0:1>
DQSENE<0:1>
ZLPHIZ
IR<8,9>,IF<8,9>
CPARI<0:3>
100F
PLACED IN Z14FULL
UNITED MEMORIES INC.
PROJECT: 128D14
Title
SPICE - I/O SIDE PERIPHERY BLOCK
Size
B
Document Number
ZIOBLK
REV
A
Date: December 6, 2001
Sheet 1 of 1

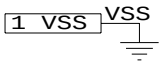
L=1800
W=0.6U (DRAWN)



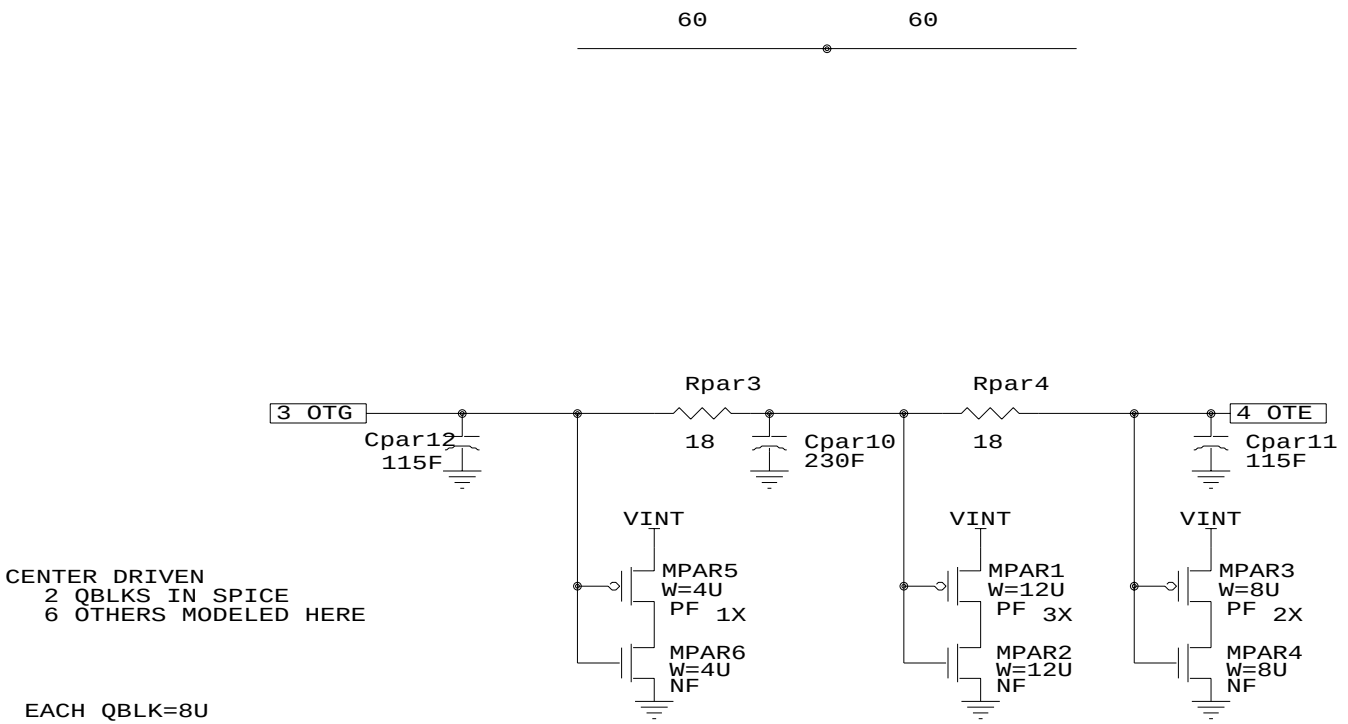
SLOW CASE

ALL GATE LOADS ARE ACCOUNTED FOR DIRECTLY!

PLACED IN ZIOBLK



UNITED MEMORIES LTD PROJECT: 128D14		
Title SPICE - IR / IF LINE PARAS		
Size A	Document Number ZLIRF	REV A
Date: October 12, 2001	Sheet 1 of 1	



CENTER DRIVEN
2 QBLKS IN SPICE
6 OTHERS MODELED HERE

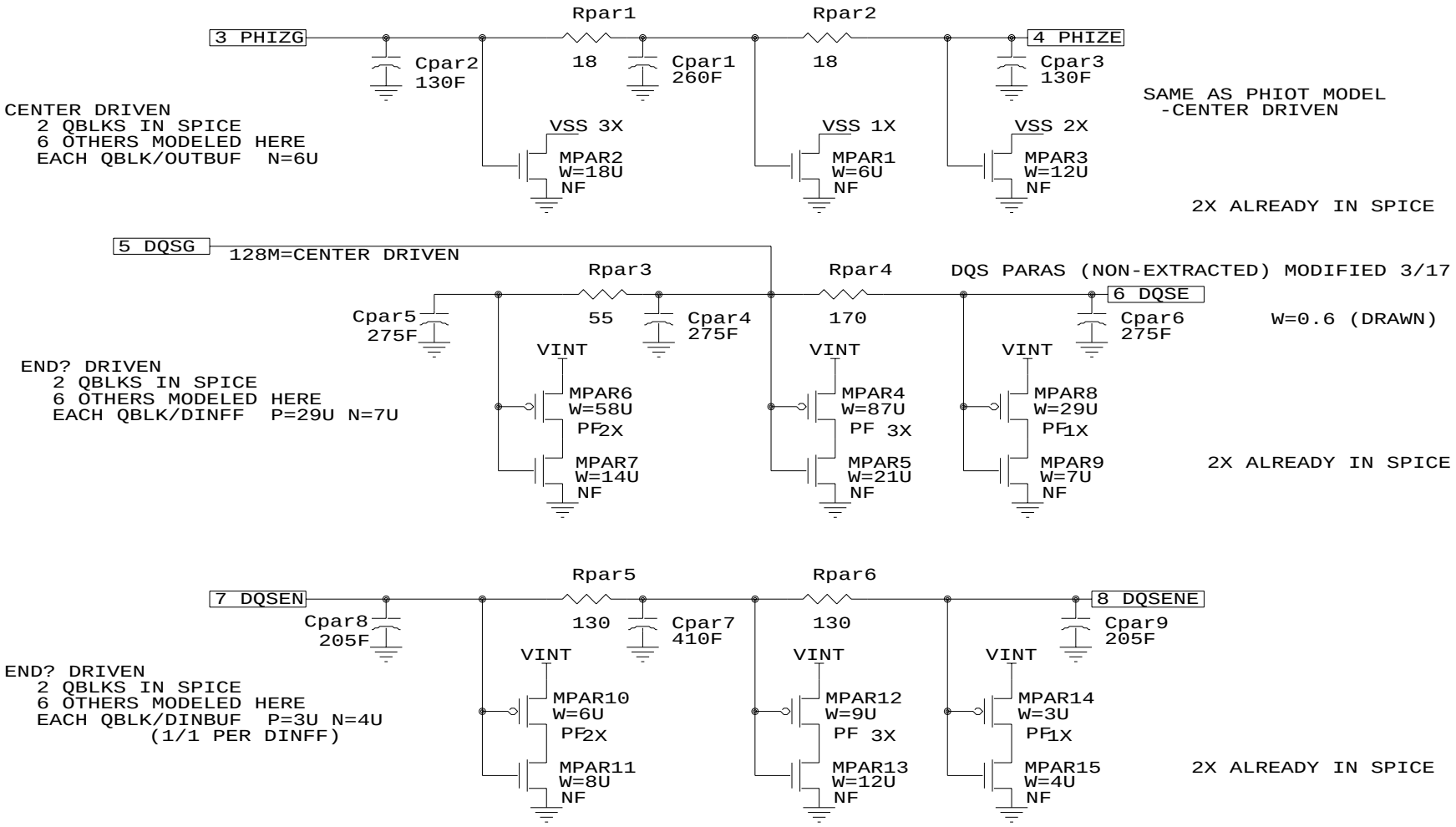
EACH QBLK=8U

OTR/OTF HAVE SAME TOTAL
**NOT THE SAME P/N RATIO

2X ALREADY IN SPICE

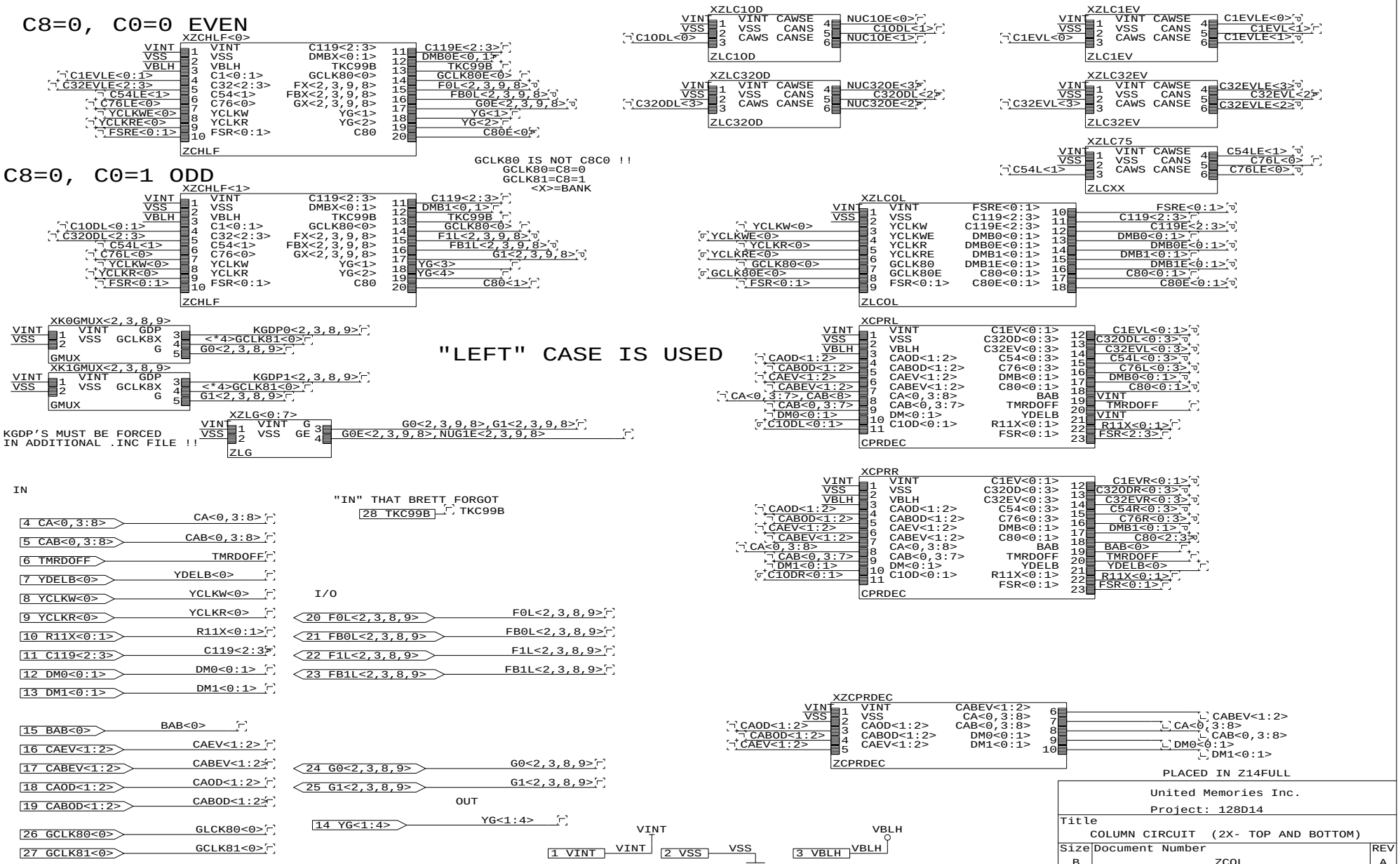
PLACED IN ZIOBLK

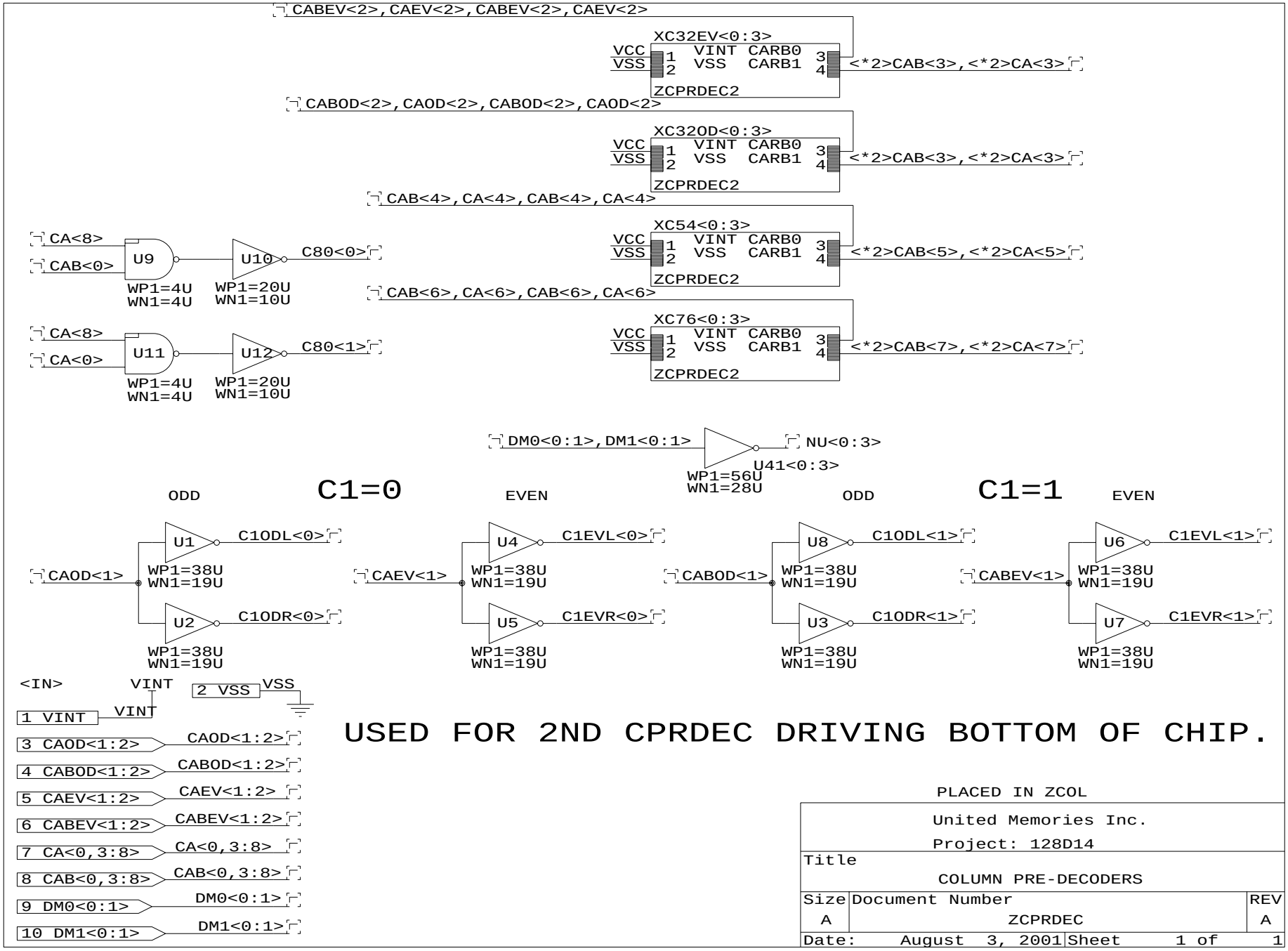
UNITED MEMORIES LTD PROJECT: 128D14		
Title SPICE- OTR AND OTF LOADS		
Size A	Document Number ZLOT	REV A
Date: October 16, 2001	Sheet 1 of 1	



PLACED IN ZIOBLK (2 TIMES)

UNITED MEMORIES LTD PROJECT: 128D14		
Title SPICE- PHIZ / DQS / DQSEN LOADS		
Size A	Document Number ZLPHIZ	REV A
Date: October 16, 2001	Sheet 1 of 1	

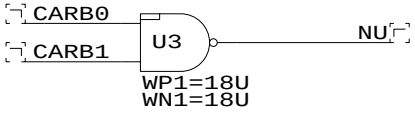

C8=0, C0=0 EVEN
XZCHLF<0>
ZCHLF
C8=0, C0=1 ODD
XZCHLF<1>
ZCHLF
GCLK80 IS NOT C8C0 !!
GCLK80=C8=0
GCLK81=C8=1
<X>=BANK
XZLC1OD
ZLC1OD
XZLC1EV
ZLC1EV
XZLC32OD
ZLC32OD
XZLC32EV
ZLC32EV
XZLC75
ZLCXX
XZLCOL
ZLCOL
XK0GMUX<2,3,8,9>
GMUX
XK1GMUX<2,3,8,9>
GMUX
XZLG<0:7>
ZLG
KGDP'S MUST BE FORCED
IN ADDITIONAL .INC FILE !!
"LEFT" CASE IS USED
XCPRL
CPRDEC
XCPRR
CPRDEC
IN
"IN" THAT BRETT FORGOT
28 TKC99B
TKC99B
I/O
OUT
XZCPRDEC
ZCPRDEC
PLACED IN Z14FULL
United Memories Inc.
Project: 128D14
Title
COLUMN CIRCUIT (2X- TOP AND BOTTOM)
Size B
Document Number ZCOL
REV A
Date: December 4, 2001
Sheet 1 of 1

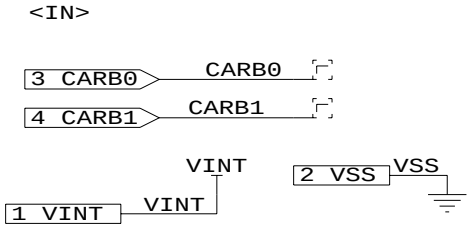


USED FOR 2ND CPRDEC DRIVING BOTTOM OF CHIP.

PLACED IN ZCOL

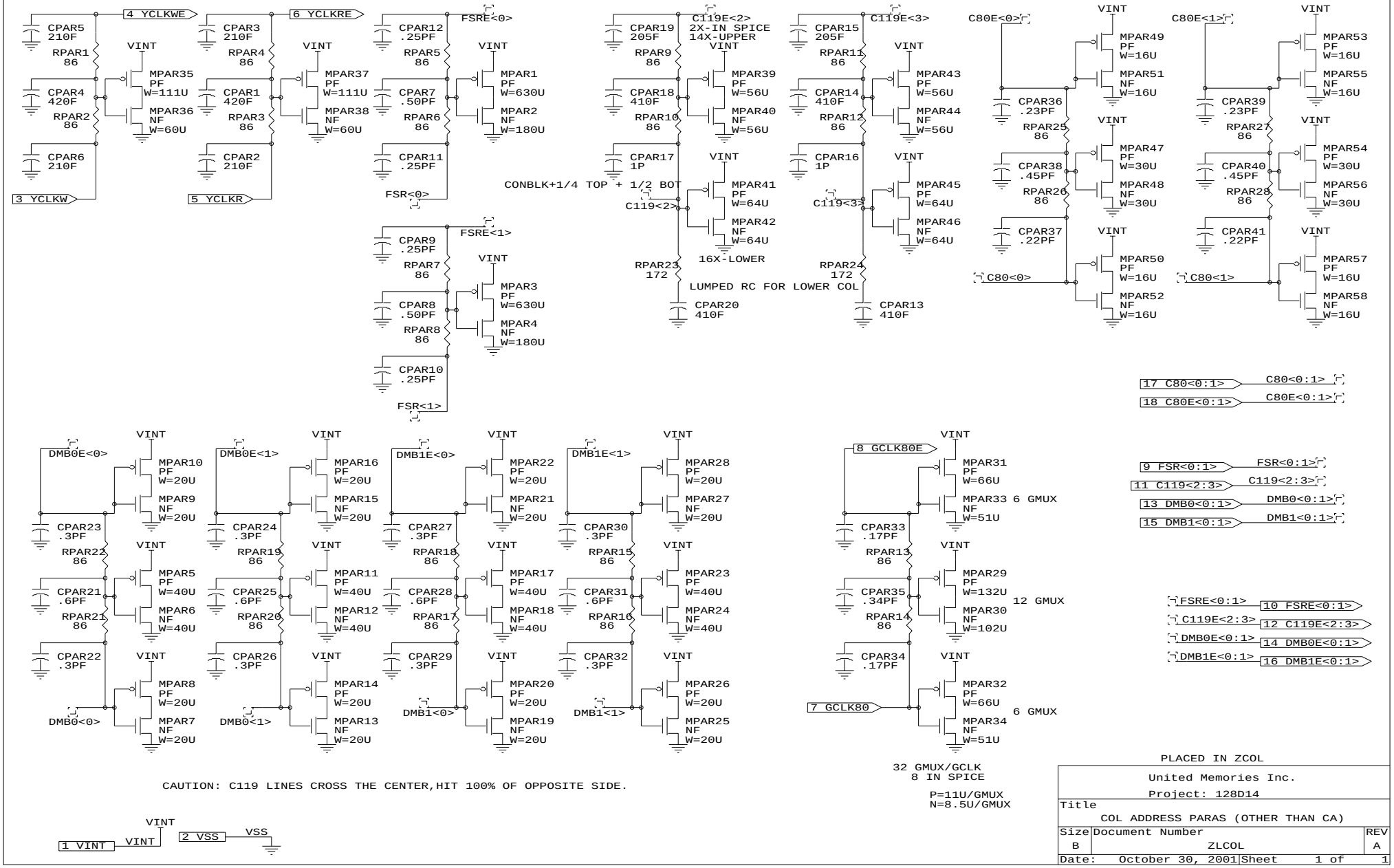
United Memories Inc.		
Project: 128D14		
Title		
COLUMN PRE-DECODERS		
Size	Document Number	REV
A	ZCPRDEC	A
Date: August 3, 2001	Sheet 1 of 1	





PLACED IN ZCPRDEC (4X)

United Memories Inc. Project: 128D14		
Title COLUMN PRE-DECODER LOGIC		
Size A	Document Number ZCPRDEC2	REV A
Date: August 24, 2001	Sheet 1 of 1	

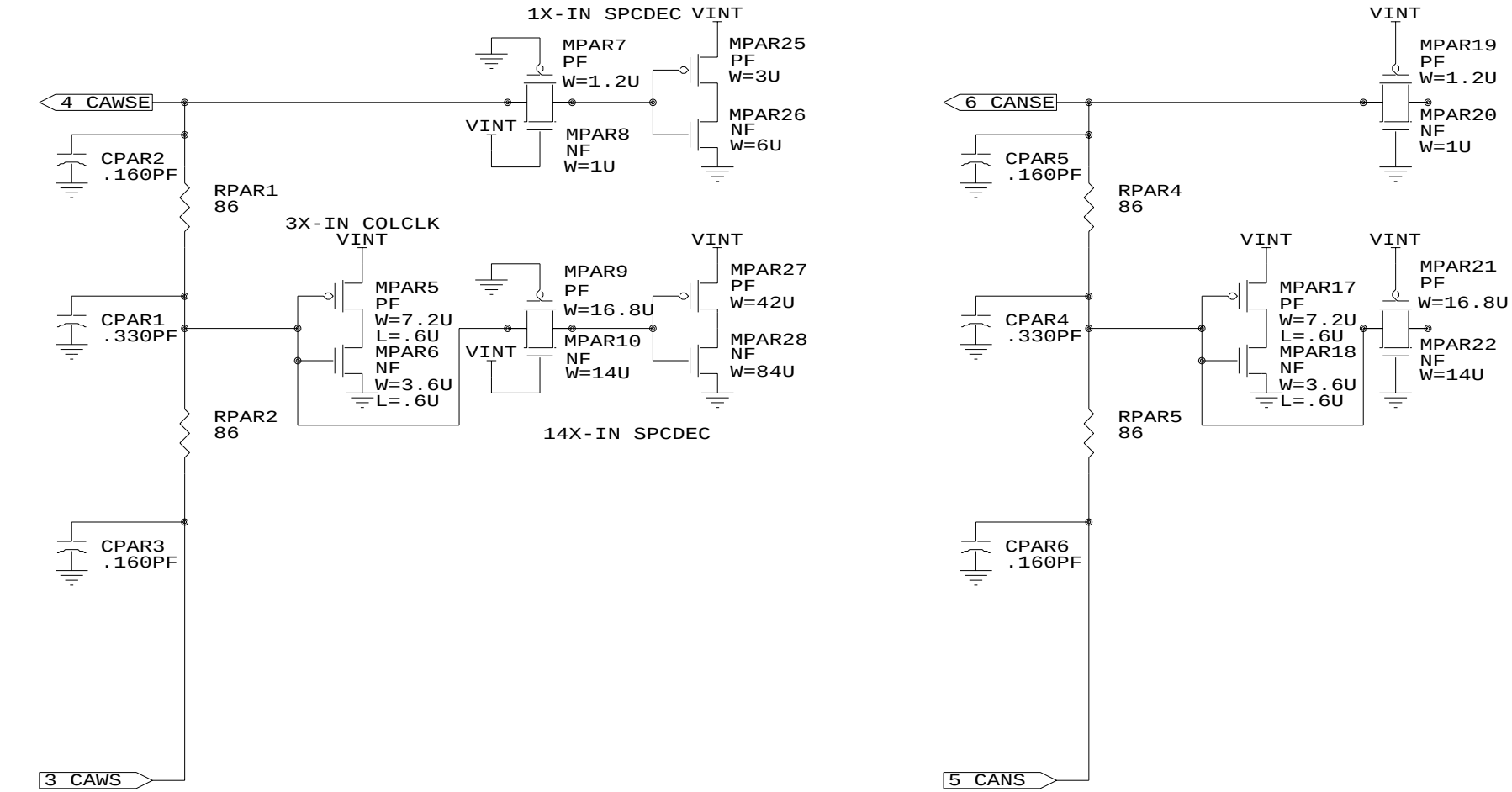


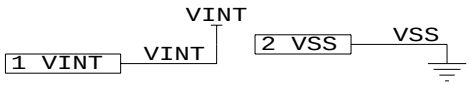
PLACED IN ZCOL

United Memories Inc.

Project: 128D14

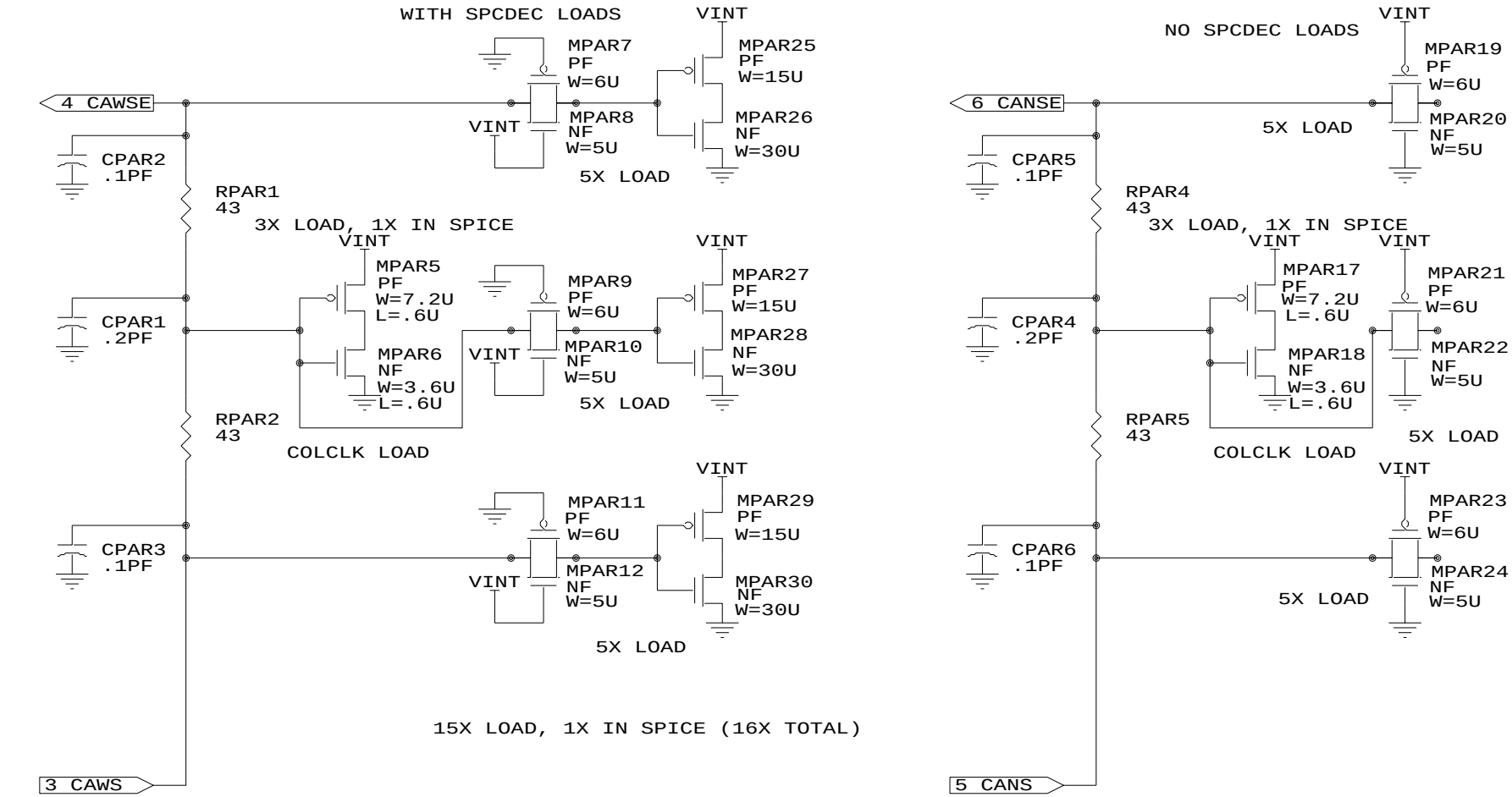
Title		
COL ADDRESS PARAS (OTHER THAN CA)		
Size B	Document Number ZLCOL	REV A
Date: October 30, 2001	Sheet 1 of 1	





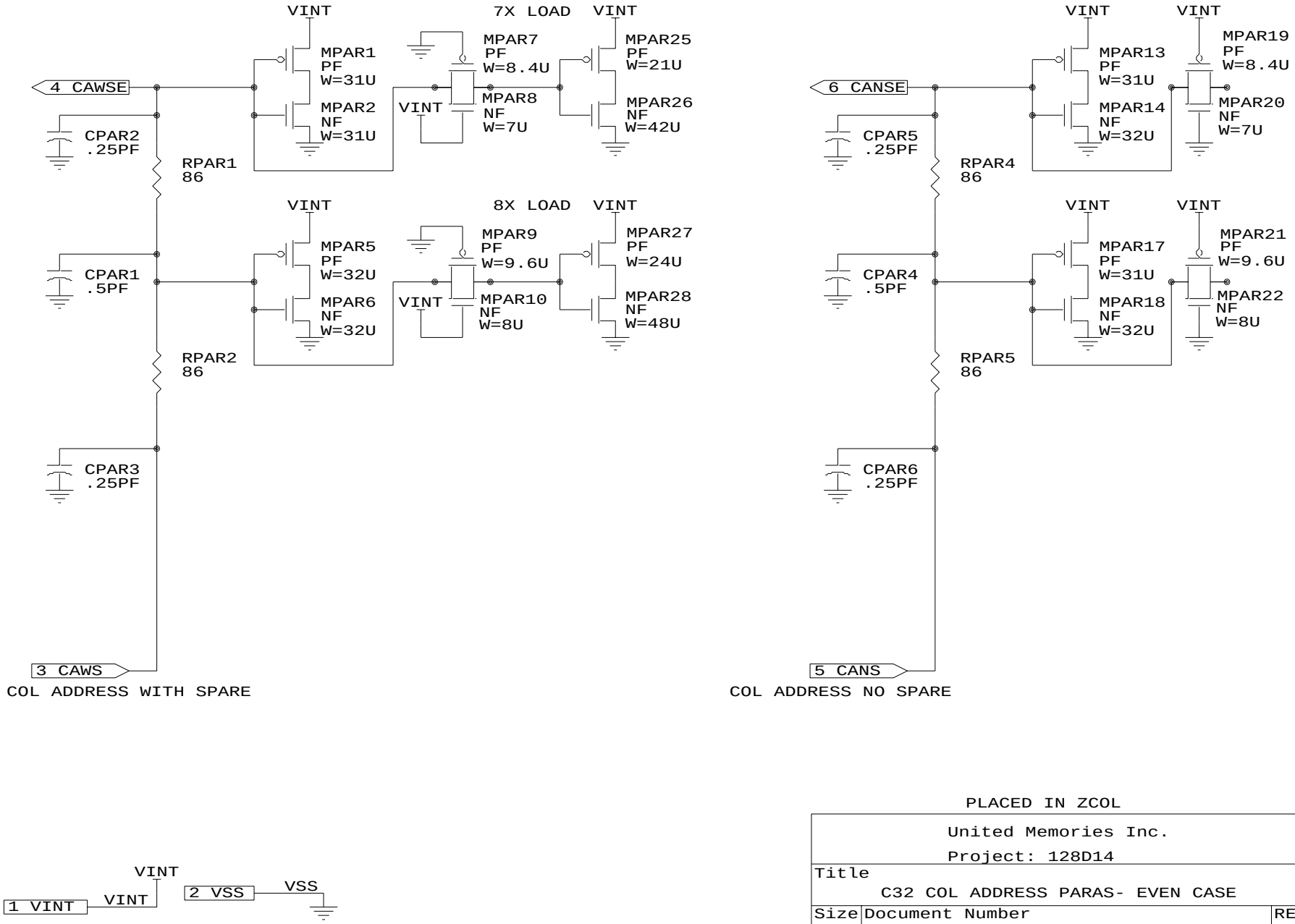
PLACED IN ZCOL

United Memories Inc. Project: 128D14		
Title COL ADDRESS PARAS (C1) EVEN		
Size A	Document Number ZLC1EV	REV A
Date: October 16, 2001	Sheet 1 of 1	



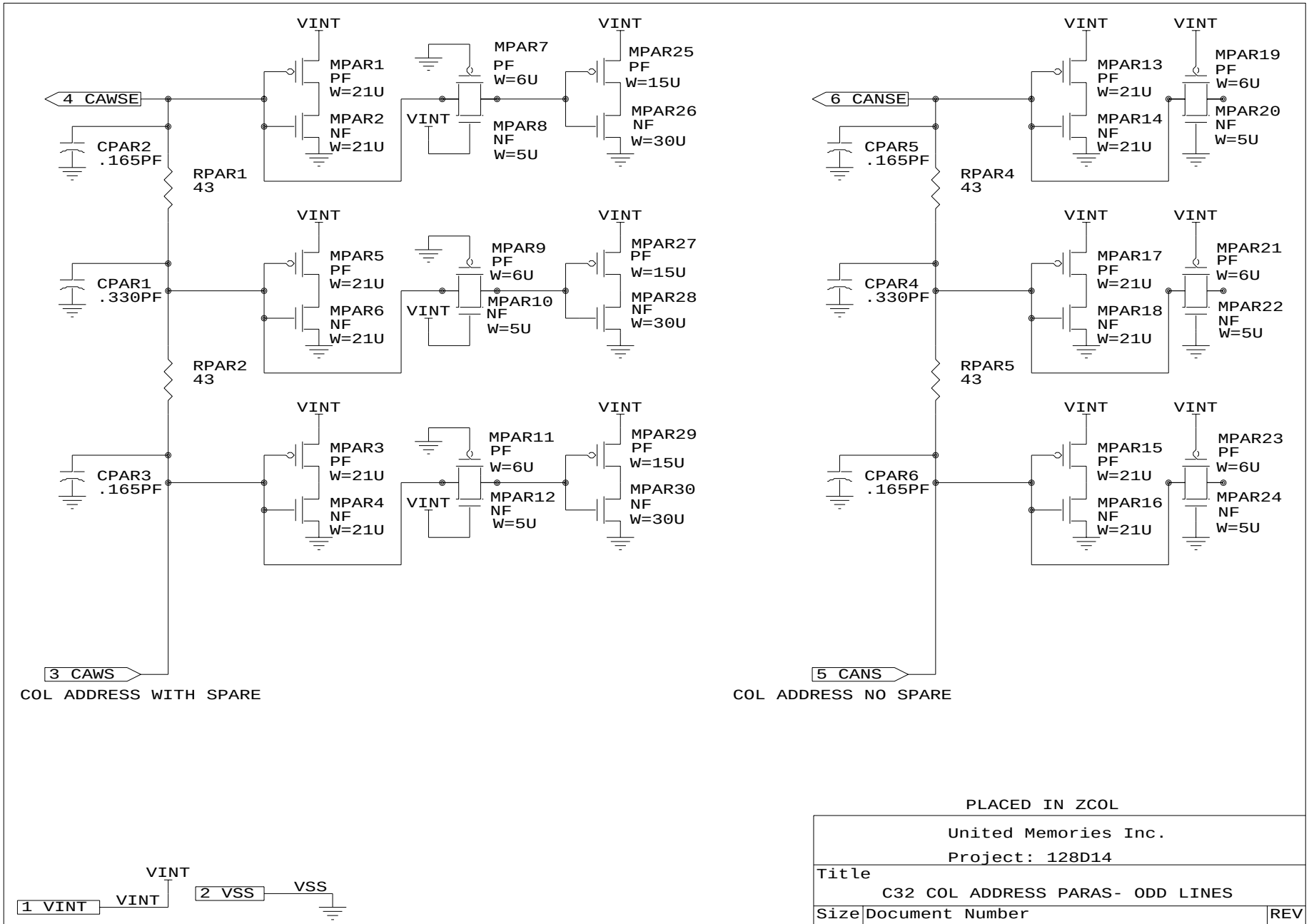
PLACED IN ZCOL

United Memories Inc.		
Project: 128D14		
Title		
COL ADDRESS PARAS (C1) ODD		
Size	Document Number	REV
A	ZLC10D	A
Date: October 16, 2001	Sheet 1 of 1	



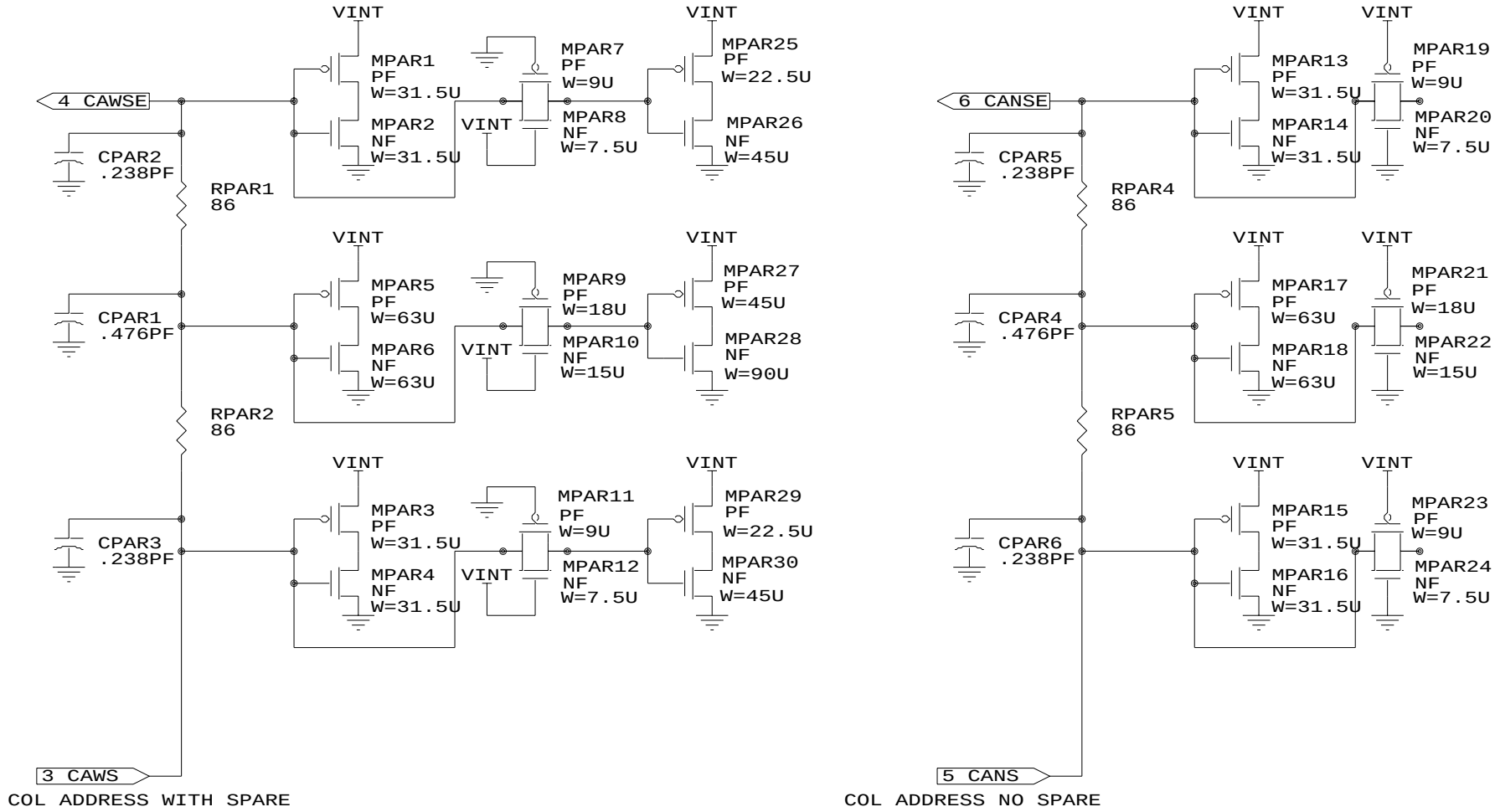
PLACED IN ZCOL

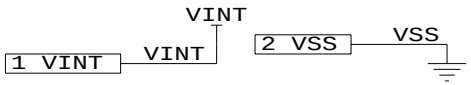
United Memories Inc. Project: 128D14		
Title C32 COL ADDRESS PARAS- EVEN CASE		
Size A	Document Number ZLC32EV	REV A
Date: October 16, 2001	Sheet 1 of 1	



PLACED IN ZCOL

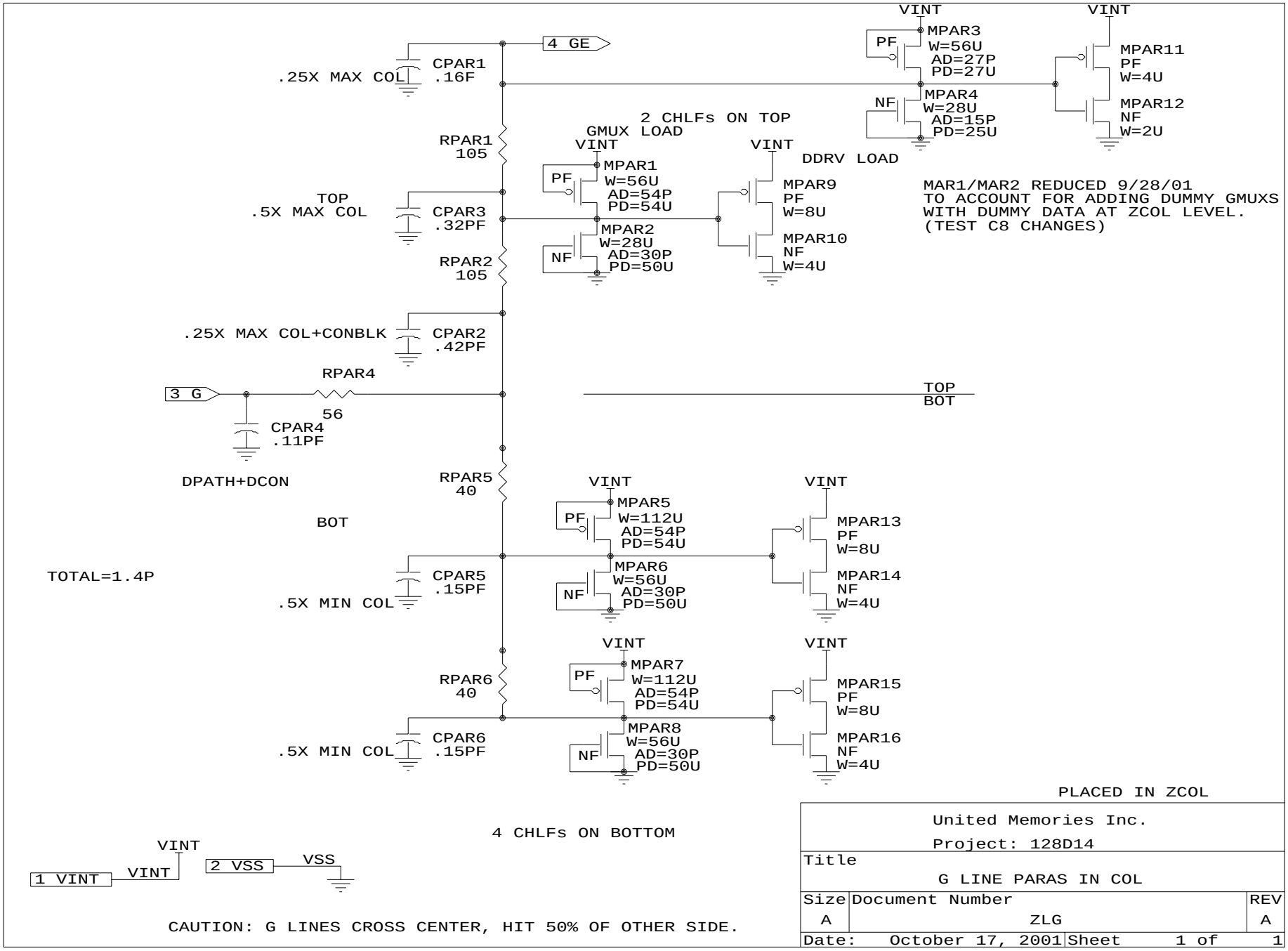
United Memories Inc. Project: 128D14		
Title C32 COL ADDRESS PARAS- ODD LINES		
Size A	Document Number ZLC32OD	REV A
Date: October 16, 2001	Sheet 1 of 1	

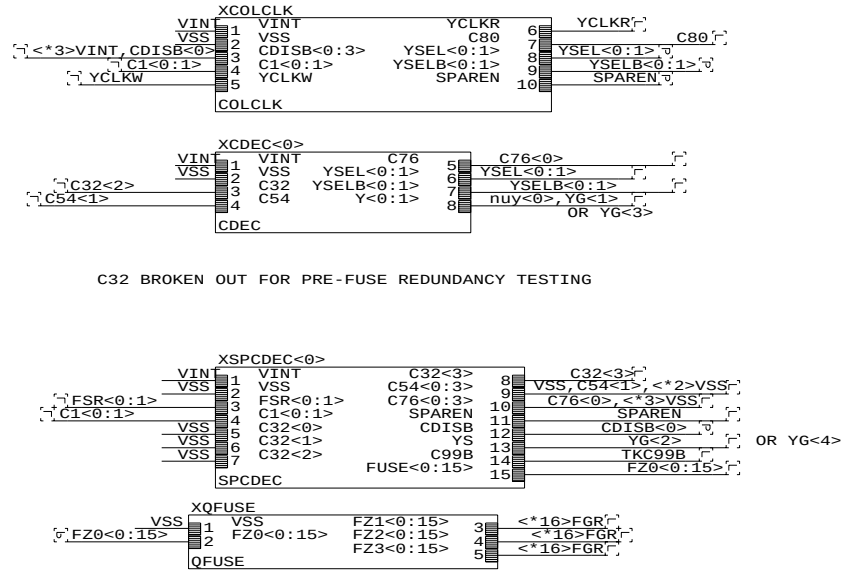




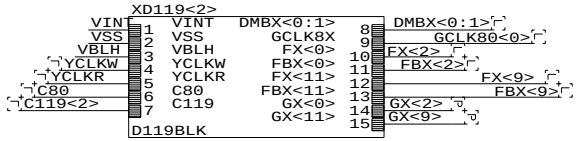
PLACED IN ZCOL

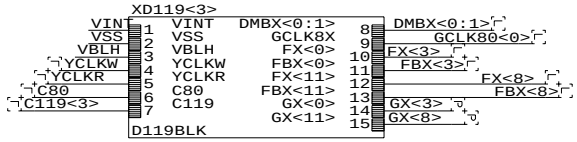
United Memories Inc.		
Project: 128D14		
Title C54/C76 COL ADDRESS PARAS (NO ODD/EVEN)		
Size A	Document Number ZLCXX	REV A
Date: September 1, 2001	Sheet 1 of 1	

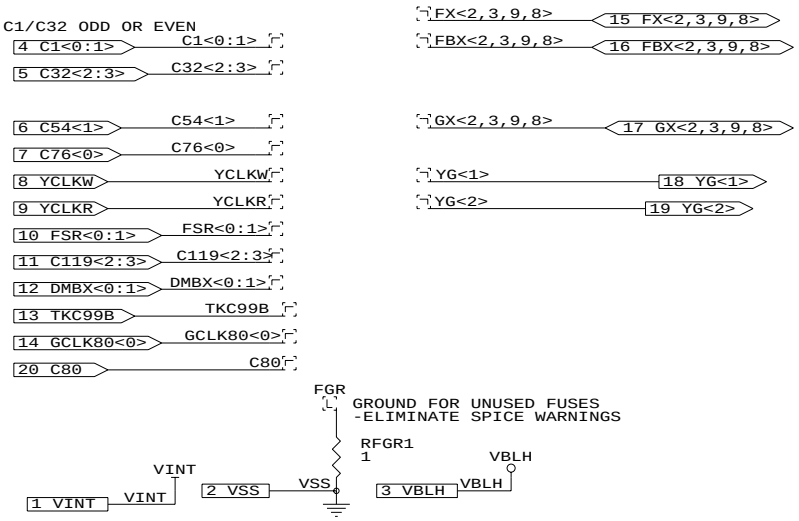

4 GE
CPAR1
.16F
.25X MAX COL
RPAR1
105
TOP
.5X MAX COL
CPAR3
.32PF
RPAR2
105
.25X MAX COL+CONBLK
CPAR2
.42PF
RPAR4
3 G
56
CPAR4
.11PF
DPATH+DCON
RPAR5
40
BOT
TOTAL=1.4P
CPAR5
.15PF
.5X MIN COL
RPAR6
40
CPAR6
.15PF
.5X MIN COL
VINT
MPAR3
PF
W=56U
AD=27P
PD=27U
MPAR4
NF
W=28U
AD=15P
PD=25U
MPAR11
PF
W=4U
MPAR12
NF
W=2U
2 CHLFs ON TOP
GMUX LOAD
MPAR1
PF
W=56U
AD=54P
PD=54U
MPAR2
NF
W=28U
AD=30P
PD=50U
DDRV LOAD
MPAR9
PF
W=8U
MPAR10
NF
W=4U
MAR1/MAR2 REDUCED 9/28/01
TO ACCOUNT FOR ADDING DUMMY GMUXS
WITH DUMMY DATA AT ZCOL LEVEL.
(TEST C8 CHANGES)
TOP
BOT
MPAR5
PF
W=112U
AD=54P
PD=54U
MPAR6
NF
W=56U
AD=30P
PD=50U
MPAR13
PF
W=8U
MPAR14
NF
W=4U
MPAR7
PF
W=112U
AD=54P
PD=54U
MPAR8
NF
W=56U
AD=30P
PD=50U
MPAR15
PF
W=8U
MPAR16
NF
W=4U
PLACED IN ZCOL
4 CHLFs ON BOTTOM
1 VINT
2 VSS
VSS
CAUTION: G LINES CROSS CENTER, HIT 50% OF OTHER SIDE.
United Memories Inc.
Project: 128D14
Title
G LINE PARAS IN COL
Size
A
Document Number
ZLG
REV
A
Date: October 17, 2001
Sheet 1 of 1



C32 BROKEN OUT FOR PRE-FUSE REDUNDANCY TESTING



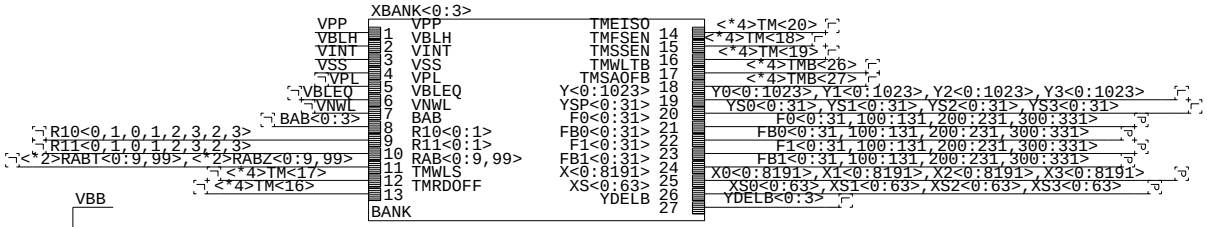


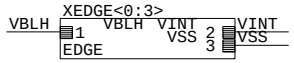


PLACED IN ZCOL

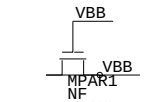
United Memories Inc.		
Project: 128D14		
Title	COLUMN HALF - SPICE	
Size B	Document Number ZCHLF	REV A
Date: December 4, 2001	Sheet 1 of 1	

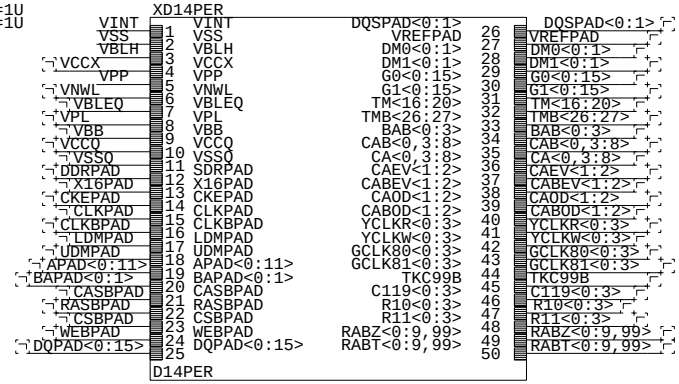
A0-REMOVED VPL PORT

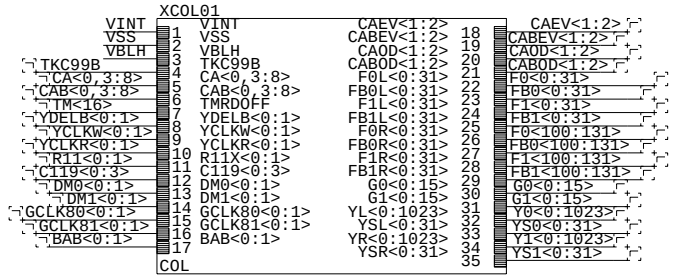




VBB GOES TO BANK AS WELL, NO LVS CONNECTION
EXCEPT ARRAY MEMORY CELL DEVICES!



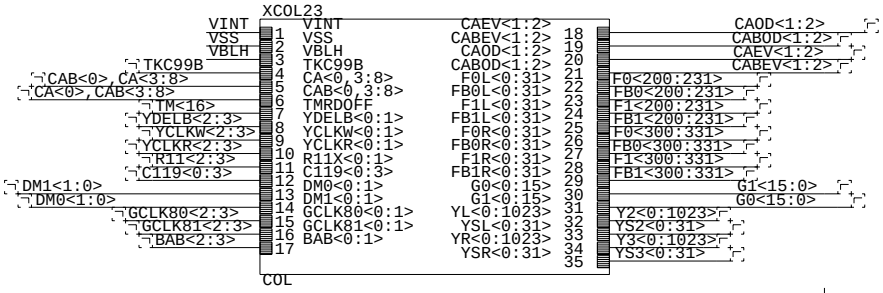


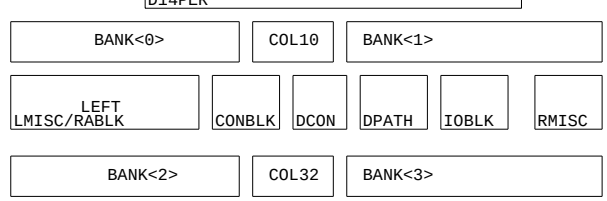


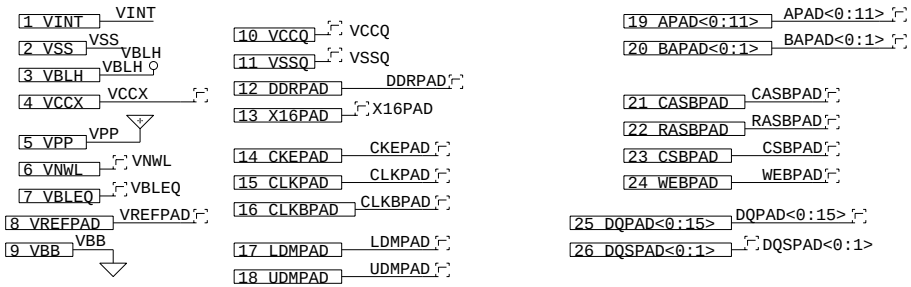
BOT COL PRGRAMMING

SWAP CO ADDRESS FOR BOTTOM(CA<0>,CAB<0>)
SWAP EVEN/ODD ADDRESSES FOR BOTTOM(C1,C32)
SWAP EVEN/ODD DATA FOR BOTTOM (G0,G1), PLUS UPPER/LOWER BYTES
SWAP EVEN/ODD MASKS FOR BOTTOM (DMB0,1), PLUS UPPER LOWER BYTES

NO CHANGE IN C119 ORDER FOR TOP AND BOTTOM !
THESE KEEPS DATA GENERATION IN SCRAMBLE EASY







	C119 <0>	<1>	<2>	<3>
L-BYTE	IO <0>	<1>	<2>	<3>
	IO <4>	<5>	<6>	<7>
U-BYTE	IO<11>	<10>	<9>	<8>
	IO<15>	<14>	<13>	<12>
	X8		X8 X4	

FOR X16 / ALL ON

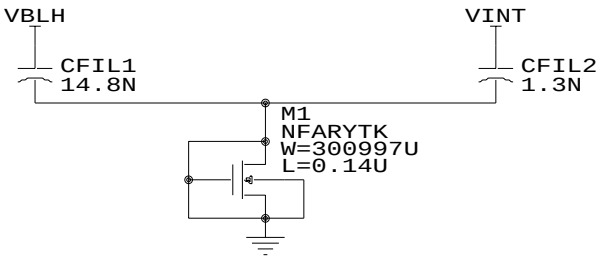
TOP G LINES:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BOT G LINES:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

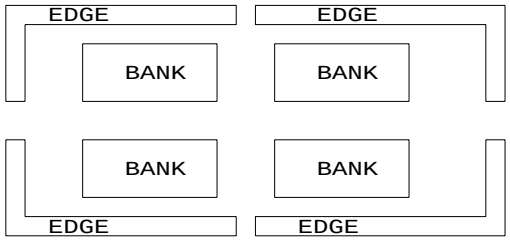
UNITED MEMORIES INC.
PROJECT: 128D14

Title
DDR/SDR - S14 TECH - FULL CHIP LVS

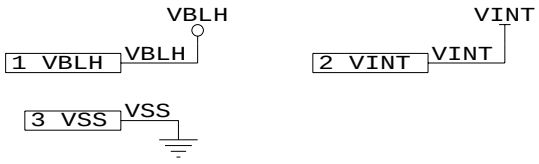
Size	Document Number	REV
B	D14CHIP	A0

Date: February 4, 2002 Sheet 1 of 1



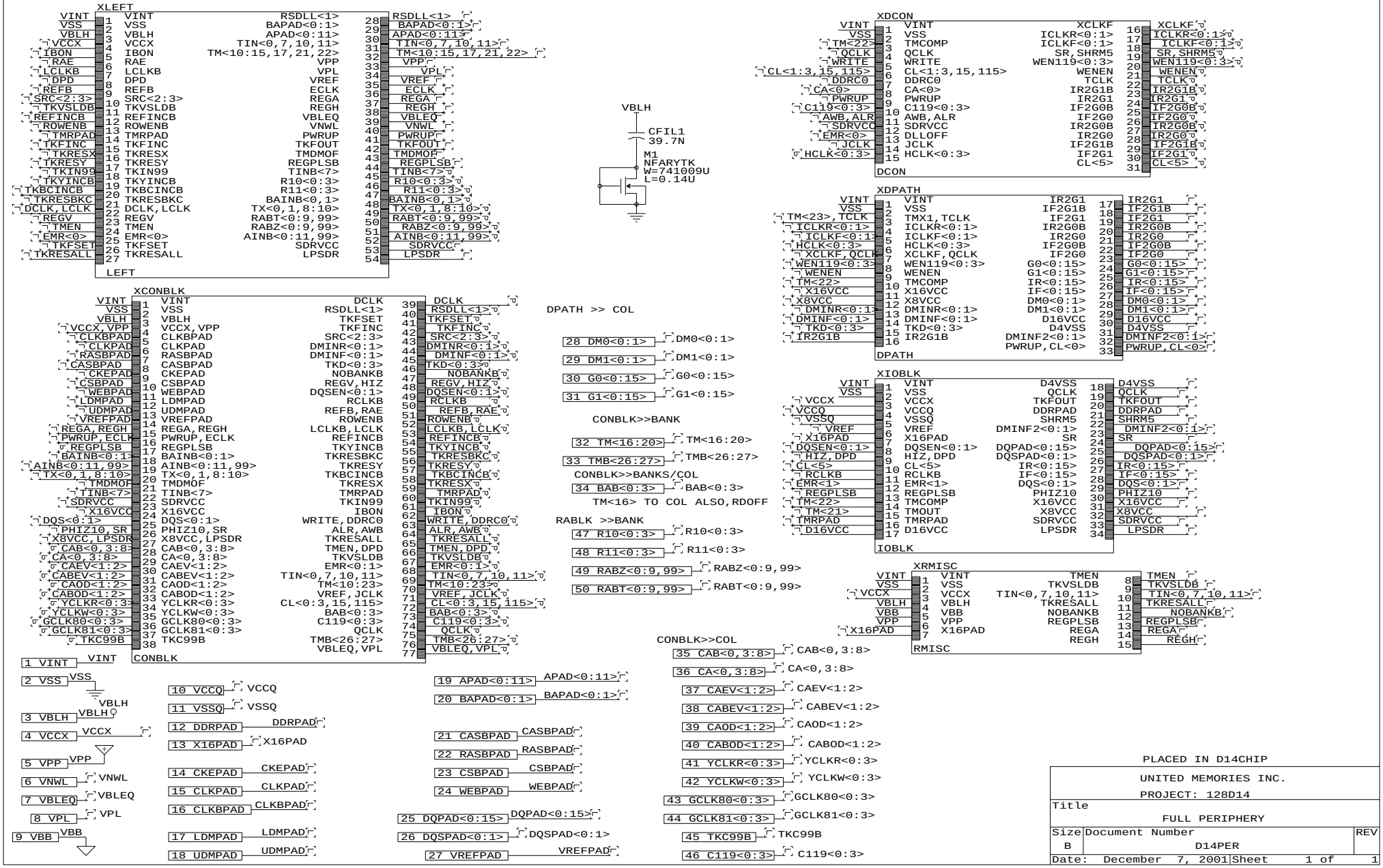


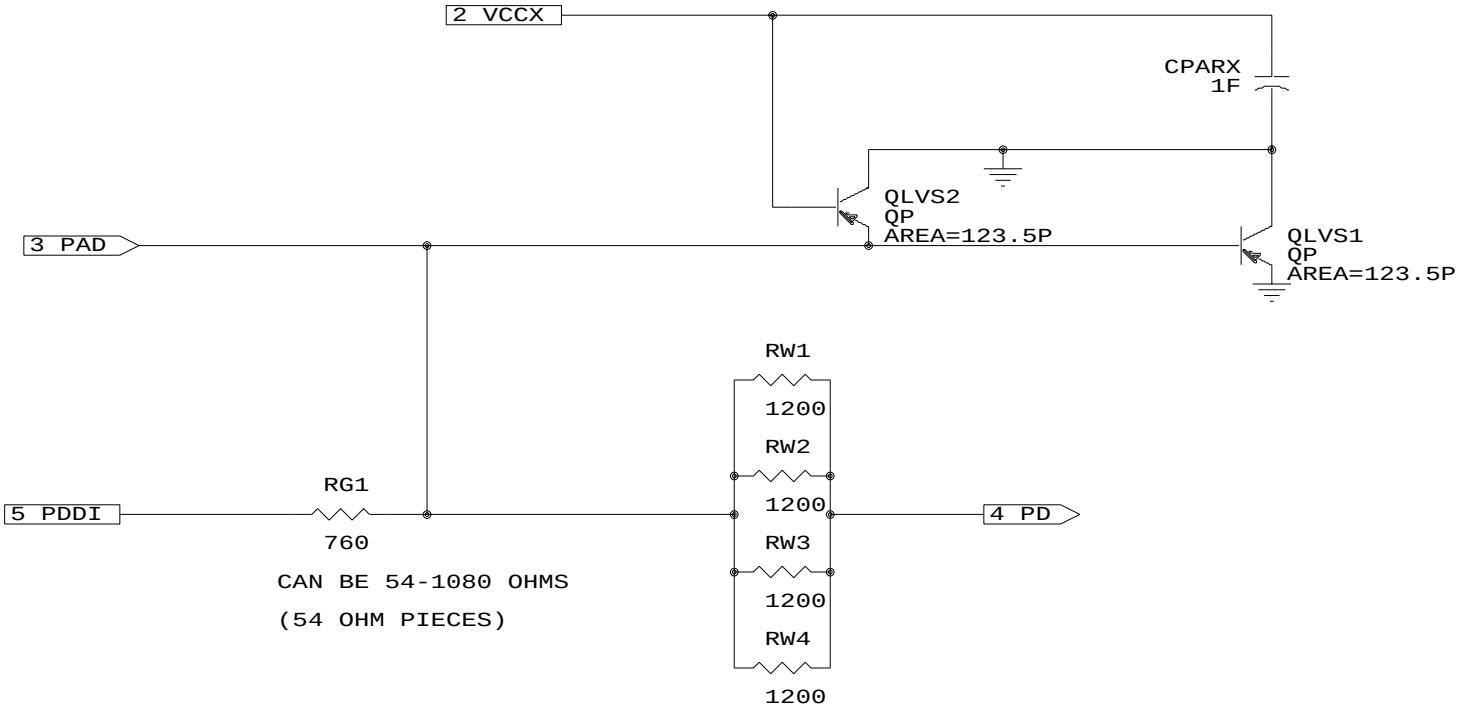
THE EDGE SEAL FOR THE CHIP IS
ALSO IN THIS LAYOUT CELL.



PLACED IN D14CHIP

UNITED MEMORIES INC. PROJECT: 128D14		
Title TOP LEVEL FILTER CAPS - PLACED 4X		
Size A	Document Number EDGE	REV A
Date: December 10, 2001	Sheet 1 of 1	

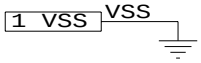

XLEFT
LEFT
XDCON
DCON
XDPATH
DPATH
XIOBLK
IOBLK
XRMISC
RMISC
XCONBLK
CONBLK
VBLH
CFIL1
39.7N
M1
NFARYTK
W=741009U
L=0.14U
DPATH >> COL
CONBLK>>BANK
CONBLK>>BANKS/COL
TM<16> TO COL ALSO,RDOFF
RABLK >>BANK
CONBLK>>COL
PLACED IN D14CHIP
UNITED MEMORIES INC.
PROJECT: 128D14
Title
FULL PERIPHERY
Size
B
Document Number
D14PER
REV
Date: December 7, 2001
Sheet 1 of 1



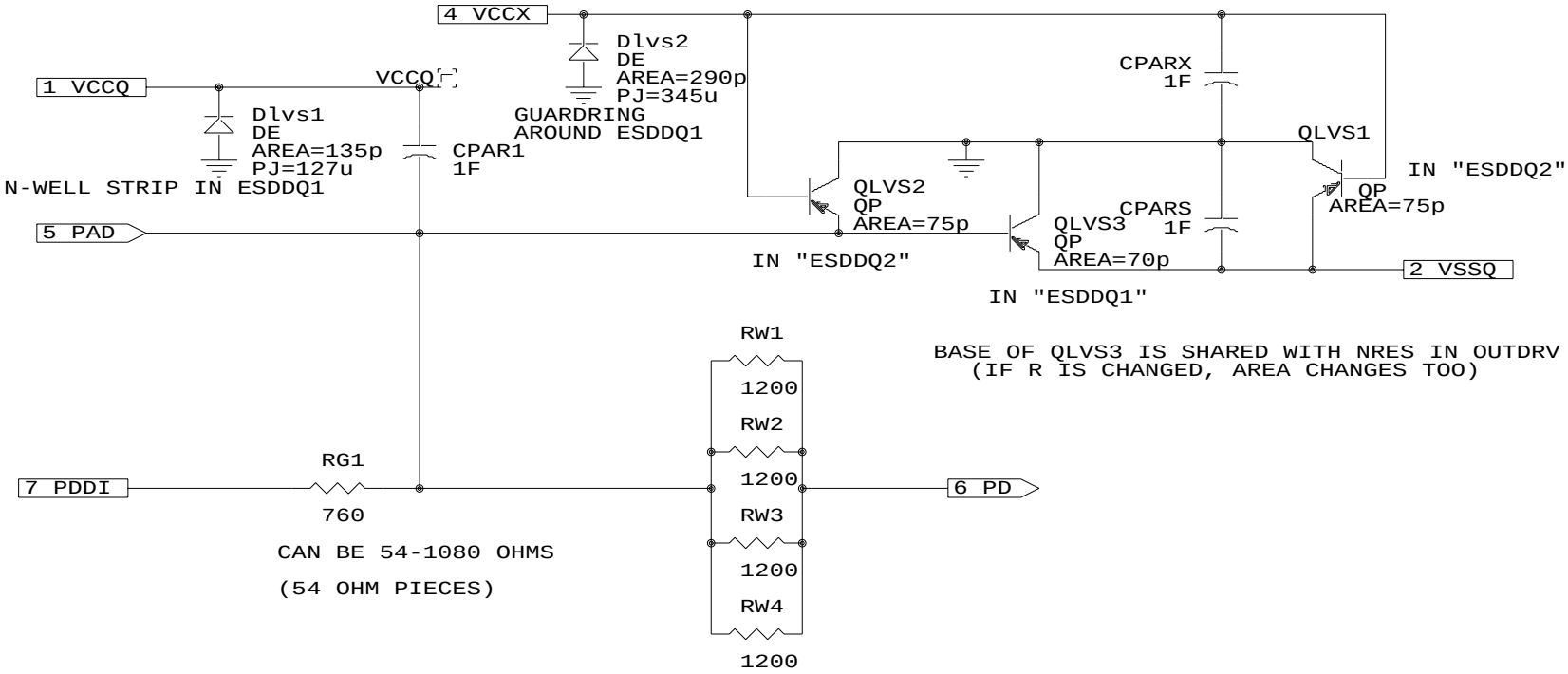
12 WELL DIODES UNDER THE PADS

THESE DIODES ARE TO ADD PAD CAPACITANCE
-INDIVIDUALLY PROGRAMABLE BY PAD

SCHEM IN "CHIP/ESD" SECTION
PLACED IN CONBLK
PLACED IN RABLK



United Memories Inc. PROJECT: 128D14		
Title INPUT PAD ESD (ADDRESS/CONTROL)		
Size A	Document Number ESDIN	REV A
Date: October 12, 2001	Sheet 1 of 1	



12 WELL DIODES UNDER THE PADS

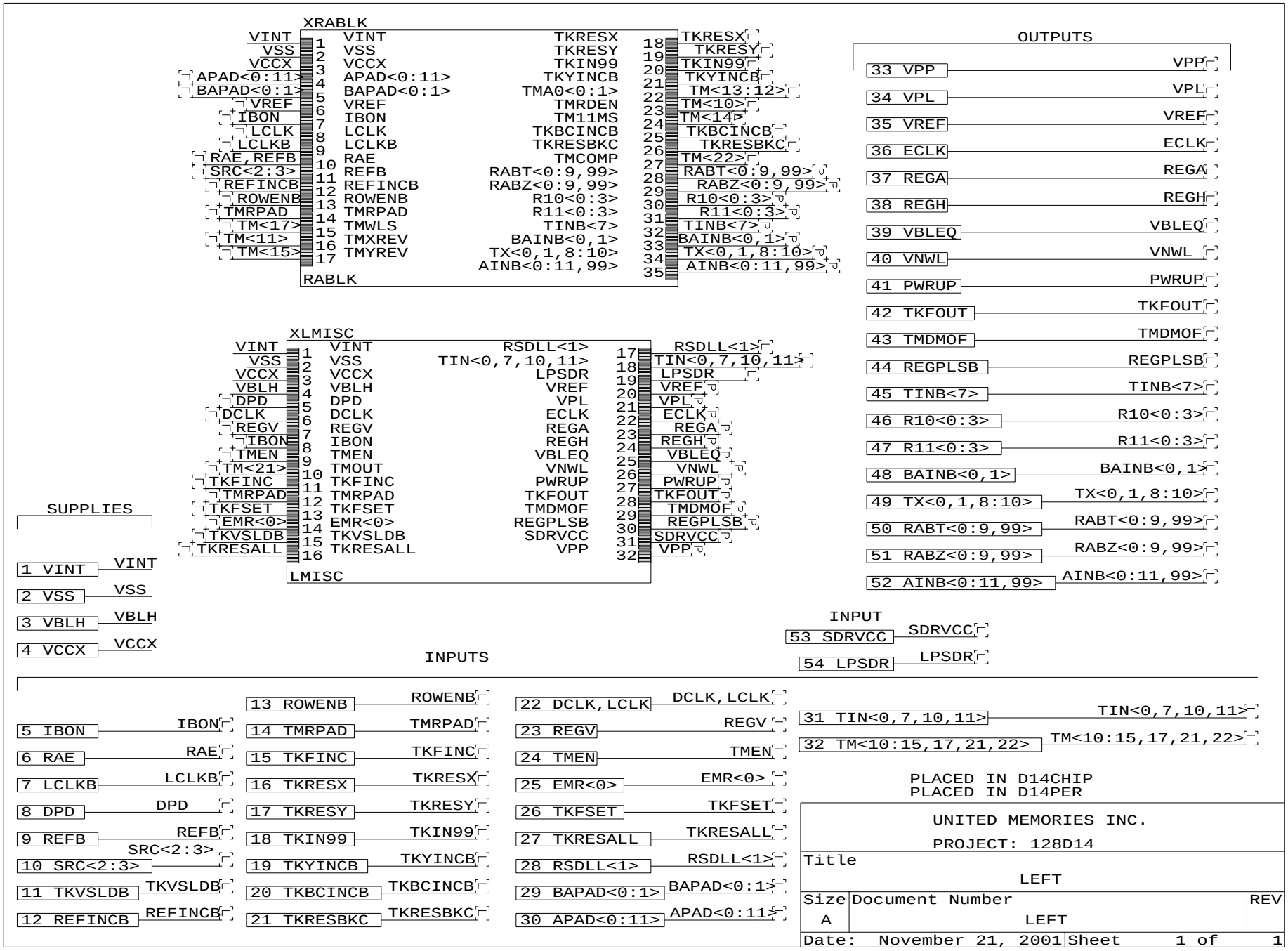
THESE DIODES ARE TO ADD PAD CAPACITANCE

PDDI NODE BROUGHT OUT TO ALLOW
INDIVIDUAL PROGRAMING FOR PER PIN TUNING

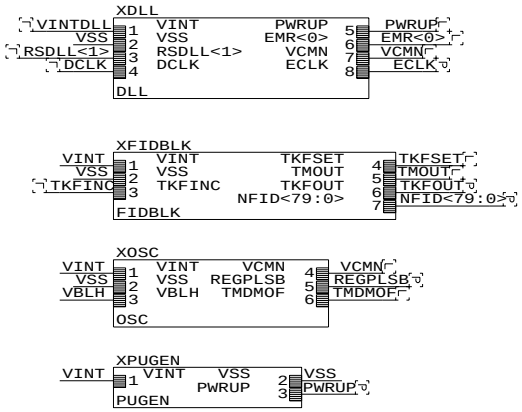
SCHEM IN "CHIP/ESD" SECTION
PLACED IN IOBLK/DQSBLK
PLACED IN IOBLK/QBLK
PLACED IN CONBLK/DQSCON

3 VSS VSS

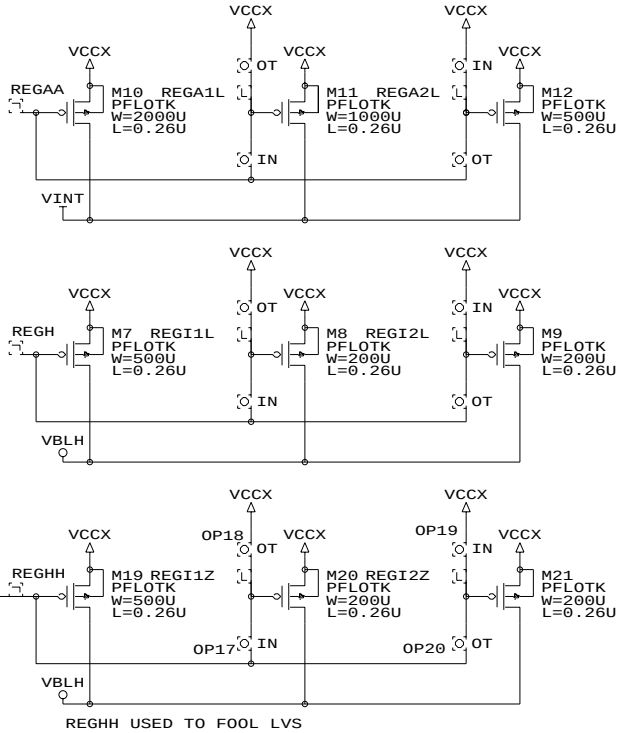
United Memories Inc. PROJECT: 128D14		
Title IO ESD		
Size A	Document Number ESDIO	REV A
Date: August 24, 2001	Sheet 1 of 1	


XRABLK
VINT 1 VINT
VSS 2 VSS
VCCX 3 VCCX
APAD<0:11> 4 APAD<0:11>
BAPAD<0:1> 5 BAPAD<0:1>
VREF 6 VREF
IBON 7 IBON
LCLK 8 LCLK
LCLKB 9 LCLKB
RAE,REFB 10 RAE
SRC<2:3> 11 REFB
REFINCB 12 REFINCB
ROWENB 13 ROWENB
TMRPAD 14 TMRPAD
TM<17> 15 TMWLS
TM<11> 16 TMXREV
TM<15> 17 TMYREV
RABLK
TKRESX 18 TKRESX
TKRESY 19 TKRESY
TKIN99 20 TKIN99
TKYINCB 21 TKYINCB
TM<13:12> 22 TMA0<0:1>
TM<10> 23 TMRDEN
TM<14> 24 TM11MS
TKBCINCB 25 TKBCINCB
TKRESBKC 26 TKRESBKC
TM<22> 27 TMCOMP
RABT<0:9,99> 28 RABT<0:9,99>
RABZ<0:9,99> 29 RABZ<0:9,99>
R10<0:3> 30 R10<0:3>
R11<0:3> 31 R11<0:3>
TINB<7> 32 TINB<7>
BAINB<0,1> 33 BAINB<0,1>
TX<0,1,8:10> 34 TX<0,1,8:10>
AINB<0:11,99> 35 AINB<0:11,99>
OUTPUTS
33 VPP VPP
34 VPL VPL
35 VREF VREF
36 ECLK ECLK
37 REGA REGA
38 REGH REGH
39 VBLEQ VBLEQ
40 VNWL VNWL
41 PWRUP PWRUP
42 TKFOUT TKFOUT
43 TMDMOF TMDMOF
44 REGPLSB REGPLSB
45 TINB<7> TINB<7>
46 R10<0:3> R10<0:3>
47 R11<0:3> R11<0:3>
48 BAINB<0,1> BAINB<0,1>
49 TX<0,1,8:10> TX<0,1,8:10>
50 RABT<0:9,99> RABT<0:9,99>
51 RABZ<0:9,99> RABZ<0:9,99>
52 AINB<0:11,99> AINB<0:11,99>
XLMISC
VINT 1 VINT
VSS 2 VSS
VCCX 3 VCCX
VBLH 4 VBLH
DPD 5 DPD
DCLK 6 DCLK
REGV 7 REGV
IBON 8 IBON
TMEN 9 TMEN
TM<21> 10 TMOUT
TKFINC 11 TKFINC
TMRPAD 12 TMRPAD
TKFSET 13 TKFSET
EMR<0> 14 EMR<0>
TKVSLDB 15 TKVSLDB
TKRESALL 16 TKRESALL
LMISC
RSDLL<1> 17 RSDLL<1>
TIN<0,7,10,11> 18 TIN<0,7,10,11>
LPSDR 19 LPSDR
VREF 20 VREF
VPL 21 VPL
ECLK 22 ECLK
REGA 23 REGA
REGH 24 REGH
VBLEQ 25 VBLEQ
VNWL 26 VNWL
PWRUP 27 PWRUP
TKFOUT 28 TKFOUT
TMDMOF 29 TMDMOF
REGPLSB 30 REGPLSB
SDRVCC 31 SDRVCC
VPP 32 VPP
SUPPLIES
1 VINT VINT
2 VSS VSS
3 VBLH VBLH
4 VCCX VCCX
INPUT
53 SDRVCC SDRVCC
54 LPSDR LPSDR
INPUTS
5 IBON IBON
6 RAE RAE
7 LCLKB LCLKB
8 DPD DPD
9 REFB REFB
10 SRC<2:3> SRC<2:3>
11 TKVSLDB TKVSLDB
12 REFINCB REFINCB
13 ROWENB ROWENB
14 TMRPAD TMRPAD
15 TKFINC TKFINC
16 TKRESX TKRESX
17 TKRESY TKRESY
18 TKIN99 TKIN99
19 TKYINCB TKYINCB
20 TKBCINCB TKBCINCB
21 TKRESBKC TKRESBKC
22 DCLK,LCLK DCLK,LCLK
23 REGV REGV
24 TMEN TMEN
25 EMR<0> EMR<0>
26 TKFSET TKFSET
27 TKRESALL TKRESALL
28 RSDLL<1> RSDLL<1>
29 BAPAD<0:1> BAPAD<0:1>
30 APAD<0:11> APAD<0:11>
31 TIN<0,7,10,11> TIN<0,7,10,11>
32 TM<10:15,17,21,22> TM<10:15,17,21,22>
PLACED IN D14CHIP
PLACED IN D14PER
UNITED MEMORIES INC.
PROJECT: 128D14
Title
LEFT
Size A
Document Number
LEFT
REV
Date: November 21, 2001
Sheet 1 of 1

MISC



VOLTAGES



SUPPLIES

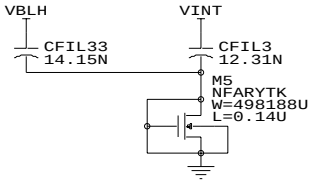
1 VINT	VINT	3 VCCX	VCCX
2 VSS	VSS	4 VBLH	VBLH

INPUTS

5 DPD	DPD
6 DCLK	DCLK
7 REGV	REGV
8 IBON	IBON
9 TMEN	TMEN
10 TMOUT	TMOUT
11 TKFINC	TKFINC
12 TMRPAD	TMRPAD
13 TKFSET	TKFSET
14 EMR<0>	EMR<0>
15 TKVSLDB	TKVSLDB
16 TKRESALL	TKRESALL
17 RSDLL<1>	RSDLL<1>
18 TIN<0,7,10,11>	TIN<0,7,10,11>
19 LPSDR	LPSDR

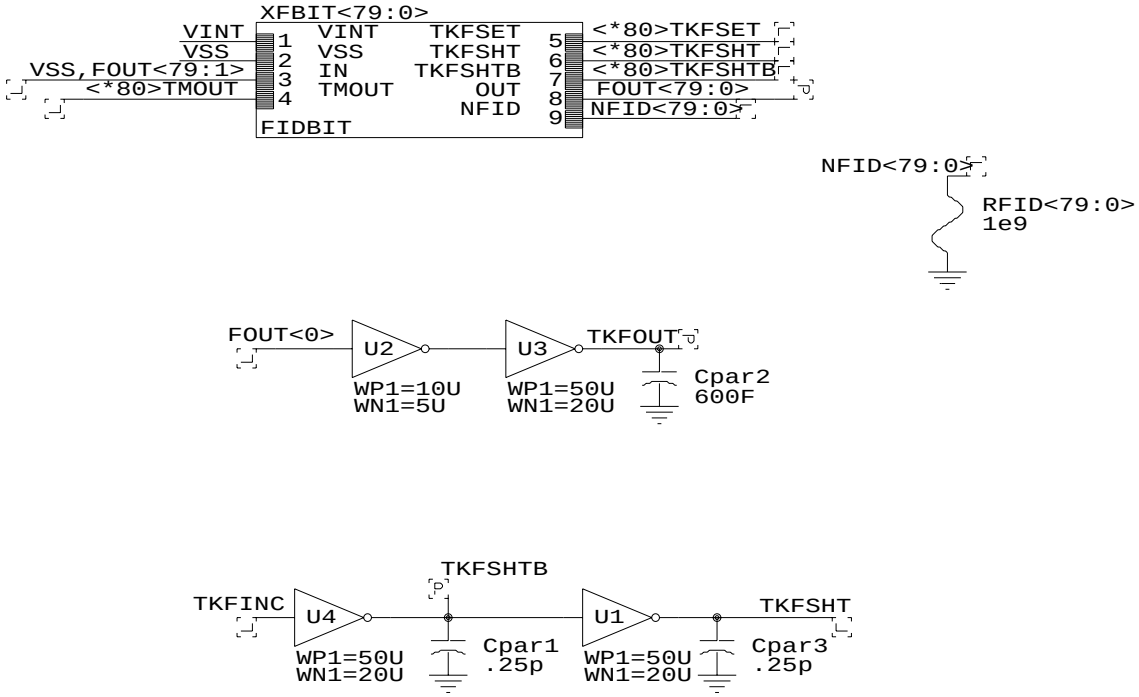
OUTPUTS

20 VREF	VREF
21 VPL	VPL
22 ECLK	ECLK
23 REGA	REGA
24 REGH	REGH
25 VBLEQ	VBLEQ
26 VNWL	VNWL
27 PWRUP	PWRUP
28 TKFOUT	TKFOUT
29 TMDMOF	TMDMOF
30 REGPLSB	REGPLSB
31 SDRVCC	SDRVCC
32 VPP	VPP

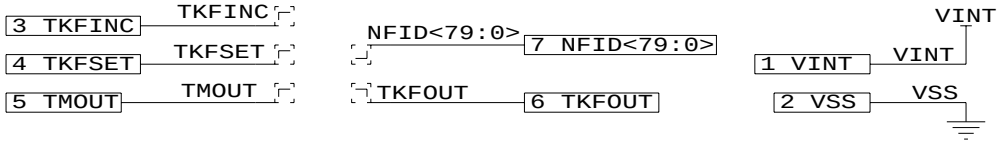


PLACED IN LEFT

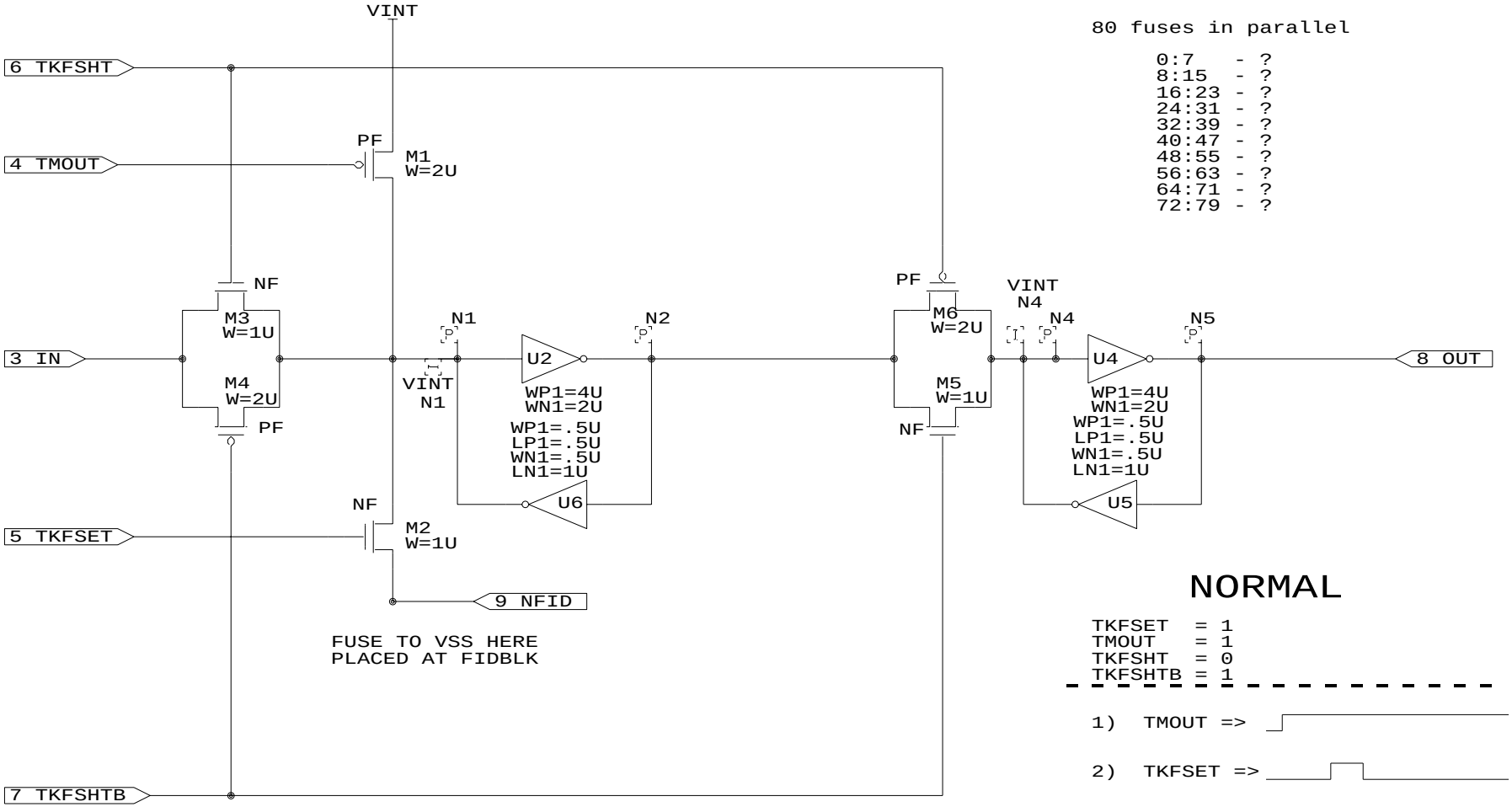
UNITED MEMORIES INC.		
PROJECT:128D14		
Title LEFT SIDE MISCELLANEOUS		
Size B	Document Number LMISC	REV A
Date: December 10, 2001	Sheet 1 of 1	



PLACED IN LMISC



United Memories Inc. Project: 128D14		
Title FUSE ID BLOCK		
Size A	Document Number FIDBLK	REV A
Date: October 17, 2001	Sheet 1 of 1	



80 fuses in parallel

0:7 - ?
8:15 - ?
16:23 - ?
24:31 - ?
32:39 - ?
40:47 - ?
48:55 - ?
56:63 - ?
64:71 - ?
72:79 - ?

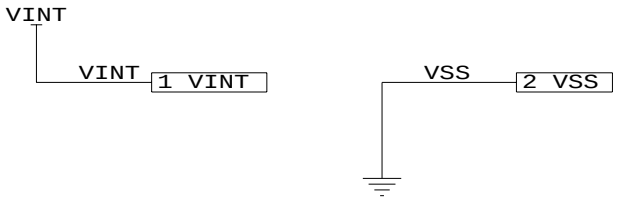
NORMAL

TKFSET = 1
TMOUT = 1
TKFSHT = 0
TKFSHTB = 1

1) TMOUT =>

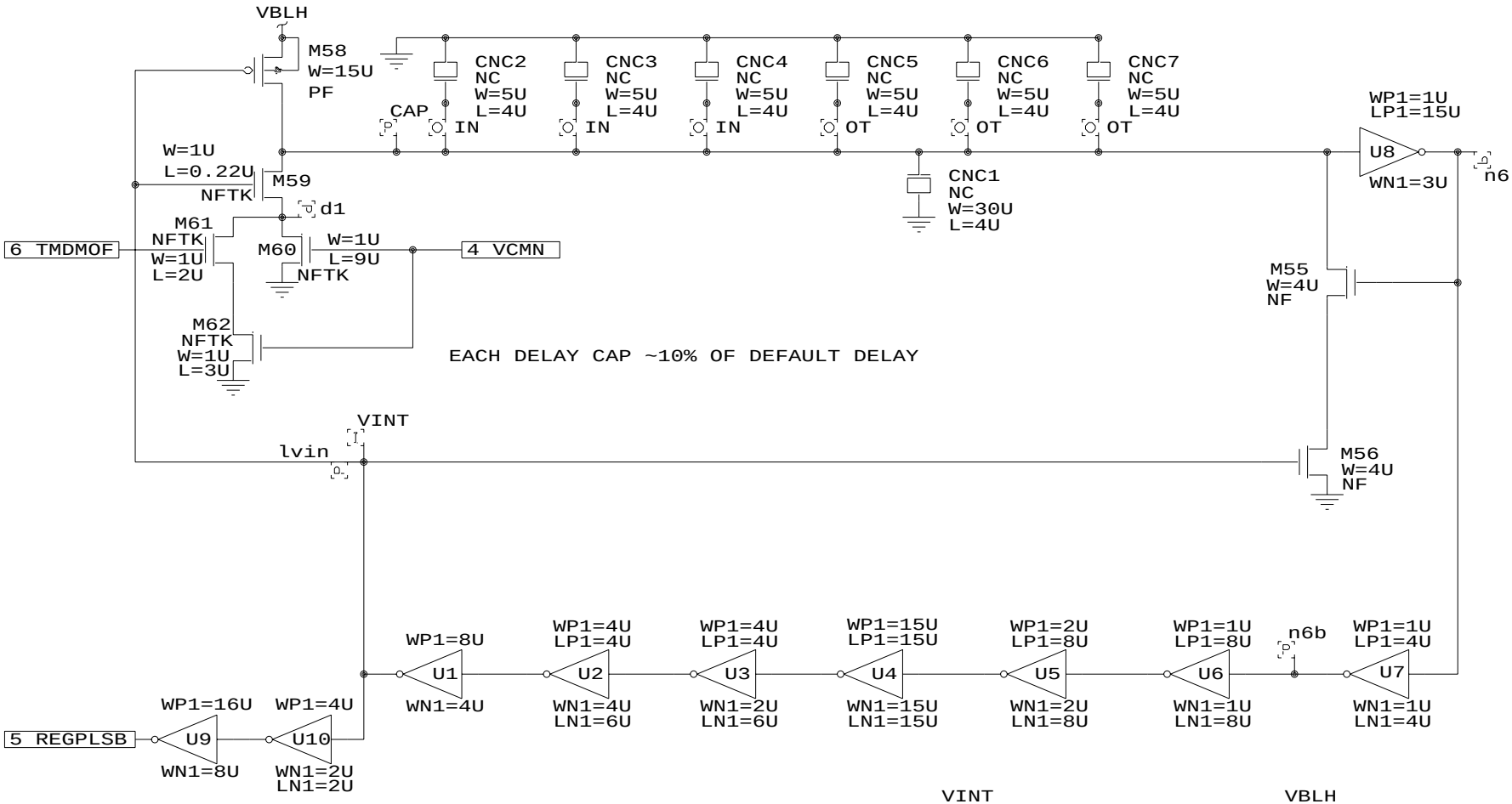
2) TKFSET =>

3) TKFSHT =>



PLACED IN LMISC
PLACED IN FIDBLK

United Memories, Inc. PROJECT: 128D14		
Title Fuse Identification Bit		
Size A	Document Number FIDBIT	REV A
Date: October 17, 2001	Sheet 1 of 1	



Operating Conditions With Delay Settings Shown:

MODELS	TEMP	VINT	VBLH	VCMN	CURRENT	PERIOD	TMDMOF	
NOM	105	2.0	1.6	0.841	1.21UA	9.04US	0	
NOM	-15	2.0	1.6	0.887	0.76UA	12.34US	0	
NOM	-15	1.8	1.75	0.887	0.53UA	14.58US	0	
NOM	-15	2.2	1.45	0.887	1.21UA	10.28US	0	
NOM	105	2.2	1.45	0.841	1.90UA	7.64US	0	
NOM	105	1.8	1.75	0.841	0.85UA	10.45US	0	
SNSP	105	2.0	1.6	0.900	1.30UA	8.44US	0	
FNFP	-15	2.0	1.6	0.847	0.90UA	12.56US	0	
NOM	105	2.0	1.6	0.841	3.39UA	2.81US	VINT	
NOM	125	2.8	2.8	0.841	4.95UA	4.36US	VINT	*BURN IN

*** HIGHLY DEPENDENT UPON VCMN WHICH SHOULD TRACK WITH N-CHAN MODS

VINT — VINT — 1 VINT

VBLH — 3 VBLH — VBLH

VSS — 2 VSS

PLACED IN LMISC

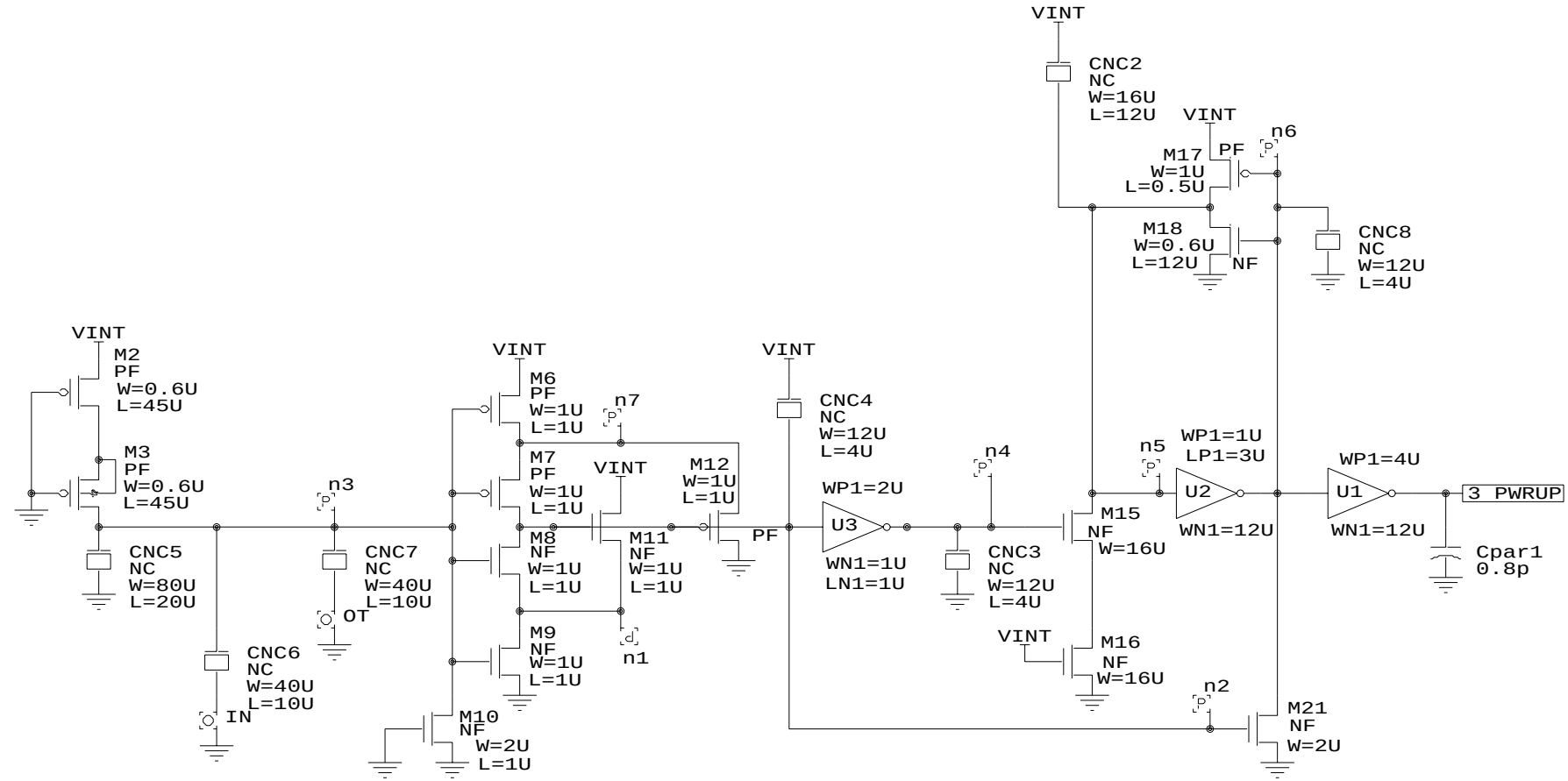
UNITED MEMORIES INC.

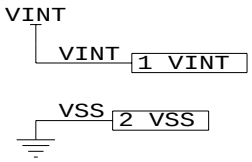
PROJECT: 128D14

Title: SRM Oscillator

Size	Document Number	REV
A	OSC	A

Date: November 15, 2001 Sheet 1 of 1

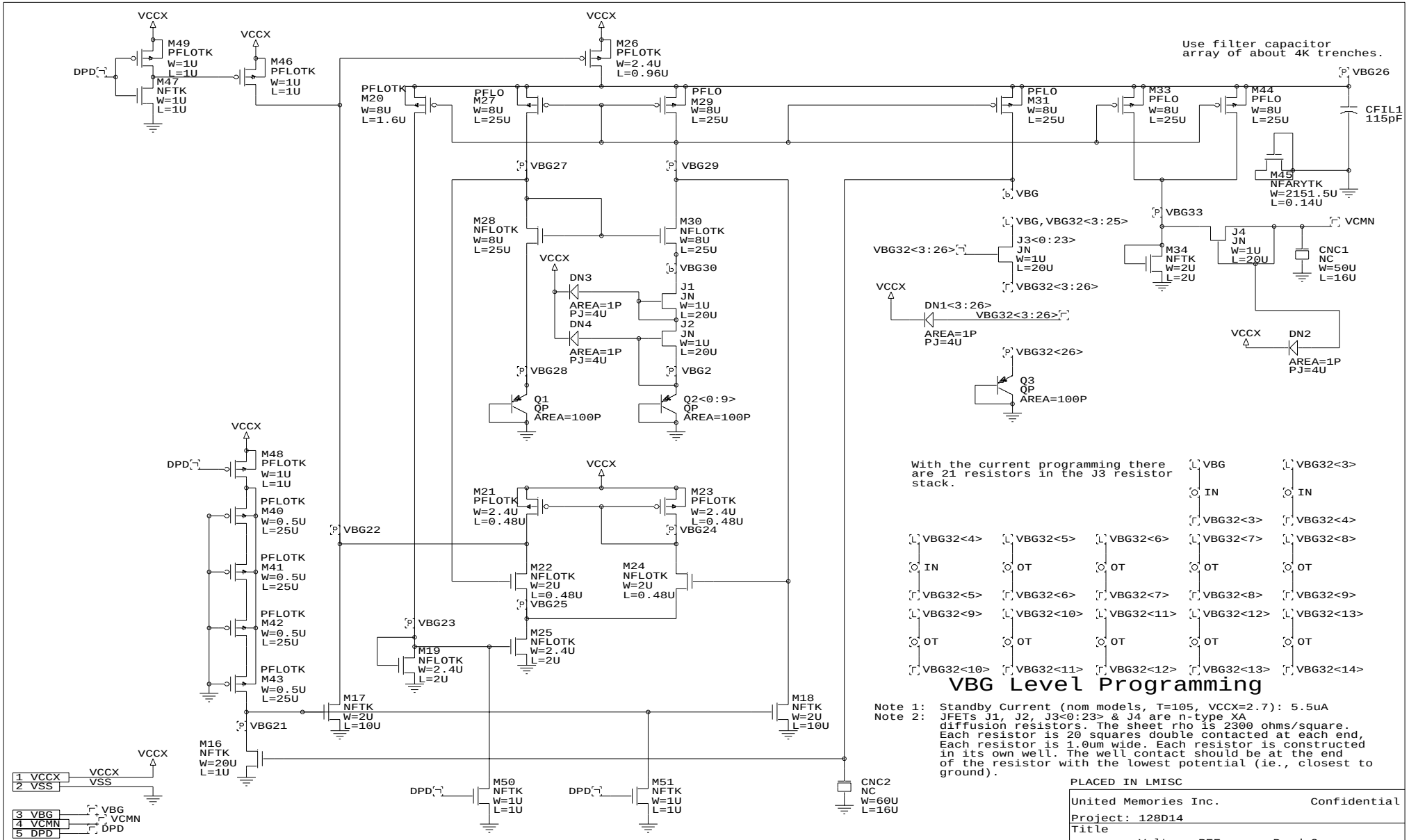


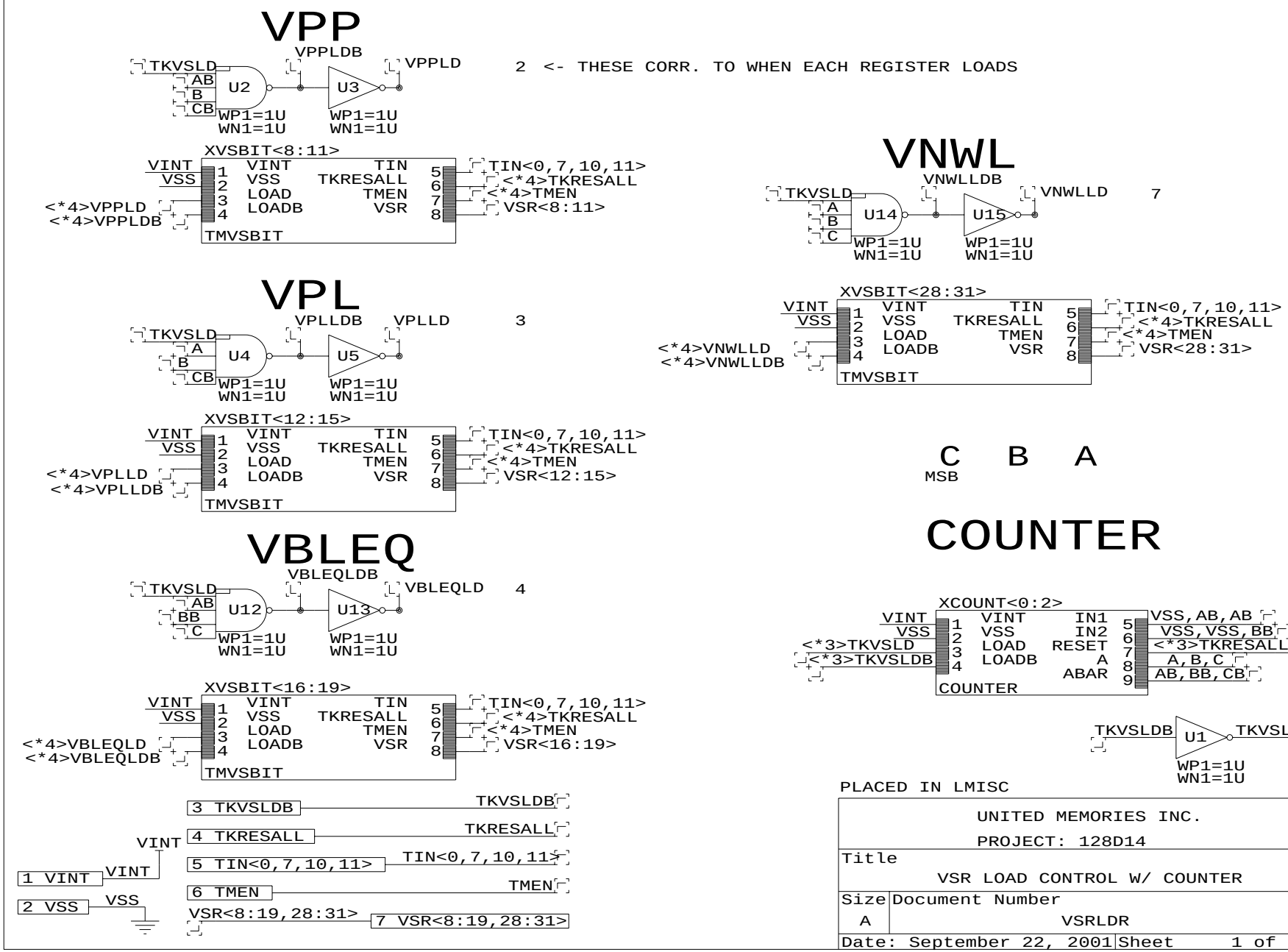


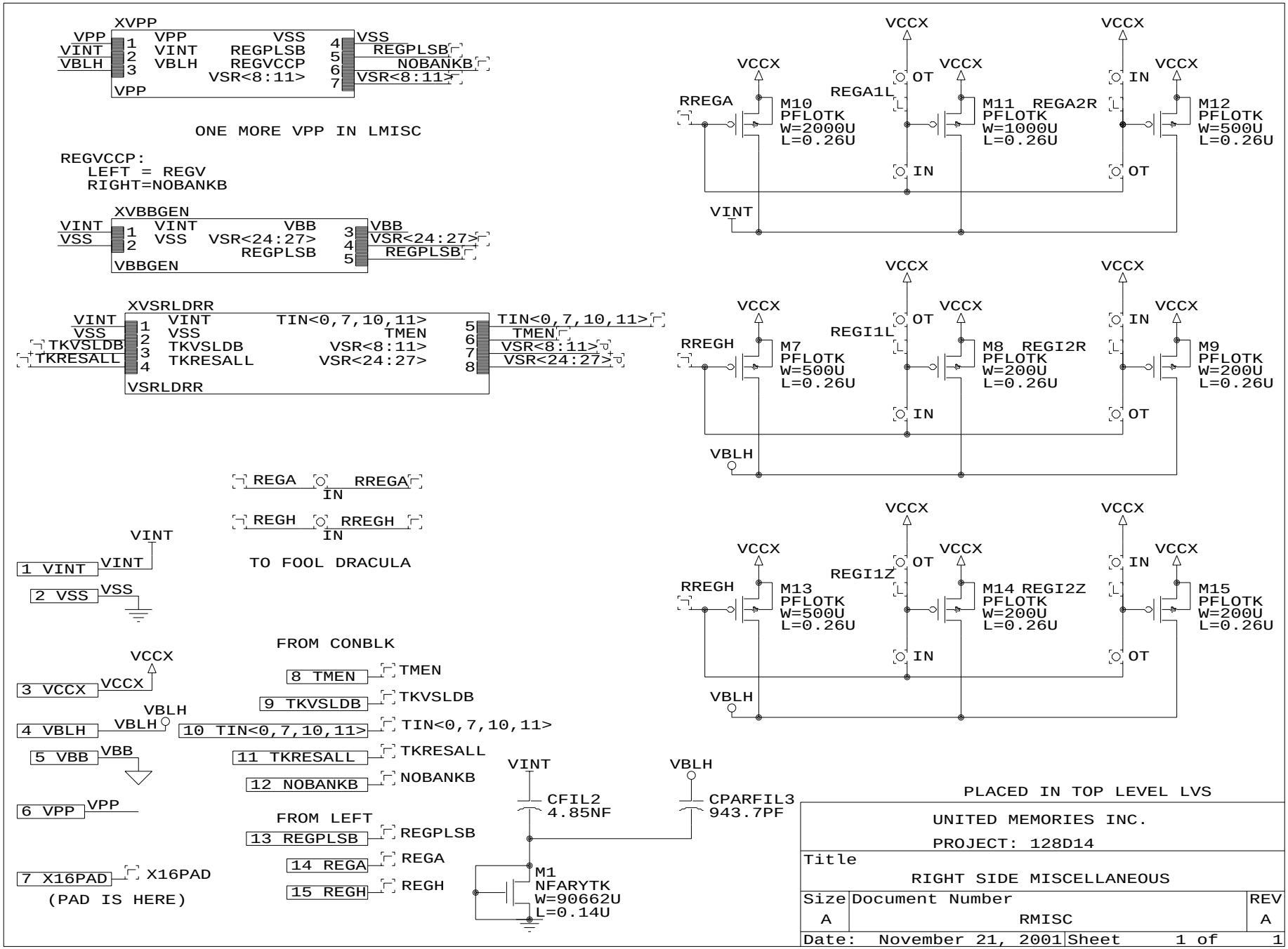
MODIFICATION OF 128DDR S17
- REMOVED JFETS (I=0)

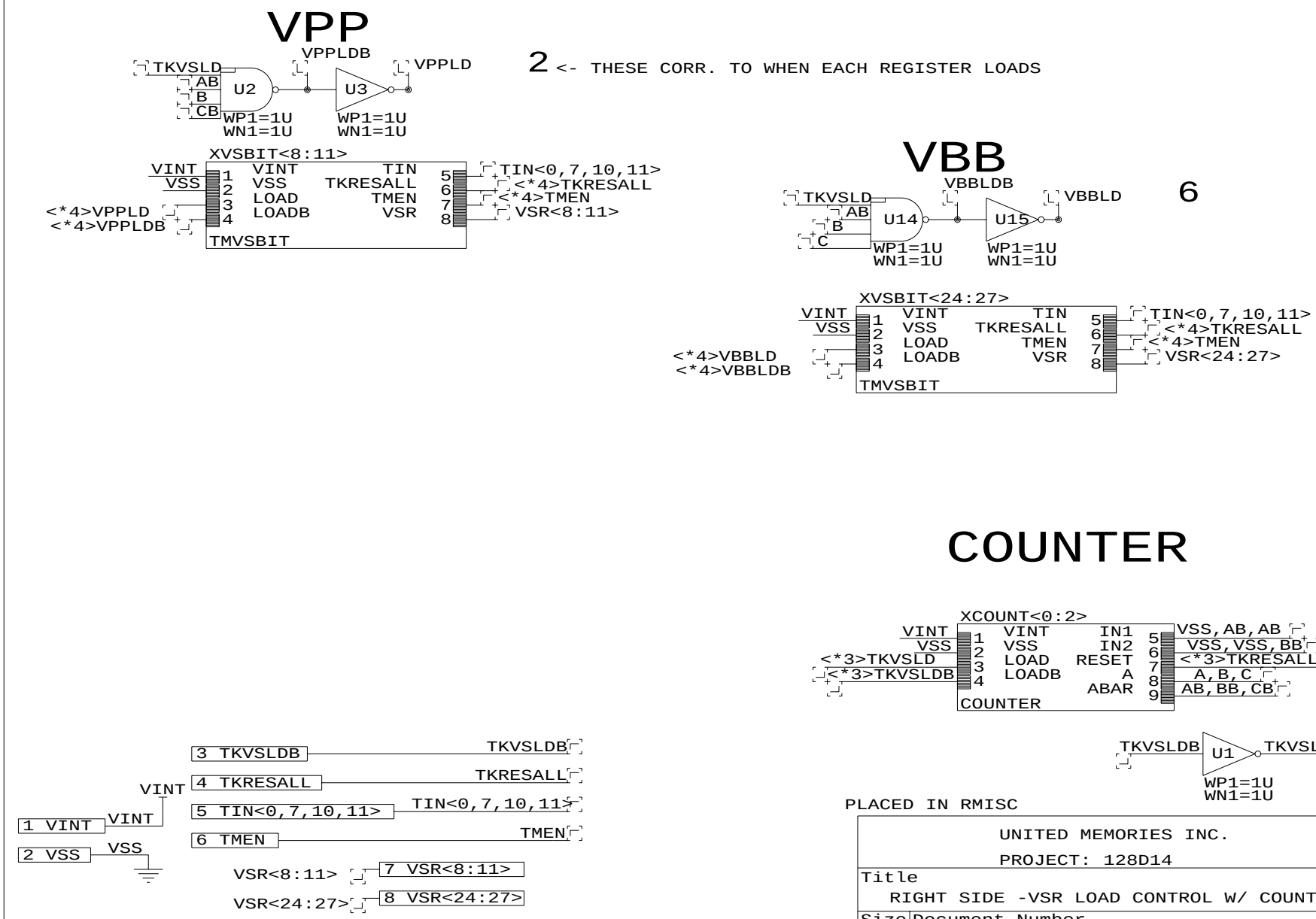
PLACED IN LMISC

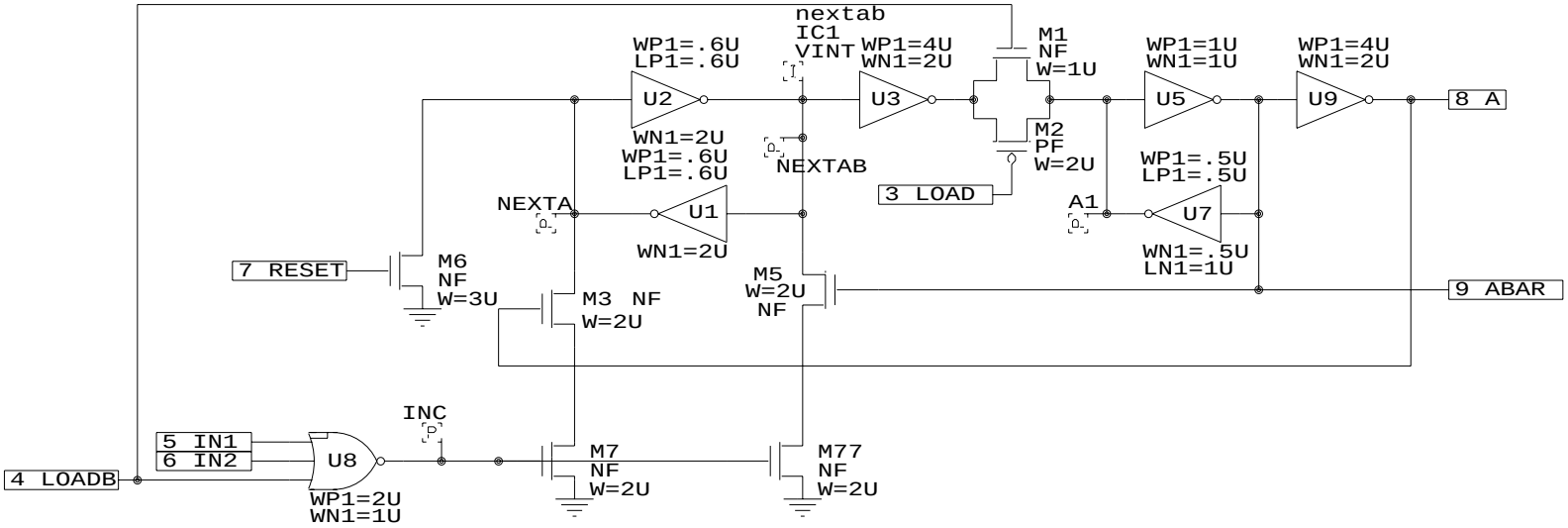
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
PWRUP GENERATOR		
Size	Document Number	REV
A	PUGEN	A
Date: May 12, 2001	Sheet 1 of 1	


VCCX
M49 PFLOTK W=1U L=1U
DPD
M47 NFTK W=1U L=1U
M46 PFLOTK W=1U L=1U
M26 PFLOTK W=2.4U L=0.96U
Use filter capacitor array of about 4K trenches.
VBG26
PFLOTK M20 W=8U L=1.6U
PFLO M27 W=8U L=25U
PFLO M29 W=8U L=25U
PFLO M31 W=8U L=25U
M33 PFLO W=8U L=25U
M44 PFLO W=8U L=25U
CFIL1 115pF
M45 NFARYTK W=2151.5U L=0.14U
VBG27
VBG29
VBG
VBG33
VCMN
M28 NFLOTK W=8U L=25U
M30 NFLOTK W=8U L=25U
VBG30
VBG,VBG32<3:25>
J3<0:23> JN W=1U L=20U
VBG32<3:26>
J4 JN W=1U L=20U
M34 NFTK W=2U L=2U
CNC1 NC W=50U L=16U
DN3
AREA=1P PJ=4U
J1 JN W=1U L=20U
DN4
J2 JN W=1U L=20U
DN1<3:26>
DN2
VBG28
VBG2
VBG32<26>
Q1 QP AREA=100P
Q2<0:9> QP AREA=100P
Q3 QP AREA=100P
M48 PFLOTK W=1U L=1U
PFLOTK M40 W=0.5U L=25U
PFLOTK M41 W=0.5U L=25U
PFLOTK M42 W=0.5U L=25U
PFLOTK M43 W=0.5U L=25U
VBG22
M21 PFLOTK W=2.4U L=0.48U
M23 PFLOTK W=2.4U L=0.48U
VBG24
M22 NFLOTK W=2U L=0.48U
M24 NFLOTK W=2U L=0.48U
VBG25
VBG23
M19 NFLOTK W=2.4U L=2U
M25 NFLOTK W=2.4U L=2U
M17 NFTK W=2U L=10U
M18 NFTK W=2U L=10U
VBG21
M16 NFTK W=20U L=1U
1 VCCX
2 VSS
3 VBG
4 VCMN
5 DPD
M50 NFTK W=1U L=1U
M51 NFTK W=1U L=1U
CNC2 NC W=60U L=16U
With the current programming there are 21 resistors in the J3 resistor stack.
VBG IN VBG32<3>
VBG32<3> IN VBG32<4>
VBG32<4> IN VBG32<5>
VBG32<5> OT VBG32<6>
VBG32<6> OT VBG32<7>
VBG32<7> OT VBG32<8>
VBG32<8> OT VBG32<9>
VBG32<9> OT VBG32<10>
VBG32<10> OT VBG32<11>
VBG32<11> OT VBG32<12>
VBG32<12> OT VBG32<13>
VBG32<13> OT VBG32<14>
VBG Level Programming
Note 1: Standby Current (nom models, T=105, VCCX=2.7): 5.5uA
Note 2: JFETs J1, J2, J3<0:23> & J4 are n-type XA diffusion resistors. The sheet rho is 2300 ohms/square. Each resistor is 20 squares double contacted at each end, Each resistor is 1.0um wide. Each resistor is constructed in its own well. The well contact should be at the end of the resistor with the lowest potential (ie., closest to ground).
PLACED IN LMISC
Outputs: VBG (Voltage reference Band Gap to ???)
VCMN (Voltage Current Mirror N-type to VPL)
United Memories Inc.
Confidential
Project: 128D14
Title
Voltage REFerence Band Gap
Size B
Document Number VREFBG
REV A
Date: October 24, 2001
Sheet 1 of 1

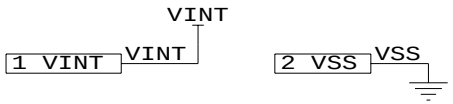

VPP
TKVSLD
AB
B
CB
U2
VPPLDB
U3
VPPLD
2 <- THESE CORR. TO WHEN EACH REGISTER LOADS
WP1=1U
WN1=1U
WP1=1U
WN1=1U
XVSBIT<8:11>
VINT
VSS
<*4>VPPLD
<*4>VPPLDB
VINT
VSS
LOAD
LOADB
TIN
TKRESALL
TMEN
VSR
TIN<0,7,10,11>
<*4>TKRESALL
<*4>TMEN
VSR<8:11>
TMVSBIT
VPL
TKVSLD
A
B
CB
U4
VPLLDB
U5
VPLLD
3
WP1=1U
WN1=1U
WP1=1U
WN1=1U
XVSBIT<12:15>
VINT
VSS
<*4>VPLLD
<*4>VPLLDB
VINT
VSS
LOAD
LOADB
TIN
TKRESALL
TMEN
VSR
TIN<0,7,10,11>
<*4>TKRESALL
<*4>TMEN
VSR<12:15>
TMVSBIT
VBLEQ
TKVSLD
AB
BB
C
U12
VBLEQLDB
U13
VBLEQLD
4
WP1=1U
WN1=1U
WP1=1U
WN1=1U
XVSBIT<16:19>
VINT
VSS
<*4>VBLEQLD
<*4>VBLEQLDB
VINT
VSS
LOAD
LOADB
TIN
TKRESALL
TMEN
VSR
TIN<0,7,10,11>
<*4>TKRESALL
<*4>TMEN
VSR<16:19>
TMVSBIT
3 TKVSLDB
TKVSLDB
4 TKRESALL
TKRESALL
VINT
5 TIN<0,7,10,11>
TIN<0,7,10,11>
1 VINT
VINT
6 TMEN
TMEN
2 VSS
VSS
VSR<8:19,28:31>
7 VSR<8:19,28:31>
VNWL
TKVSLD
A
B
C
U14
VNWLLDB
U15
VNWLLD
7
WP1=1U
WN1=1U
WP1=1U
WN1=1U
XVSBIT<28:31>
VINT
VSS
<*4>VNWLLD
<*4>VNWLLDB
VINT
VSS
LOAD
LOADB
TIN
TKRESALL
TMEN
VSR
TIN<0,7,10,11>
<*4>TKRESALL
<*4>TMEN
VSR<28:31>
TMVSBIT
C B A
MSB
COUNTER
XCOUNT<0:2>
VINT
VSS
<*3>TKVSLD
<*3>TKVSLDB
VINT
VSS
LOAD
LOADB
IN1
IN2
RESET
A
ABAR
VSS,AB,AB
VSS,VSS,BB
<*3>TKRESALL
A,B,C
AB,BB,CB
COUNTER
TKVSLDB
U1
TKVSLD
WP1=1U
WN1=1U
PLACED IN LMISC
UNITED MEMORIES INC.
PROJECT: 128D14
Title
VSR LOAD CONTROL W/ COUNTER
Size
A
Document Number
VSRLDR
REV
A
Date: September 22, 2001
Sheet 1 of 1


XVPP
VPP
VINT
VBLH
VPP
VINT
VBLH
VPP
VINT
REGPLSB
REGVCCP
VSR<8:11>
VSS
REGPLSB
NOBANKB
VSR<8:11>
ONE MORE VPP IN LMISC
REGVCCP:
LEFT = REGV
RIGHT=NOBANKB
XVBBGEN
VINT
VSS
VINT
VSS
VSR<24:27>
REGPLSB
VBB
VBB
VSR<24:27>
REGPLSB
VBBGEN
XVSRLDRR
VINT
VSS
TKVSLDB
TKRESALL
VINT
VSS
TKVSLDB
TKRESALL
TIN<0,7,10,11>
TMEN
VSR<8:11>
VSR<24:27>
TIN<0,7,10,11>
TMEN
VSR<8:11>
VSR<24:27>
VSRLDRR
REGA
IN
RREGA
REGH
IN
RREGH
TO FOOL DRACULA
VINT
1 VINT
VINT
2 VSS
VSS
VCCX
3 VCCX
VCCX
VBLH
4 VBLH
VBLH
5 VBB
VBB
6 VPP
VPP
7 X16PAD
X16PAD
(PAD IS HERE)
FROM CONBLK
8 TMEN
TMEN
9 TKVSLDB
TKVSLDB
10 TIN<0,7,10,11>
TIN<0,7,10,11>
11 TKRESALL
TKRESALL
12 NOBANKB
NOBANKB
FROM LEFT
13 REGPLSB
REGPLSB
14 REGA
REGA
15 REGH
REGH
VINT
CFIL2
4.85NF
VBLH
CPARFIL3
943.7PF
M1
NFARYTK
W=90662U
L=0.14U
VCCX
VCCX
VCCX
VCCX
VCCX
VCCX
RREGA
M10
PFLOTK
W=2000U
L=0.26U
REGA1L
OT
IN
M11 REGA2R
PFLOTK
W=1000U
L=0.26U
IN
OT
M12
PFLOTK
W=500U
L=0.26U
VINT
VCCX
VCCX
VCCX
VCCX
VCCX
RREGH
M7
PFLOTK
W=500U
L=0.26U
REGI1L
OT
IN
M8 REGI2R
PFLOTK
W=200U
L=0.26U
IN
OT
M9
PFLOTK
W=200U
L=0.26U
VBLH
VCCX
VCCX
VCCX
VCCX
VCCX
RREGH
M13
PFLOTK
W=500U
L=0.26U
REGI1Z
OT
IN
M14 REGI2Z
PFLOTK
W=200U
L=0.26U
IN
OT
M15
PFLOTK
W=200U
L=0.26U
VBLH
PLACED IN TOP LEVEL LVS
UNITED MEMORIES INC.
PROJECT: 128D14
Title
RIGHT SIDE MISCELLANEOUS
Size
A
Document Number
RMISC
REV
A
Date: November 21, 2001
Sheet 1 of 1

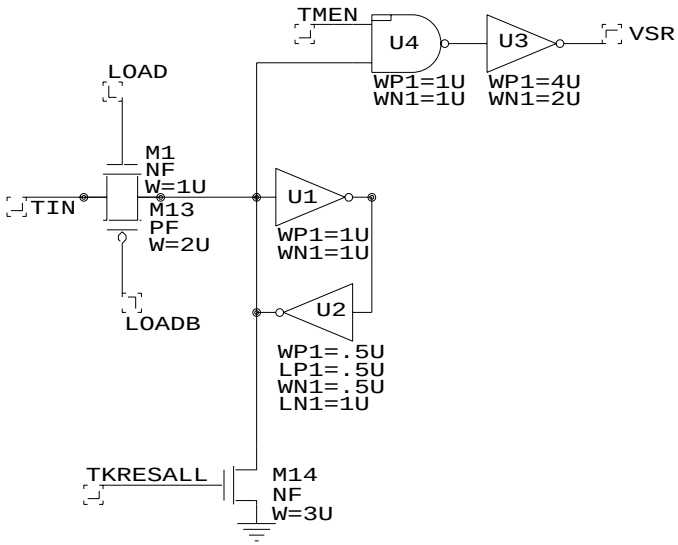

VPP
TKVSLD
AB
B
CB
U2
VPPLDB
U3
VPPLD
WP1=1U
WN1=1U
WP1=1U
WN1=1U
2 <- THESE CORR. TO WHEN EACH REGISTER LOADS
XVSBIT<8:11>
VINT
VSS
<*4>VPPLD
<*4>VPPLDB
1 VINT
2 VSS
3 LOAD
4 LOADB
VINT
VSS
TKRESALL
TMEN
VSR
TIN
5
6
7
8
TIN<0,7,10,11>
<*4>TKRESALL
<*4>TMEN
VSR<8:11>
TMVSBIT
VBB
TKVSLD
AB
B
C
U14
VBBLDB
U15
VBBLD
WP1=1U
WN1=1U
WP1=1U
WN1=1U
6
XVSBIT<24:27>
VINT
VSS
<*4>VBBLD
<*4>VBBLDB
1 VINT
2 VSS
3 LOAD
4 LOADB
VINT
VSS
TKRESALL
TMEN
VSR
TIN
5
6
7
8
TIN<0,7,10,11>
<*4>TKRESALL
<*4>TMEN
VSR<24:27>
TMVSBIT
COUNTER
XCOUNT<0:2>
VINT
VSS
<*3>TKVSLD
<*3>TKVSLDB
1 VINT
2 VSS
3 LOAD
4 LOADB
VINT
VSS
IN1
IN2
RESET
A
ABAR
5
6
7
8
9
VSS,AB,AB
VSS,VSS,BB
<*3>TKRESALL
A,B,C
AB,BB,CB
COUNTER
TKVSLDB
U1
TKVSLD
WP1=1U
WN1=1U
PLACED IN RMISC
3 TKVSLDB
TKVSLDB
4 TKRESALL
TKRESALL
VINT
5 TIN<0,7,10,11>
TIN<0,7,10,11>
1 VINT
VINT
6 TMEN
TMEN
2 VSS
VSS
VSR<8:11>
7 VSR<8:11>
VSR<24:27>
8 VSR<24:27>
UNITED MEMORIES INC.
PROJECT: 128D14
Title
RIGHT SIDE -VSR LOAD CONTROL W/ COUNTER
Size
A
Document Number
VSRLDRR
REV
A
Date: August 24, 2001
Sheet 1 of 1

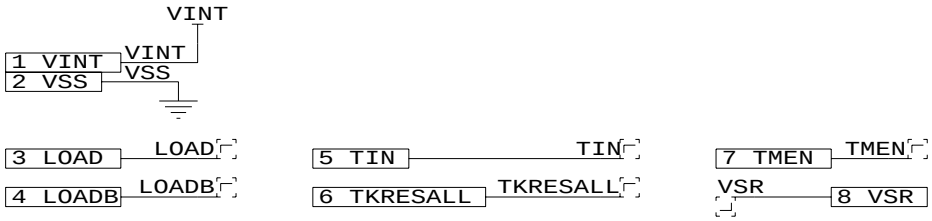


MAKE SURE INC IS OFF BEFORE LOAD=0 !



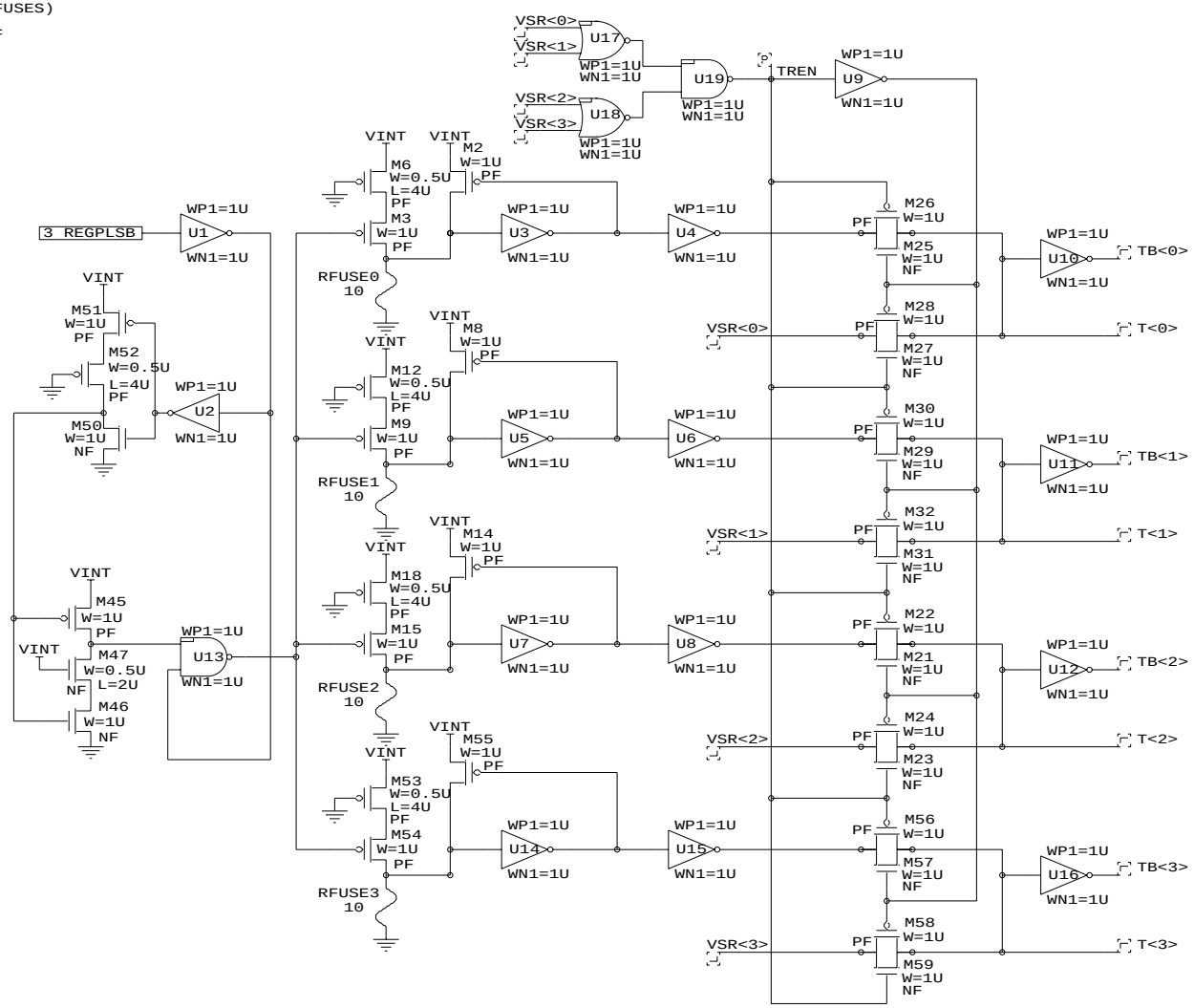
UNITED MEMORIES INC. PROJECT: 128D14		
Title COUNTER		
Size A	Document Number COUNTER	REV A
Date: July 6, 2001	Sheet 1 of 1	





UNITED MEMORIES INC. PROJECT: 128D14		
Title TEST MODE VSR BIT		
Size A	Document Number TMVSBIT	REV A
Date: July 2, 2001	Sheet 1 of 1	

VSR	3	2	1	0	
	0	0	0	0	DEFAULT (FUSES)
	1	1	1	1	SOURCE=OFF



One of these circuits is used for the VINT VDC,
and one is used for the VBLH VDC.

1 VINT — VINT

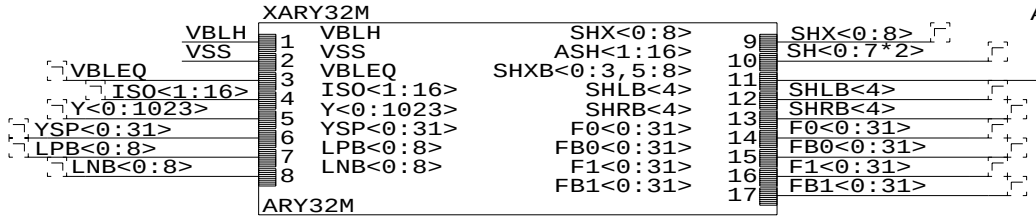
2 VSS

4 VSR<0:3> — VSR<0:3>

5 T<0:3> — T<0:3>

6 TB<0:3> — TB<0:3>

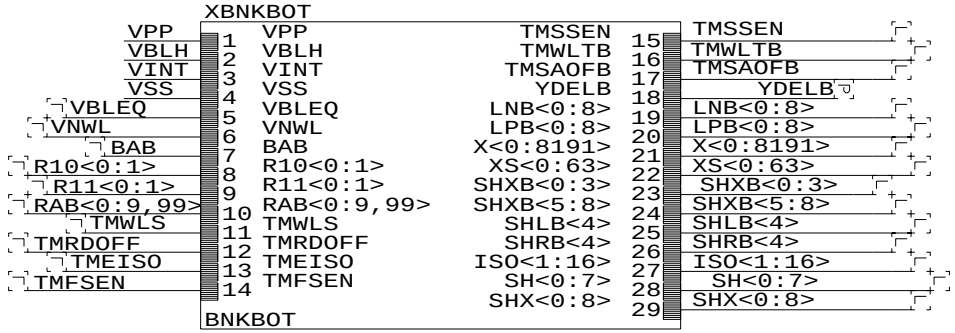
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title VOLTAGE SET REGISTER FUSE CIRCUITRY		
Size B	Document Number VSRFUSE	REV A
Date: June 11, 2001	Sheet 1 of 1	

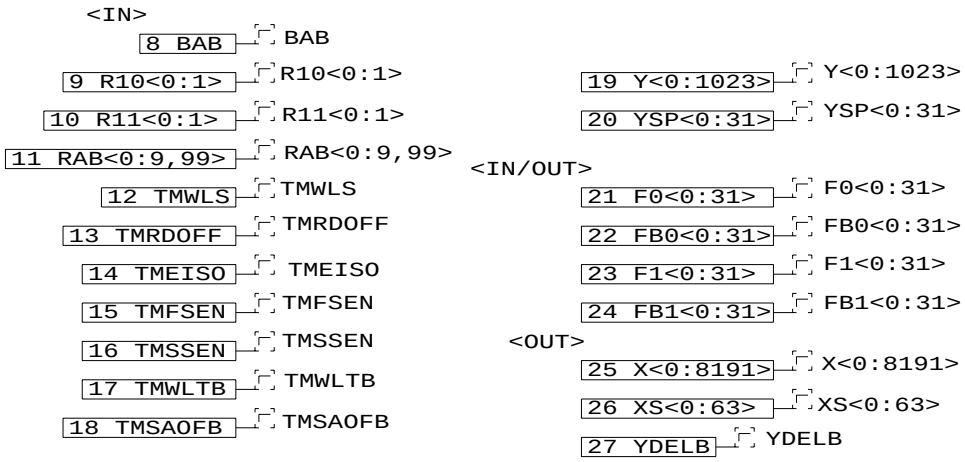


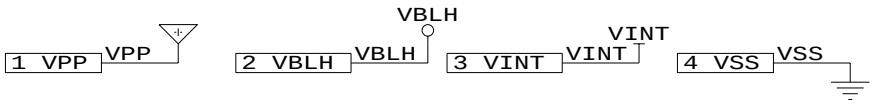
ASH=ARRAY SIDE SH NODES

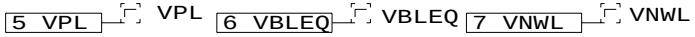
SHLB,SHRB ONLY USED IN MIDDLE CASE
SHXB USED 0:3,5:8

SHX USED IN ALL CASES





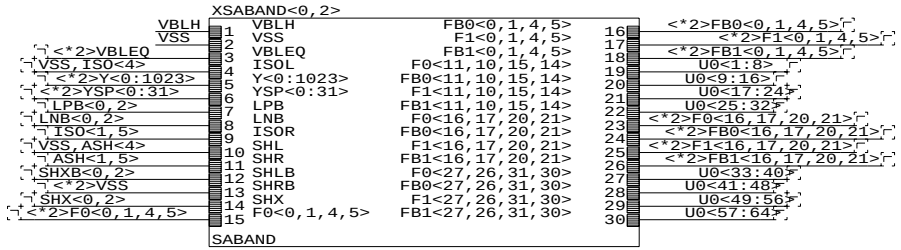


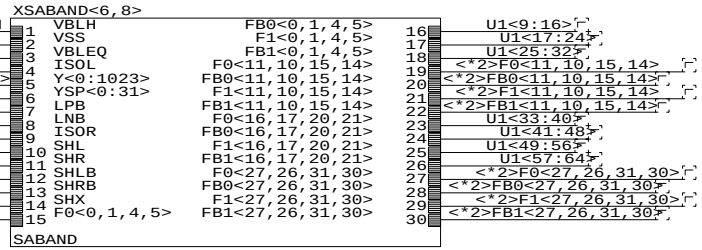


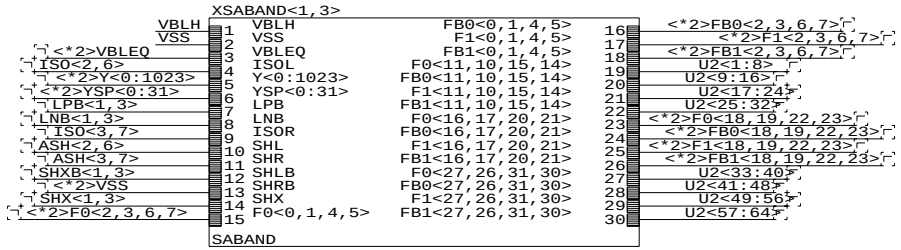
NOT ACTUALLY CONNECTED,
VBB SHOULD BE BROUGHT IN AS WELL

PLACED AT TOP LEVEL LVS

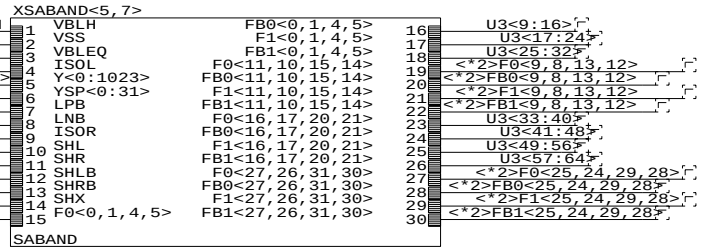
UNITED MEMORIES INC. PROJECT: 128D14		
Title FULL 32M BANK (ARRAY PLUS BOT32M LOGIC)		
Size A	Document Number BANK	REV A
Date: August 24, 2001	Sheet 1 of 1	



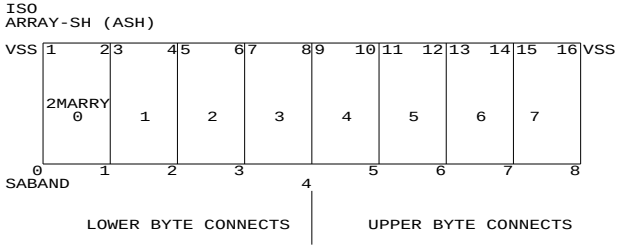


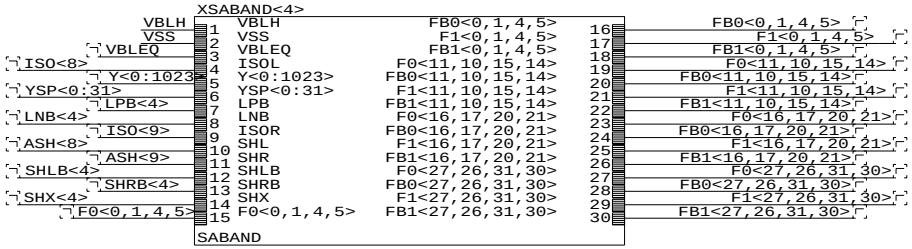


LEFT SIDE OF BANK

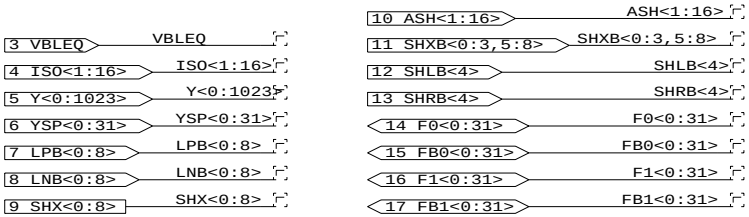


RIGHT SIDE OF BANK





Ux<w:y> ARE UNUSED EXCEPT FOR THE CENTER CASE



ASH=ARRAY SIDE SH NODES
(SHL,SHR SEPARATE AT ARRAY LEVEL)

MIDDLE SABAND OF BANK

DQ MAPPING - THIS LEVEL

	0	1	2	3	4	5	6	7
	15	14	13	12	11	10	9	8

=512 CELLS/BL

	SABANDS<0,2,4>	SABANDS<1,3>	
EVEN C0=0	0 1	2 3	HQUAD<0>
	4 5	6 7	HQUAD<1>
ODD C0=1	0 1	2 3	HQUAD<2>
	4 5	6 7	HQUAD<3>

PLACED IN BANK

UNITED MEMORIES INC.

PROJECT: 128D14

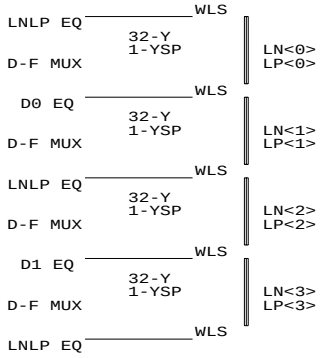
Title

32 MEG ARRAY - 9X SABAND

Size	Document Number	REV
B	ARY32M	A

Date: August 24, 2001 Sheet 1 of 1

CASE TEXTED FOR CENTER SABAND
FOR LEFT SIDE 11,10,15,14 AND 27,26,31,30 PASS THRU
FOR LEFT SIDE 0,1,4,5 AND 16,17,20,21 PASS THRU



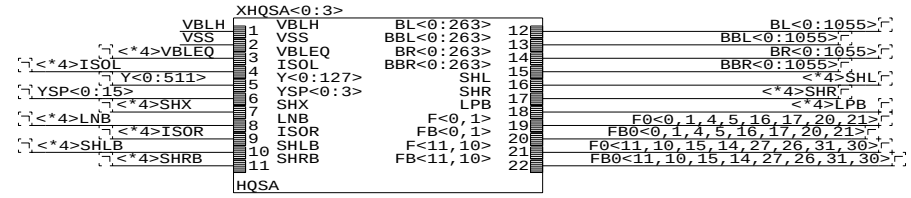
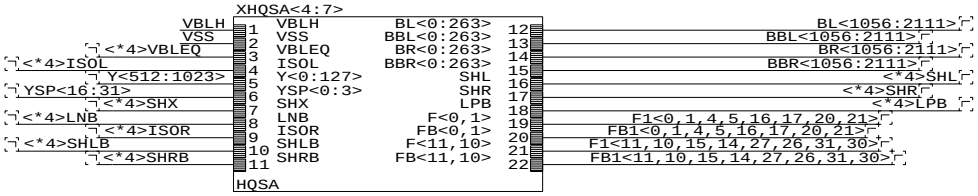
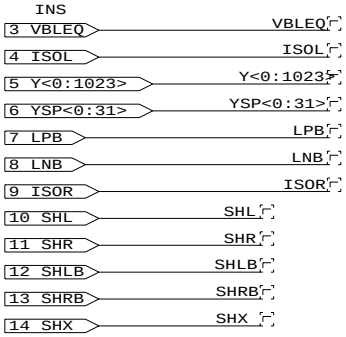
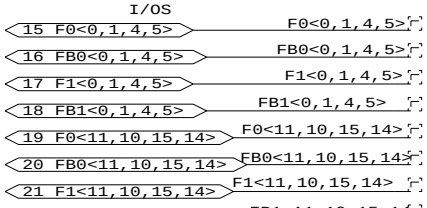


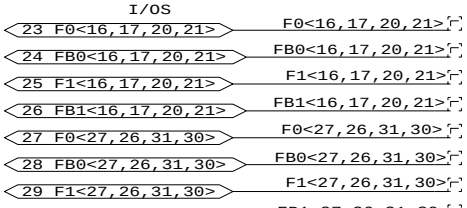
DIAGRAM OF ONE H-QUAD

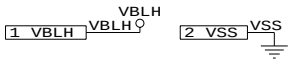
- -128 Y LNES
- -4 SPARE Y'S
- -4 SEPARATE LN/LP BUSES
- (EACH CONNECTS WITH 66 SENSE-AMPS)





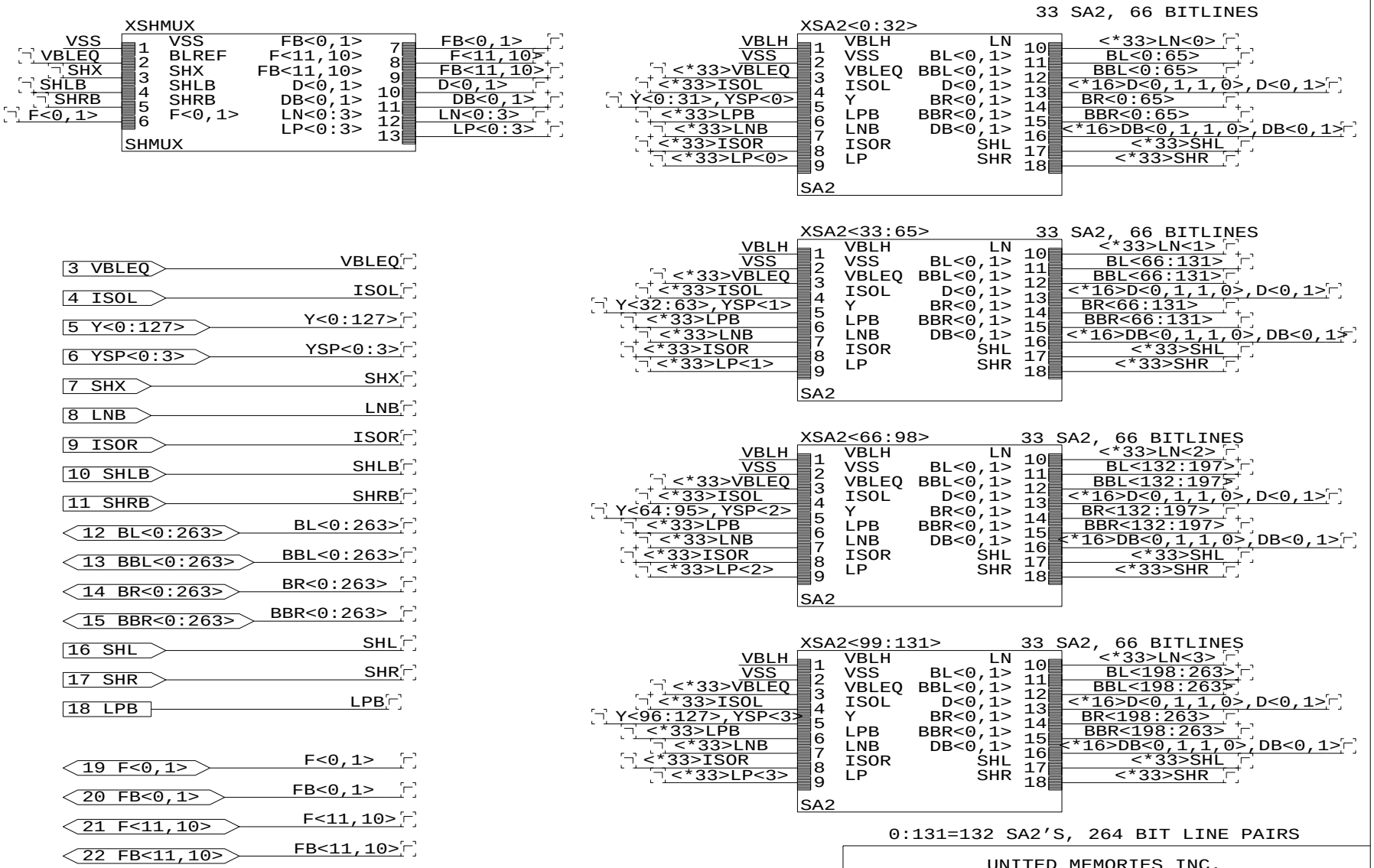


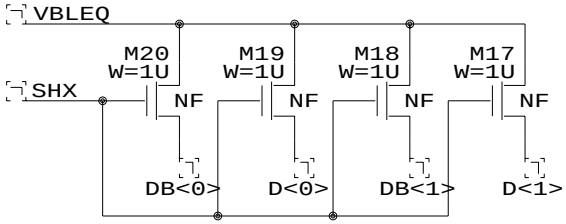




PLACED IN BANK
PLACED IN ARY32M

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	SA BAND - 8X HQSA	
Size B	Document Number SABAND	REV A
Date: August 14, 2001	Sheet 1 of 1	

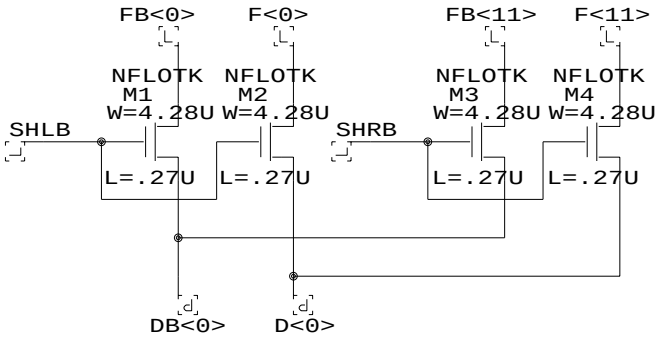

XSHMUX
VSS 1 VSS FB<0,1> 7 FB<0,1>
VBLEQ 2 BLREF F<11,10> 8 F<11,10>
SHX 3 SHX FB<11,10> 9 FB<11,10>
SHLB 4 SHLB D<0,1> 10 D<0,1>
SHRB 5 SHRB DB<0,1> 11 DB<0,1>
F<0,1> 6 F<0,1> LN<0:3> 12 LN<0:3>
LP<0:3> 13 LP<0:3>
SHMUX
33 SA2, 66 BITLINES
XSA2<0:32>
VBLH 1 VBLH LN 10 <*33>LN<0>
VSS 2 VSS BL<0,1> 11 BL<0:65>
<*33>VBLEQ 3 VBLEQ BBL<0,1> 12 BBL<0:65>
<*33>ISOL 4 ISOL D<0,1> 13 <*16>D<0,1,1,0>,D<0,1>
Y<0:31>,YSP<0> 5 Y BR<0,1> 14 BR<0:65>
<*33>LPB 6 LPB BBR<0,1> 15 BBR<0:65>
<*33>LNB 7 LNB DB<0,1> 16 <*16>DB<0,1,1,0>,DB<0,1>
<*33>ISOR 8 ISOR SHL 17 <*33>SHL
<*33>LP<0> 9 LP SHR 18 <*33>SHR
SA2
XSA2<33:65>
33 SA2, 66 BITLINES
VBLH 1 VBLH LN 10 <*33>LN<1>
VSS 2 VSS BL<0,1> 11 BL<66:131>
<*33>VBLEQ 3 VBLEQ BBL<0,1> 12 BBL<66:131>
<*33>ISOL 4 ISOL D<0,1> 13 <*16>D<0,1,1,0>,D<0,1>
Y<32:63>,YSP<1> 5 Y BR<0,1> 14 BR<66:131>
<*33>LPB 6 LPB BBR<0,1> 15 BBR<66:131>
<*33>LNB 7 LNB DB<0,1> 16 <*16>DB<0,1,1,0>,DB<0,1>
<*33>ISOR 8 ISOR SHL 17 <*33>SHL
<*33>LP<1> 9 LP SHR 18 <*33>SHR
SA2
XSA2<66:98>
33 SA2, 66 BITLINES
VBLH 1 VBLH LN 10 <*33>LN<2>
VSS 2 VSS BL<0,1> 11 BL<132:197>
<*33>VBLEQ 3 VBLEQ BBL<0,1> 12 BBL<132:197>
<*33>ISOL 4 ISOL D<0,1> 13 <*16>D<0,1,1,0>,D<0,1>
Y<64:95>,YSP<2> 5 Y BR<0,1> 14 BR<132:197>
<*33>LPB 6 LPB BBR<0,1> 15 BBR<132:197>
<*33>LNB 7 LNB DB<0,1> 16 <*16>DB<0,1,1,0>,DB<0,1>
<*33>ISOR 8 ISOR SHL 17 <*33>SHL
<*33>LP<2> 9 LP SHR 18 <*33>SHR
SA2
XSA2<99:131>
33 SA2, 66 BITLINES
VBLH 1 VBLH LN 10 <*33>LN<3>
VSS 2 VSS BL<0,1> 11 BL<198:263>
<*33>VBLEQ 3 VBLEQ BBL<0,1> 12 BBL<198:263>
<*33>ISOL 4 ISOL D<0,1> 13 <*16>D<0,1,1,0>,D<0,1>
Y<96:127>,YSP<3> 5 Y BR<0,1> 14 BR<198:263>
<*33>LPB 6 LPB BBR<0,1> 15 BBR<198:263>
<*33>LNB 7 LNB DB<0,1> 16 <*16>DB<0,1,1,0>,DB<0,1>
<*33>ISOR 8 ISOR SHL 17 <*33>SHL
<*33>LP<3> 9 LP SHR 18 <*33>SHR
SA2
3 VBLEQ VBLEQ
4 ISOL ISOL
5 Y<0:127> Y<0:127>
6 YSP<0:3> YSP<0:3>
7 SHX SHX
8 LNB LNB
9 ISOR ISOR
10 SHLB SHLB
11 SHRB SHRB
12 BL<0:263> BL<0:263>
13 BBL<0:263> BBL<0:263>
14 BR<0:263> BR<0:263>
15 BBR<0:263> BBR<0:263>
16 SHL SHL
17 SHR SHR
18 LPB LPB
19 F<0,1> F<0,1>
20 FB<0,1> FB<0,1>
21 F<11,10> F<11,10>
22 FB<11,10> FB<11,10>
1 VBLH VBLH VBLH
2 VSS VSS VSS
0:131=132 SA2'S, 264 BIT LINE PAIRS
128 REAL SA2
4 SPARE SA2
PLACED IN BANK
PLACED IN ARY32M
PLACED IN SABAND
UNITED MEMORIES INC.
PROJECT: 128D14
Title
H-QUAD SA AREA
Size A
Document Number HQSA
REV A
Date: August 14, 2001
Sheet 1 of 1

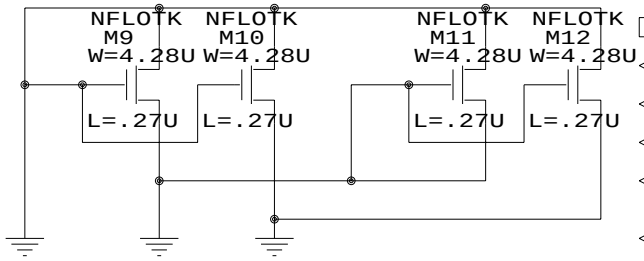


CENTER CASE F<0,11> MUX TO D0
F<1,10> MUX TO D1

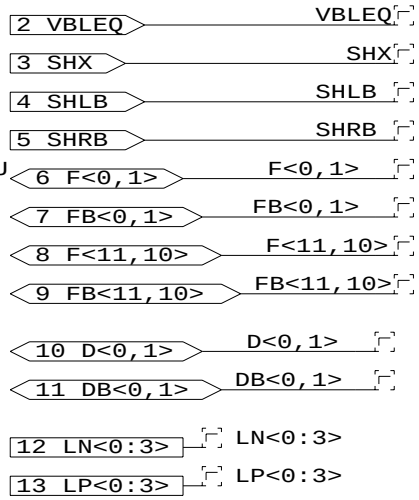
LEFT HALF F<0> MUXES TO D0, F<11> PASSES THRU
RIGHT HALF F<11> MUXES TO D0, F<0> PASSES THRU
(SAME FOR 1,10)

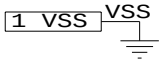
(MIMICS CENTER CASE)

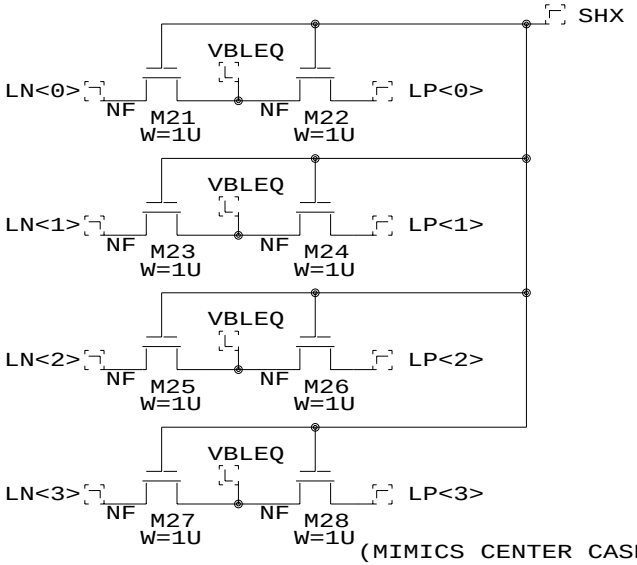




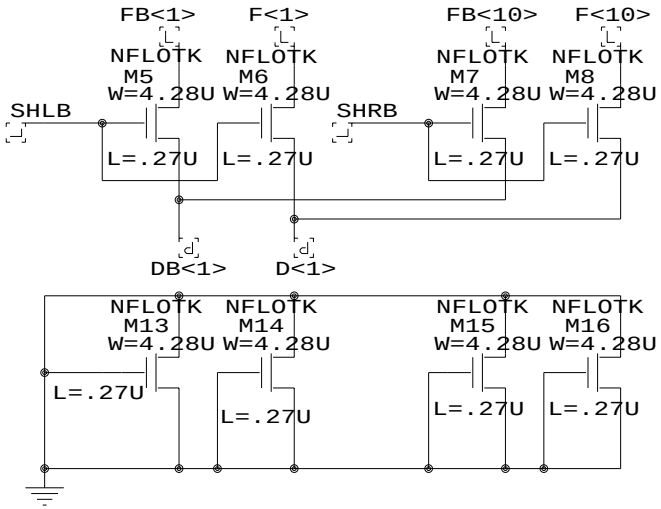
PLACED IN BANK
PLACED IN ARY32M
PLACED IN SABAND
PLACED IN HQSA



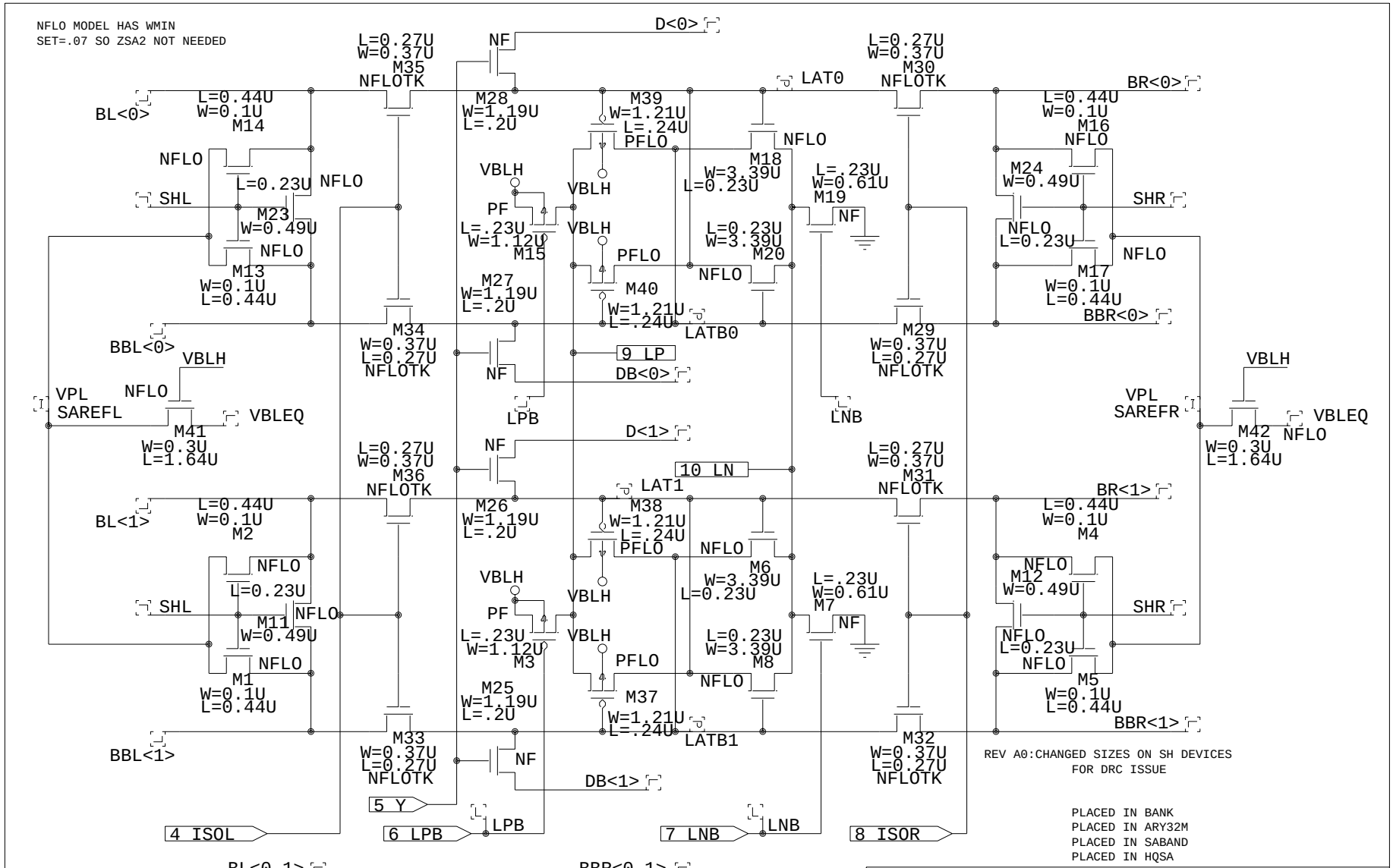


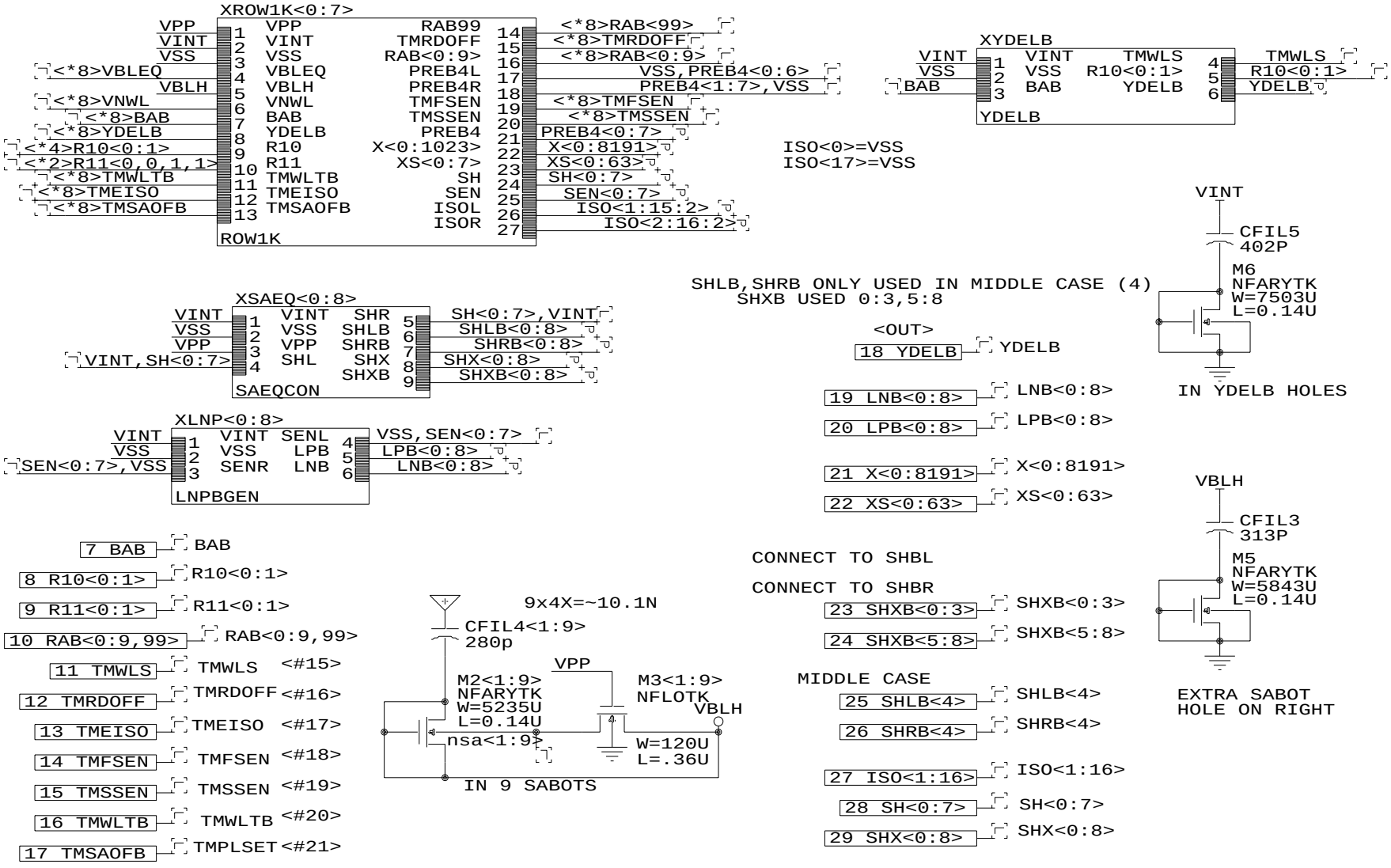


(MIMICS CENTER CASE)



UNITED MEMORIES INC. PROJECT: 128D14		
Title SH CONTROLLED DATA MUX (1 PER HQUAD)		
Size A	Document Number SHMUX	REV A
Date: October 29, 2001	Sheet 1 of 1	


NFLO MODEL HAS WMIN
SET=.07 SO ZSA2 NOT NEEDED
D<0>
L=0.27U W=0.37U M35 NFLOTK
NF
L=0.27U W=0.37U M30 NFLOTK
LAT0
BR<0>
BL<0>
L=0.44U W=0.1U M14
M28 W=1.19U L=.2U
M39 W=1.21U L=.24U PFLO
NFLO
M18 W=3.39U L=0.23U
L=.23U W=0.61U M19
L=0.44U W=0.1U M16 NFLO
M24 W=0.49U
NFLO
L=0.23U NFLO
SHL
M23 W=0.49U
VBLH
PF
L=.23U W=1.12U M15
VBLH
L=0.23U W=3.39U M20
NFLO L=0.23U
SHR
NFLO
M13 W=0.1U L=0.44U
M27 W=1.19U L=.2U
PFLO
M40 W=1.21U L=.24U
LATB0
M17 W=0.1U L=0.44U
BBR<0>
BBL<0>
M34 W=0.37U L=0.27U NFLOTK
9 LP
DB<0>
M29 W=0.37U L=0.27U NFLOTK
VBLH
VPL SAREFL
NFLO
VBLEQ
M41 W=0.3U L=1.64U
LPB
LNB
VPL SAREFR
M42 NFLO W=0.3U L=1.64U
D<1>
10 LN
LAT1
BR<1>
BL<1>
M2
M26 W=1.19U L=.2U
M38 W=1.21U L=.24U PFLO
M6 W=3.39U L=0.23U
M12 W=0.49U
M4
M11 W=0.49U
M3
M7
M8
M1 W=0.1U L=0.44U
M25 W=1.19U L=.2U
M37 W=1.21U L=.24U
LATB1
M5 W=0.1U L=0.44U
BBR<1>
BBL<1>
M33 W=0.37U L=0.27U NFLOTK
M32 W=0.37U L=0.27U NFLOTK
DB<1>
5 Y
4 ISOL
6 LPB
7 LNB
8 ISOR
REV A0:CHANGED SIZES ON SH DEVICES FOR DRC ISSUE
PLACED IN BANK
PLACED IN ARY32M
PLACED IN SABAND
PLACED IN HQSA
11 BL<0,1>
12 BBL<0,1>
13 D<0,1>
14 BR<0,1>
15 BBR<0,1>
16 DB<0,1>
17 SHL
18 SHR
1 VBLH
2 VSS
3 VBLEQ
UNITED MEMORIES INC.
PROJECT: 128D14
Title
SENSE AMP - TWO
Size A
Document Number SA2
REV A0
Date: January 22, 2002
Sheet 1 of 1



UNITED MEMORIES INC.

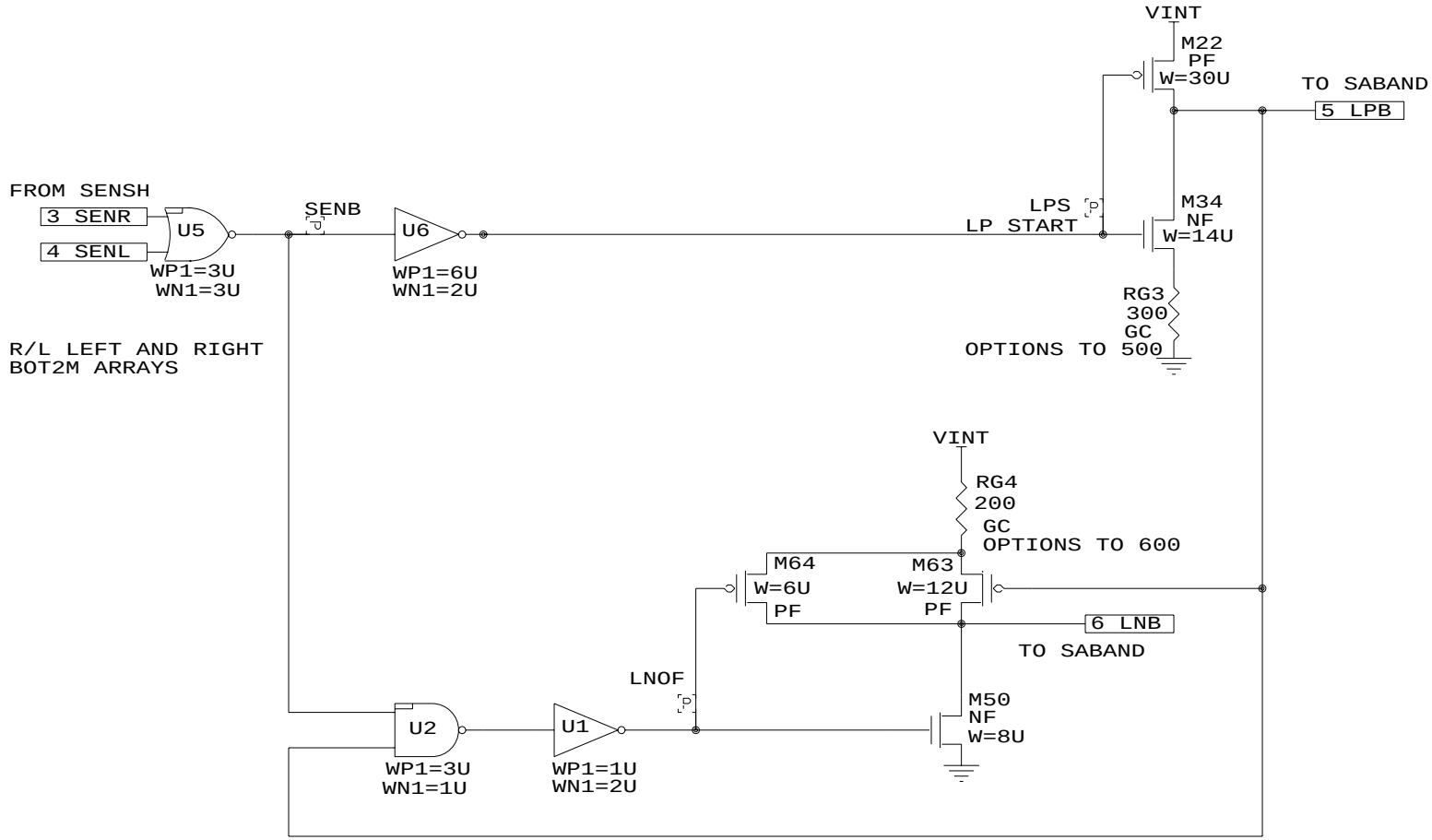
PROJECT: 128D14

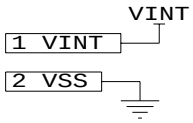
Title

ROW/SA DRIVE LOGIC FOR BOTOM OF BANK

Size	Document Number	REV
A	BNKBOT	A

Date: November 21, 2001 Sheet 1 of 1

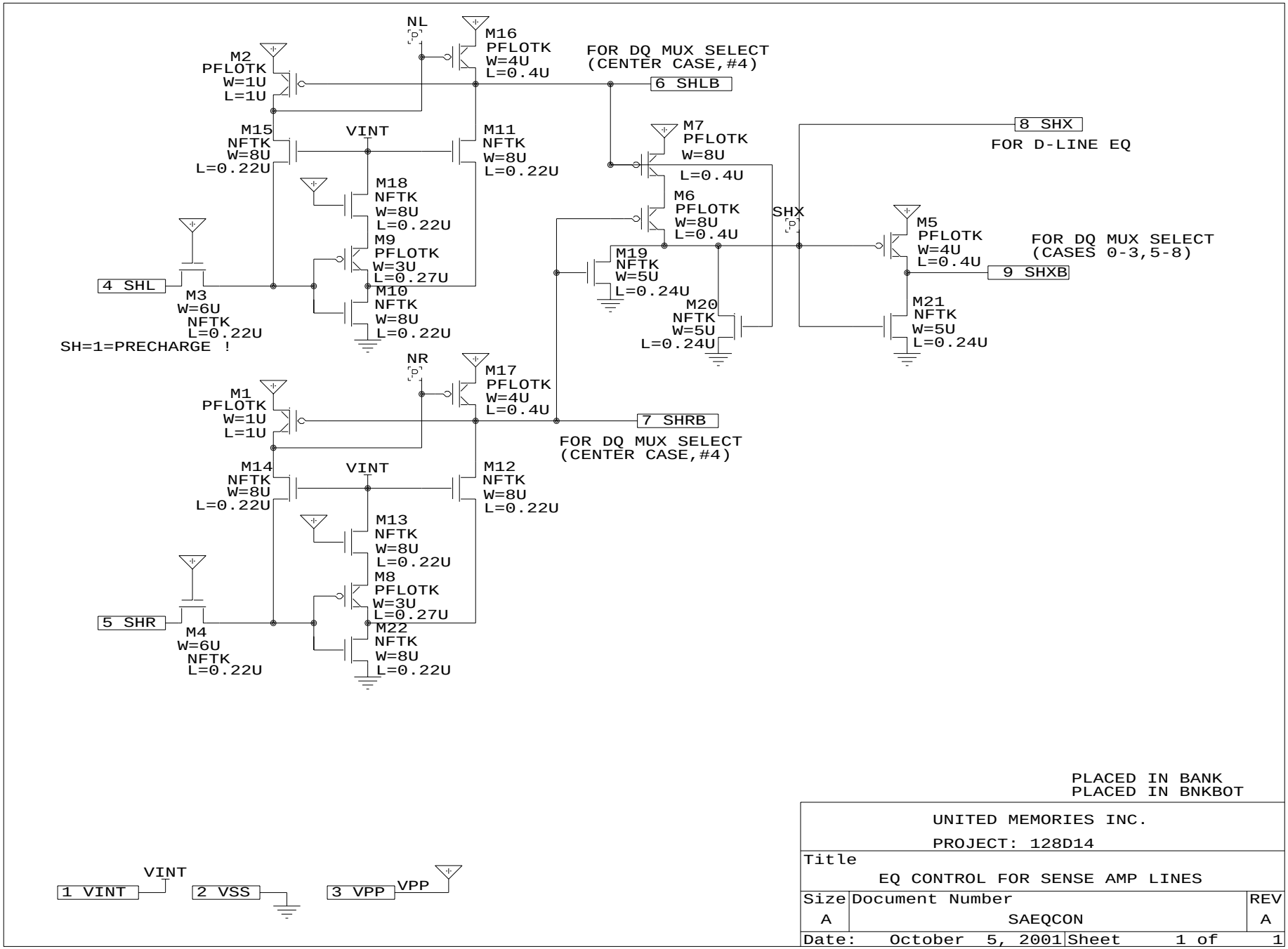




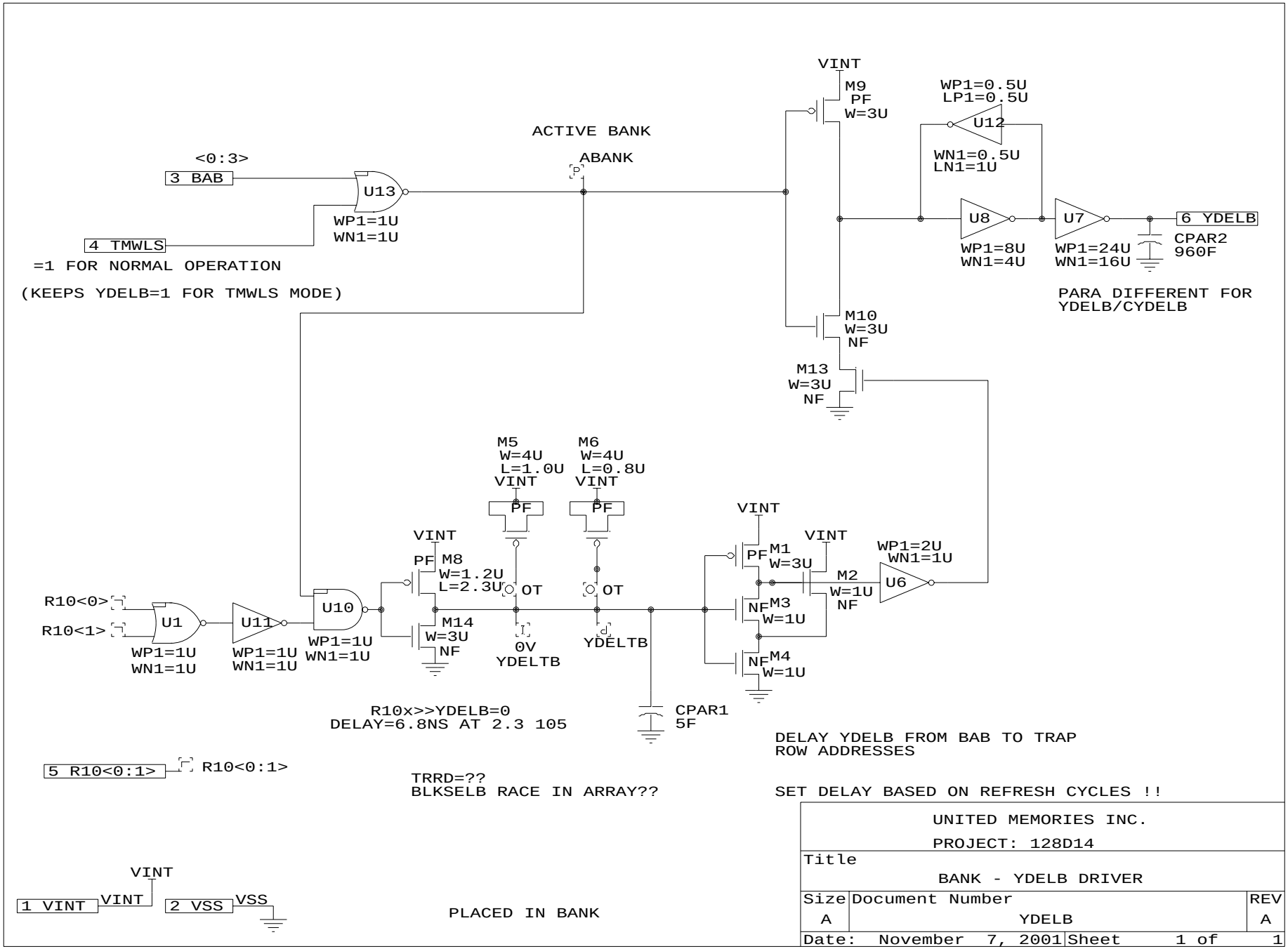
include M1 options to change resistors by 100ohms

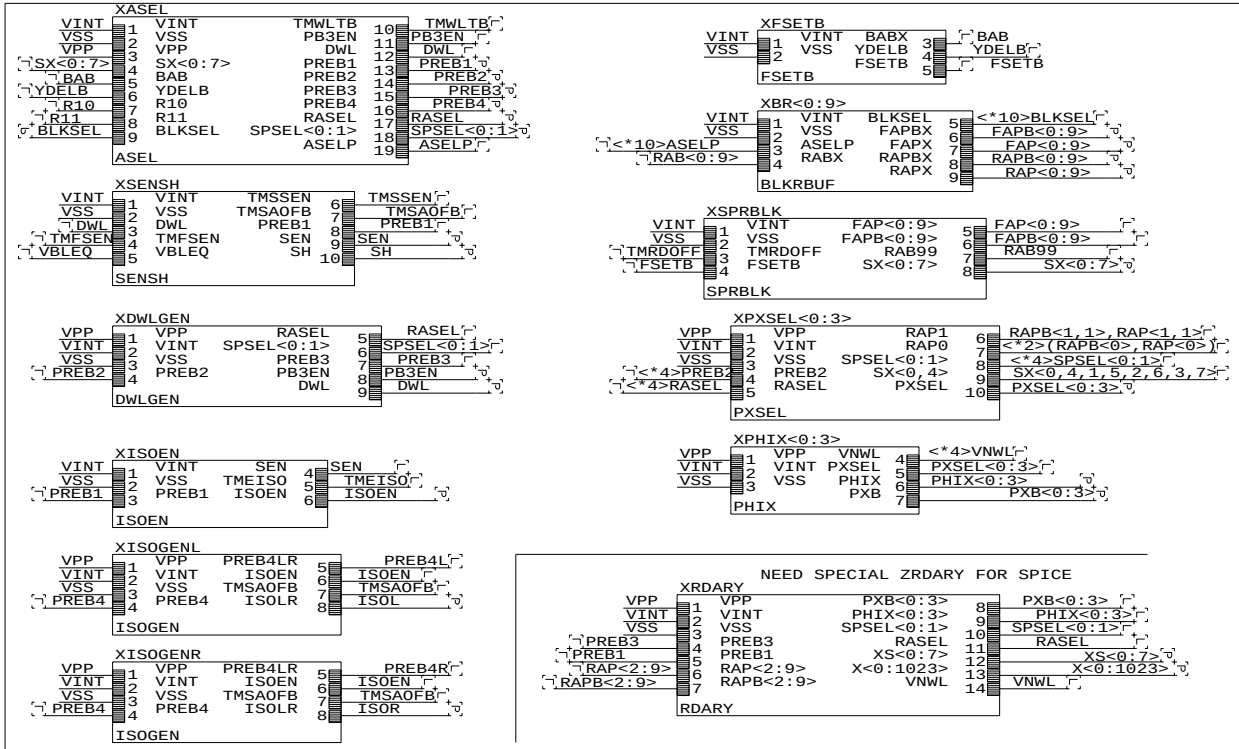
PLACED IN BANK
PLACED IN BNKBOT

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
LNB AND LPB GENERATOR		
Size	Document Number	REV
A	LNPBGEN	A
Date: July 28, 2001	Sheet 1 of 1	



UNITED MEMORIES INC. PROJECT: 128D14		
Title EQ CONTROL FOR SENSE AMP LINES		
Size A	Document Number SAEQCON	REV A
Date: October 5, 2001	Sheet 1 of 1	


VINT
M9
PF
W=3U
WP1=0.5U
LP1=0.5U
U12
WN1=0.5U
LN1=1U
ACTIVE BANK
ABANK
<0:3>
3 BAB
U13
WP1=1U
WN1=1U
4 TMWLS
=1 FOR NORMAL OPERATION
(KEEPS YDELB=1 FOR TMWLS MODE)
U8
WP1=8U
WN1=4U
U7
WP1=24U
WN1=16U
6 YDELB
CPAR2
960F
PARA DIFFERENT FOR
YDELB/CYDELB
M10
W=3U
NF
M13
W=3U
NF
M5
W=4U
L=1.0U
VINT
M6
W=4U
L=0.8U
VINT
PF
PF
VINT
PF M8
W=1.2U
L=2.3U
OT
OT
M14
W=3U
NF
0V
YDELTB
YDELTB
VINT
PF M1
W=3U
VINT
M2
W=1U
NF
WP1=2U
WN1=1U
U6
NF M3
W=1U
NF M4
W=1U
R10<0>
R10<1>
U1
WP1=1U
WN1=1U
U11
WP1=1U
WN1=1U
U10
WP1=1U
WN1=1U
R10x>>YDELB=0
DELAY=6.8NS AT 2.3 105
CPAR1
5F
DELAY YDELB FROM BAB TO TRAP
ROW ADDRESSES
5 R10<0:1>
R10<0:1>
TRRD=??
BLKSELB RACE IN ARRAY??
SET DELAY BASED ON REFRESH CYCLES !!
VINT
1 VINT
VINT
2 VSS
VSS
PLACED IN BANK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
BANK - YDELB DRIVER
Size
A
Document Number
YDELB
REV
A
Date: November 7, 2001
Sheet 1 of 1



PLACED IN BANK
PLACED IN BNKBOT

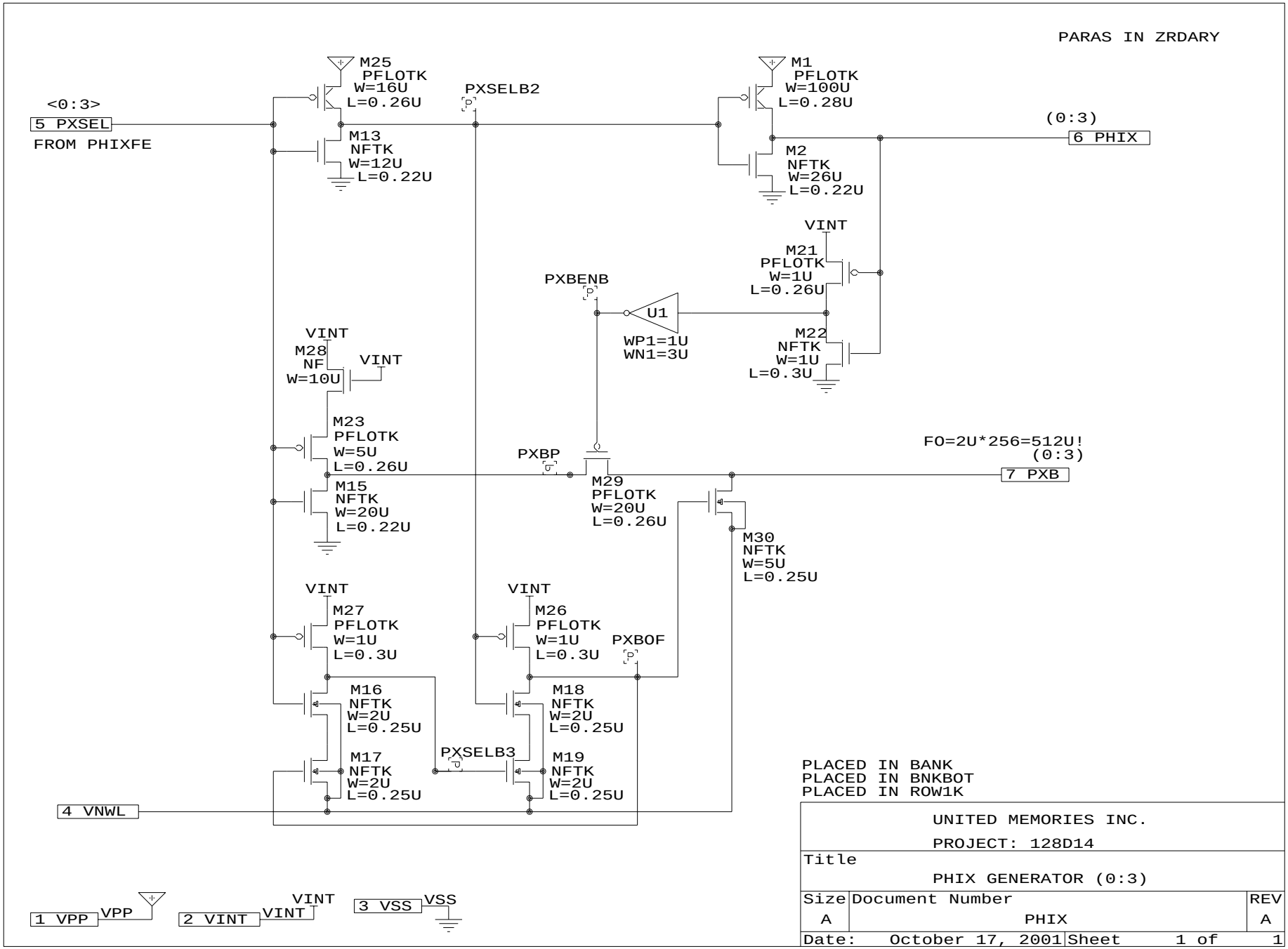
UNITED MEMORIES INC.

PROJECT: 128D14

Title: SUPPORT CIRCUITS FOR 1K ROWS

Size	Document Number	REV
B	ROW1K	A

Date: October 19, 2001 | Sheet 1 of 1



PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

UNITED MEMORIES INC. PROJECT: 128D14		
Title PHIX GENERATOR (0:3)		
Size A	Document Number PHIX	REV A
Date: October 17, 2001	Sheet 1 of 1	

CONTROLS 2M ROW ARRAY SELECT AND PRECHARGE

INPUTS
BAB-BANK ACTIVE BAR-LOW ON BANK SELECT (ACTIVE OR PRECHARGE)
R10,R11- MAIN ARRAY SELECT ADDRESSES, =1 AFTER ROWENB FIRES
(THESE ADDRESSES RESET=0 AFTER EACH SELECTION)

YDELB- DELAY AFTER BAB=0, LOCKS OUT ALL FUTURE ADDRESSES
WHILE BANK IS ACTIVE

SX<0:7>-FUSE MATCH COMPARE FOR THE 8 SPARES
=1 IF A MATCH IS PRESENT

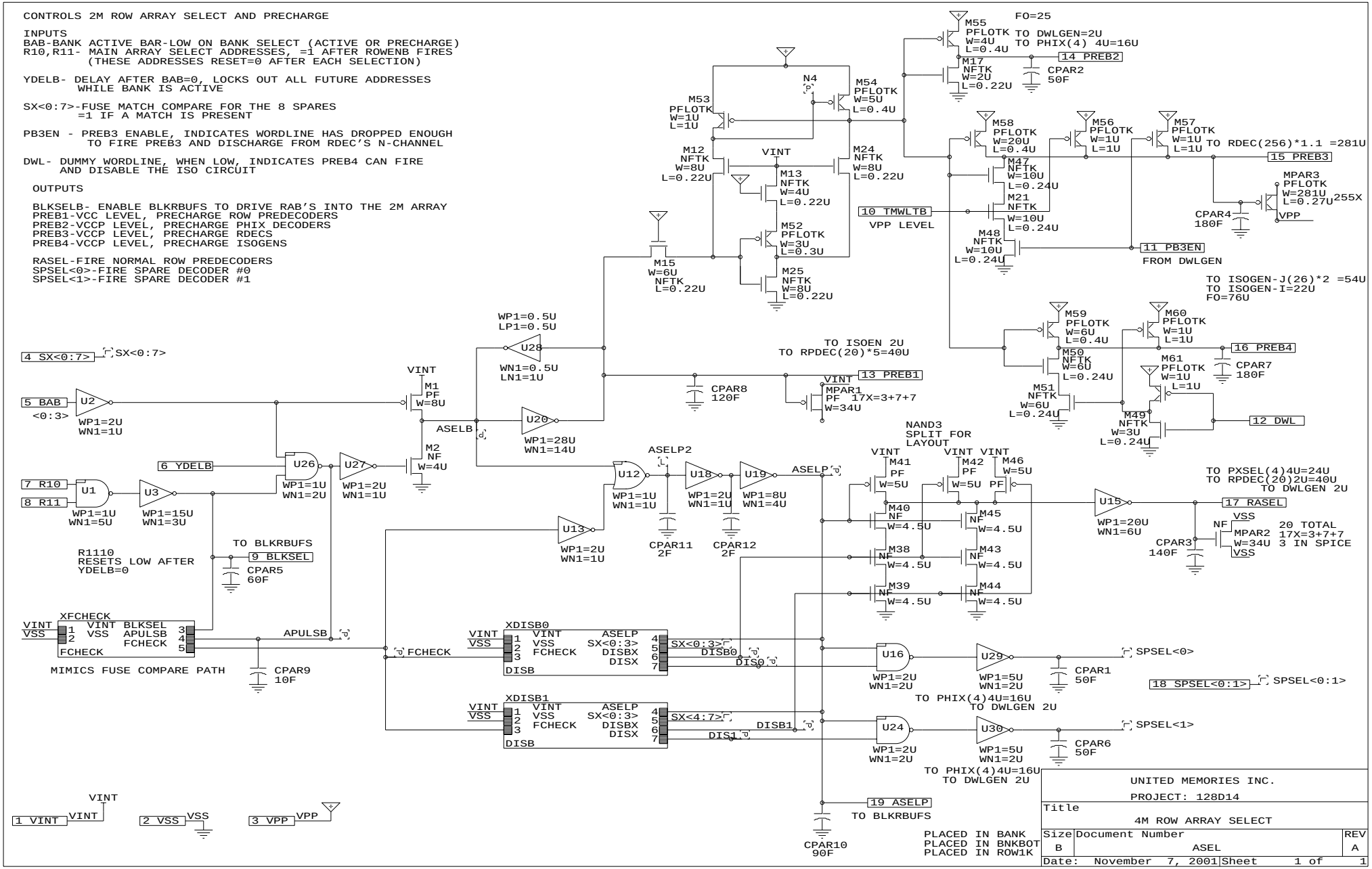
PB3EN - PREB3 ENABLE, INDICATES WORDLINE HAS DROPPED ENOUGH
TO FIRE PREB3 AND DISCHARGE FROM RDEC'S N-CHANNEL

DWL- DUMMY WORDLINE, WHEN LOW, INDICATES PREB4 CAN FIRE
AND DISABLE THE ISO CIRCUIT

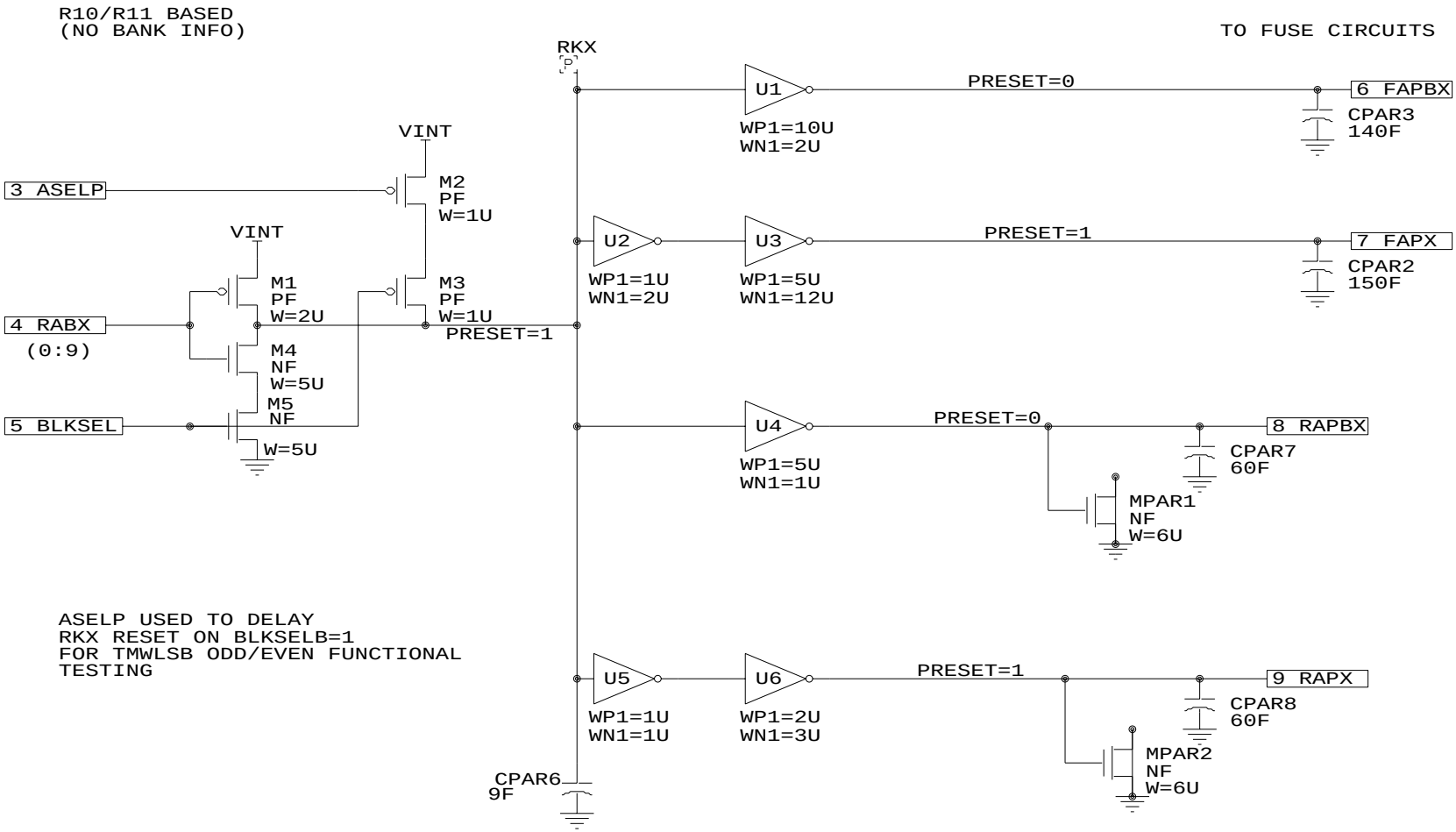
OUTPUTS

BLKSELB- ENABLE BLKRBUFS TO DRIVE RAB'S INTO THE 2M ARRAY
PREB1-VCC LEVEL, PRECHARGE ROW PREDECODERS
PREB2-VCCP LEVEL, PRECHARGE PHIX DECODERS
PREB3-VCCP LEVEL, PRECHARGE RDECS
PREB4-VCCP LEVEL, PRECHARGE ISOGENS

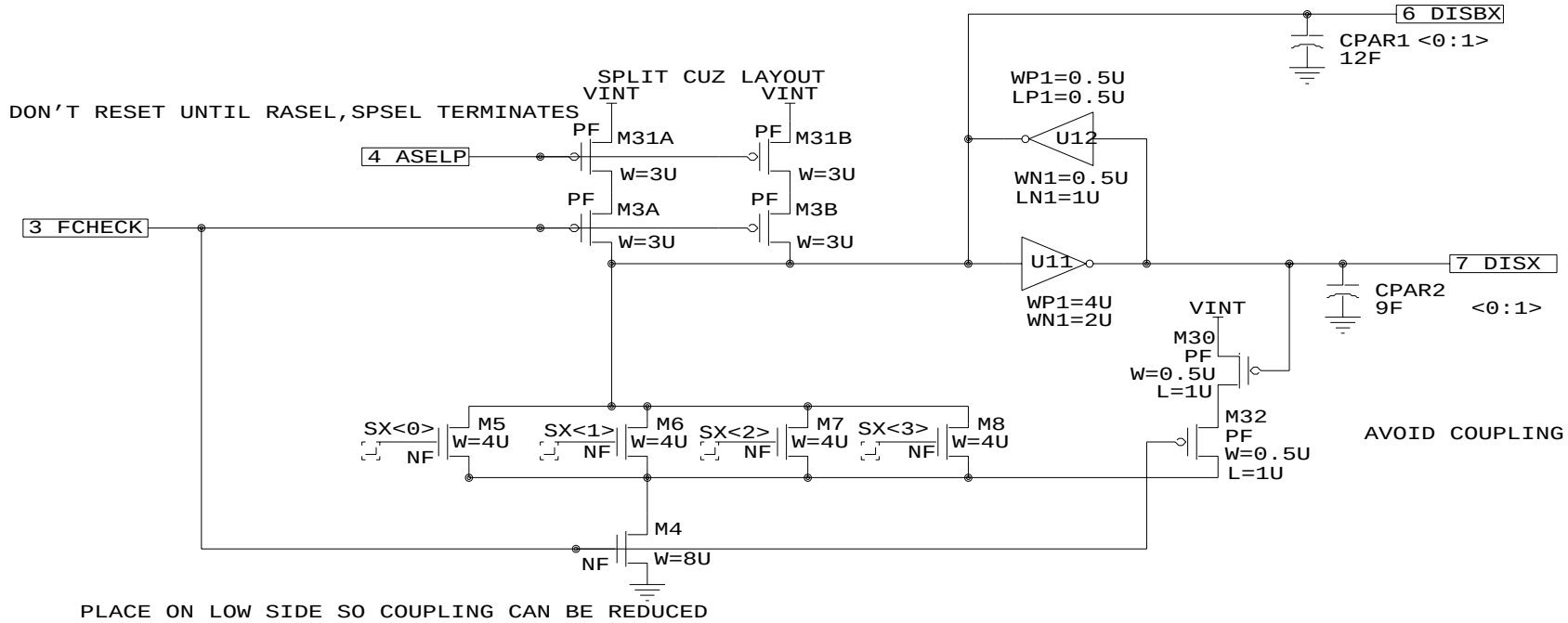
RASEL-FIRE NORMAL ROW PREDECODERS
SPSEL<0>-FIRE SPARE DECODER #0
SPSEL<1>-FIRE SPARE DECODER #1



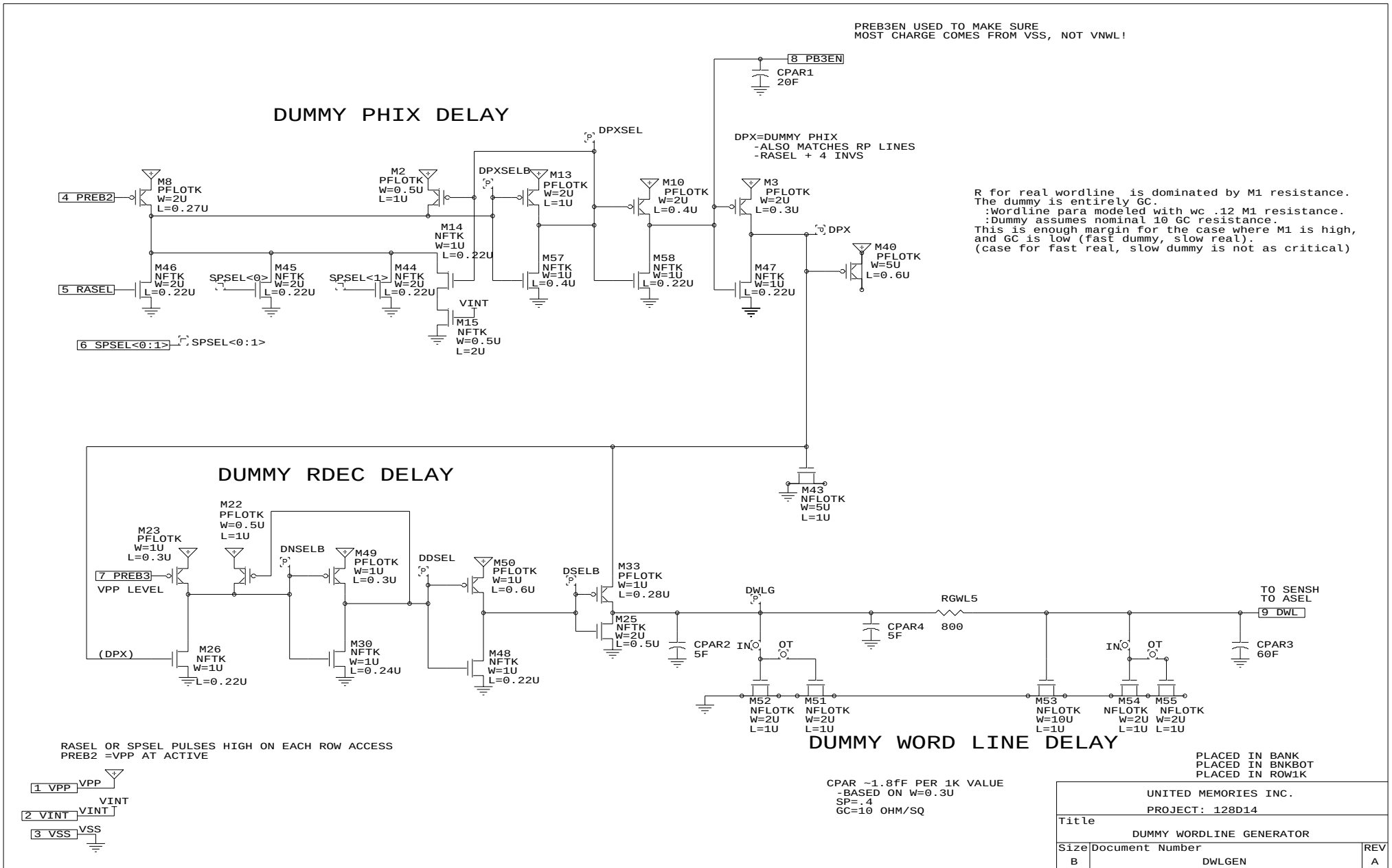
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	4M ROW ARRAY SELECT	
Size B	Document Number ASEL	REV A
Date: November 7, 2001	Sheet 1 of 1	

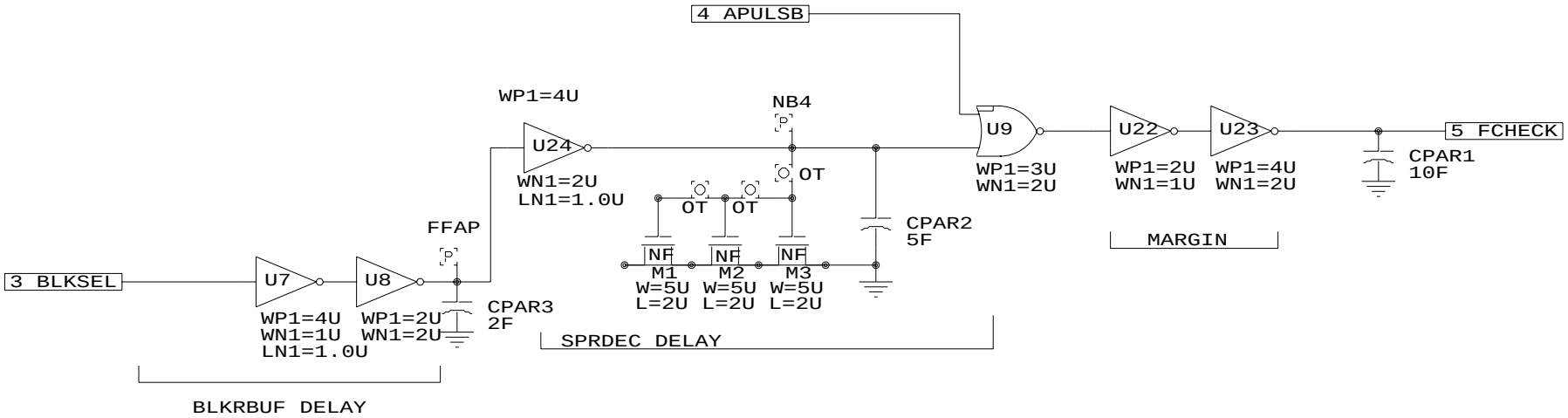


UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
ROW ADDRESS DRIVERS / PER BLOCK		
Size	Document Number	REV
A	BLKRBUF	A
Date: November 7, 2001	Sheet 1 of 1	



UNITED MEMORIES INC.		
PROJECT: 128D14		
Title DISABLE ROW SELECTION FOR SPARE ENABLE		
Size A	Document Number DISB	REV A
Date: November 7, 2001	Sheet 1 of 1	


PREB3EN USED TO MAKE SURE
MOST CHARGE COMES FROM VSS, NOT VNWL!
8 PB3EN
CPAR1
20F
DUMMY PHIX DELAY
DPXSEL
DPX=DUMMY PHIX
-ALSO MATCHES RP LINES
-RASEL + 4 INVS
4 PREB2
M8
PFLOTK
W=2U
L=0.27U
M2
PFLOTK
W=0.5U
L=1U
DPXSELB
M13
PFLOTK
W=2U
L=1U
M10
PFLOTK
W=2U
L=0.4U
M3
PFLOTK
W=2U
L=0.3U
R for real wordline is dominated by M1 resistance.
The dummy is entirely GC.
:Wordline para modeled with wc .12 M1 resistance.
:Dummy assumes nominal 10 GC resistance.
This is enough margin for the case where M1 is high,
and GC is low (fast dummy, slow real).
(case for fast real, slow dummy is not as critical)
DPX
M14
NFTK
W=1U
L=0.22U
M40
PFLOTK
W=5U
L=0.6U
M46
NFTK
W=2U
L=0.22U
5 RASEL
SPSEL<0>
M45
NFTK
W=2U
L=0.22U
SPSEL<1>
M44
NFTK
W=2U
L=0.22U
M57
NFTK
W=1U
L=0.4U
M58
NFTK
W=1U
L=0.22U
M47
NFTK
W=1U
L=0.22U
VINT
M15
NFTK
W=0.5U
L=2U
6 SPSEL<0:1>
SPSEL<0:1>
DUMMY RDEC DELAY
M43
NFLOTK
W=5U
L=1U
M22
PFLOTK
W=0.5U
L=1U
M23
PFLOTK
W=1U
L=0.3U
DNSELB
M49
PFLOTK
W=1U
L=0.3U
DDSEL
M50
PFLOTK
W=1U
L=0.6U
DSELB
M33
PFLOTK
W=1U
L=0.28U
7 PREB3
VPP LEVEL
DWLG
RGWL5
TO SENSH
TO ASEL
9 DWL
M25
NFTK
W=2U
L=0.5U
CPAR2
5F
CPAR4
5F
800
CPAR3
60F
(DPX)
M26
NFTK
W=1U
L=0.22U
M30
NFTK
W=1U
L=0.24U
M48
NFTK
W=1U
L=0.22U
IN
OT
IN
OT
M52
NFLOTK
W=2U
L=1U
M51
NFLOTK
W=2U
L=1U
M53
NFLOTK
W=10U
L=1U
M54
NFLOTK
W=2U
L=1U
M55
NFLOTK
W=2U
L=1U
DUMMY WORD LINE DELAY
RASEL OR SPSEL PULSES HIGH ON EACH ROW ACCESS
PREB2 =VPP AT ACTIVE
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
1 VPP
VPP
VINT
2 VINT
VINT
3 VSS
VSS
CPAR ~1.8fF PER 1K VALUE
-BASED ON W=0.3U
SP=.4
GC=10 OHM/SQ
UNITED MEMORIES INC.
PROJECT: 128D14
Title
DUMMY WORDLINE GENERATOR
Size
B
Document Number
DWLGEN
REV
A
Date: November 21, 2001
Sheet 1 of 1

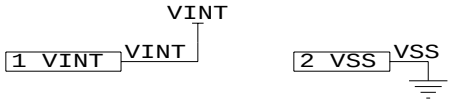


MIMICS FUSE COMPARE PATH

1X PER 4M ARRAY

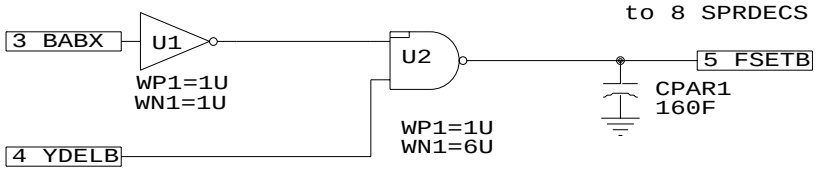
WHEN TO CHECK ROW FUSE COMPARE ??

PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN ASEL

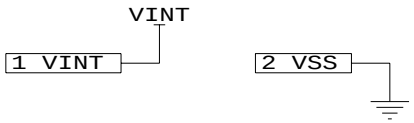


UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
FCHECK TIMER GENERATOR		
Size	Document Number	REV
A	FCHECK	A
Date: November 7, 2001	Sheet 1 of 1	

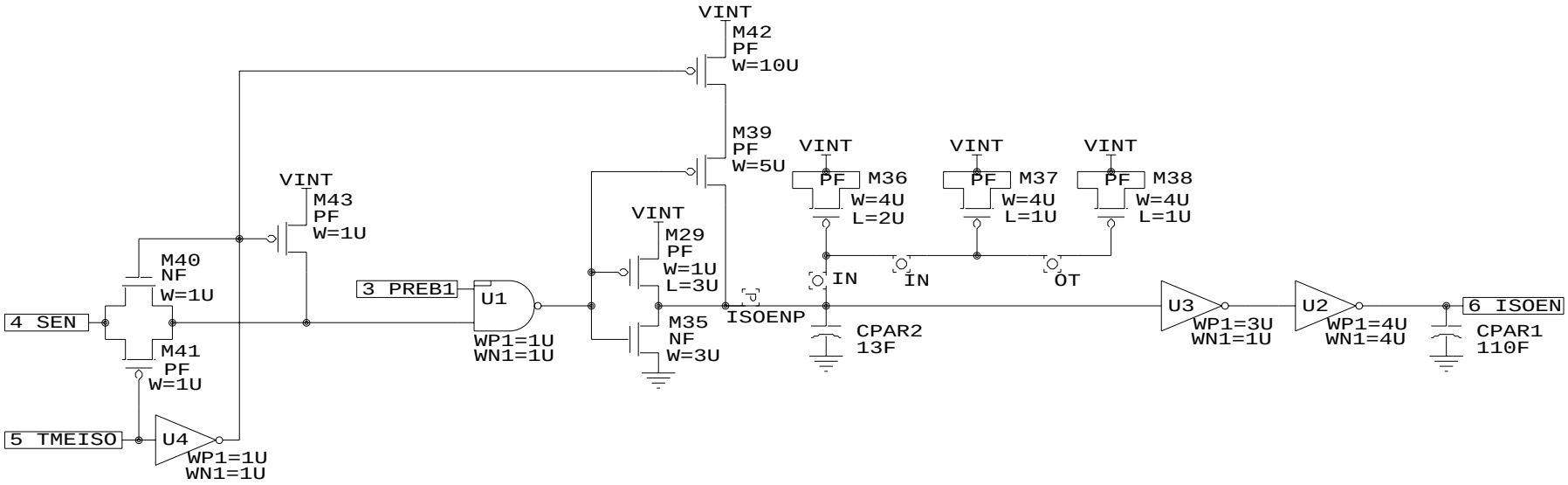
LOW PULSE ON BAB=0 TO SET FUSES



PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K



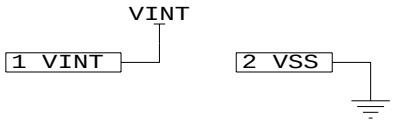
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title SPARE ROW - SET PULSE STROBE (BASED ON BAB)		
Size A	Document Number FSETB	REV A
Date: August 24, 2001	Sheet 1 of 1	



TEST MODE FOR "EARLY" ISO

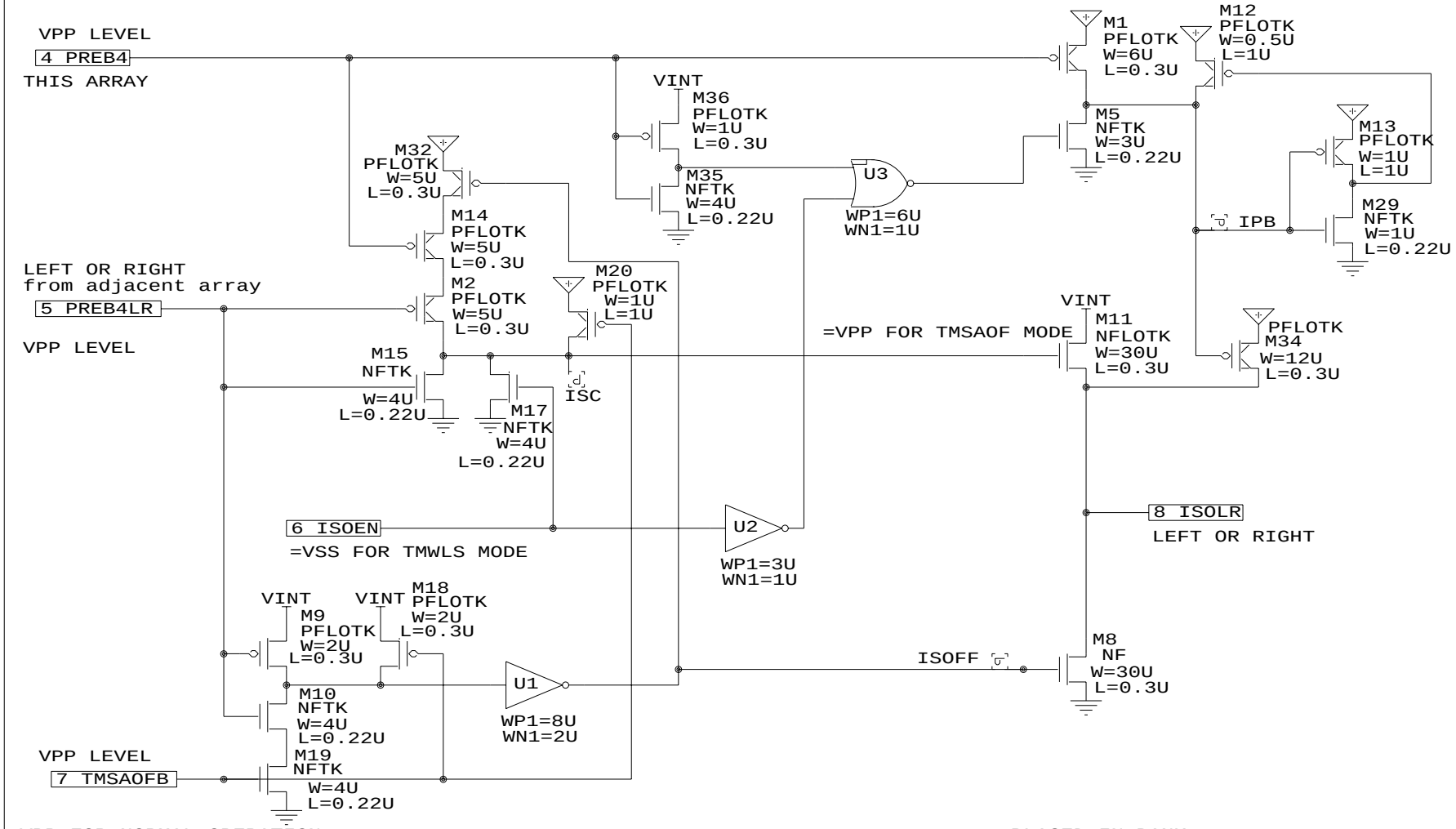
PREB1 IS NEEDED IN CASE OF EARLY ISO OPTION

PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

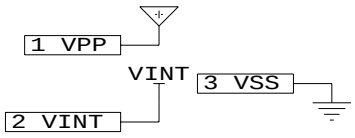


UNITED MEMORIES INC. PROJECT: 128D14		
Title ISOEN GENERATOR		
Size A	Document Number ISOEN	REV A
Date: November 9, 2001	Sheet 1 of 1	

MAKE SURE ISOEN TURN'S OFF B4 PREB4

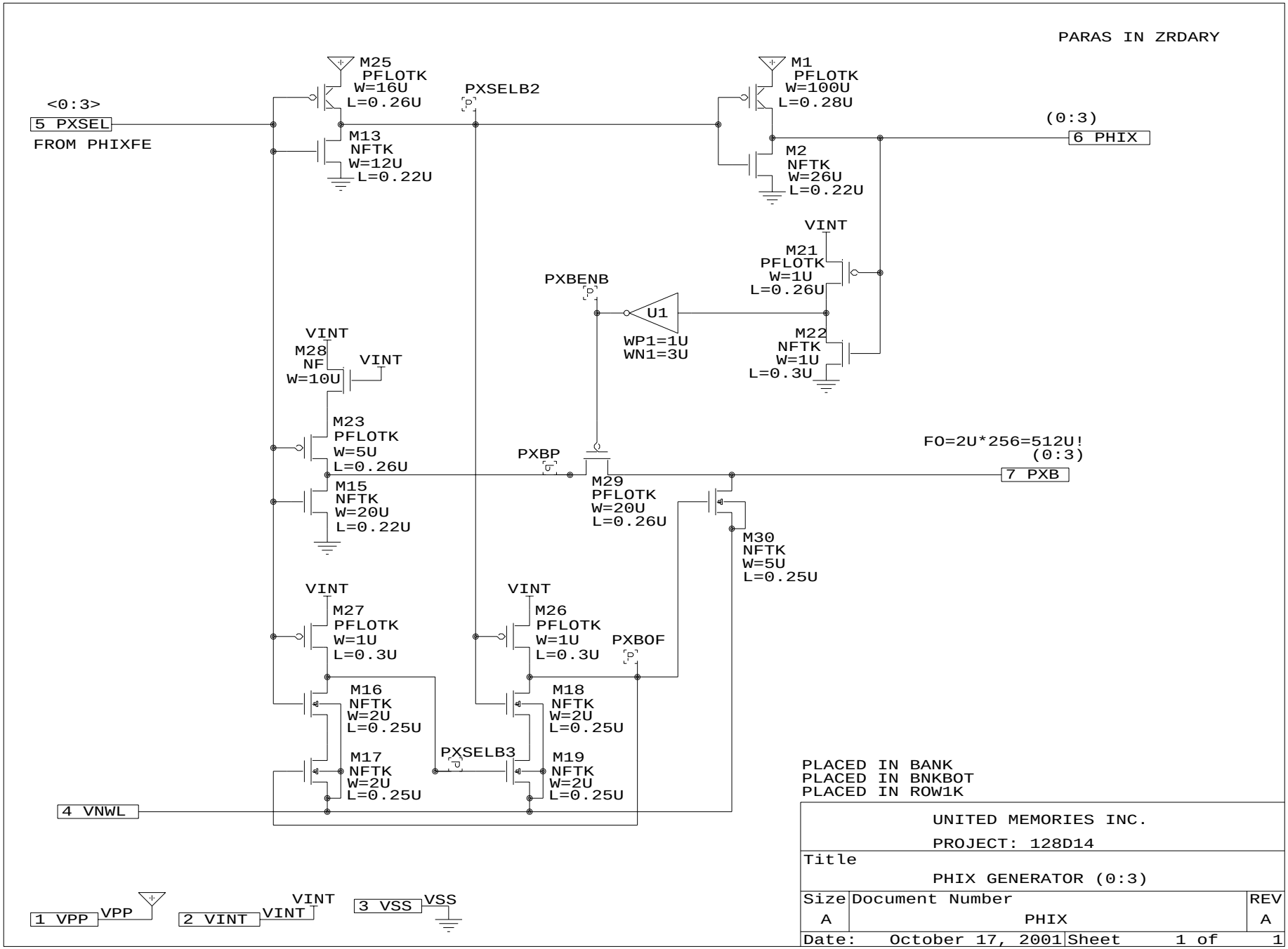


PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K



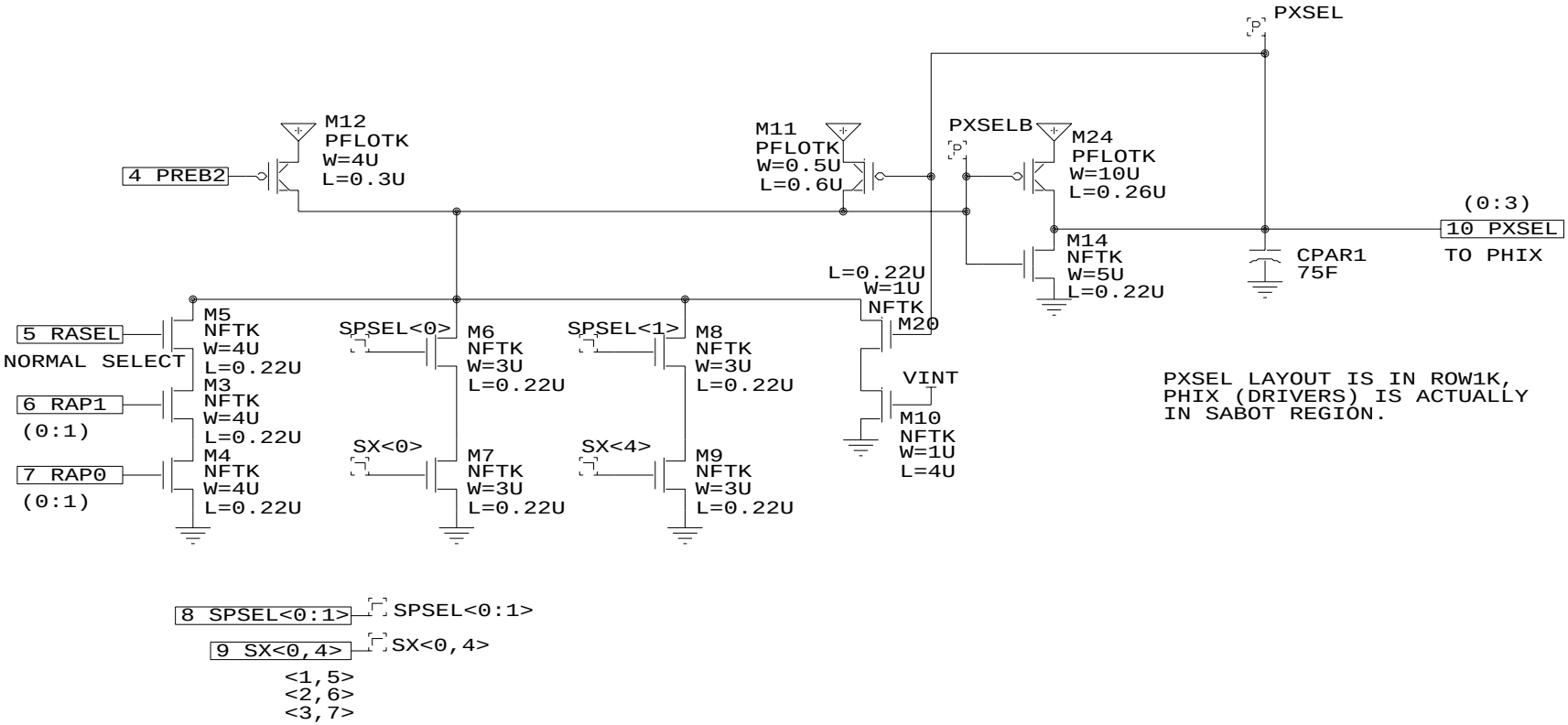
The PP type transistors need to be in a common N Well tied to VCCP, and the normal P type transistors need to be in an N Well tied to VCC.

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	ISO GENERATOR	
Size A	Document Number ISOGEN	REV A
Date: September 4, 2001	Sheet 1 of 1	



PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

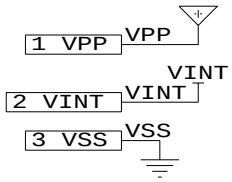
UNITED MEMORIES INC. PROJECT: 128D14		
Title PHIX GENERATOR (0:3)		
Size A	Document Number PHIX	REV A
Date: October 17, 2001	Sheet 1 of 1	



RASEL OR SPSEL PULSES HIGH ON EACH ROW ACCESS

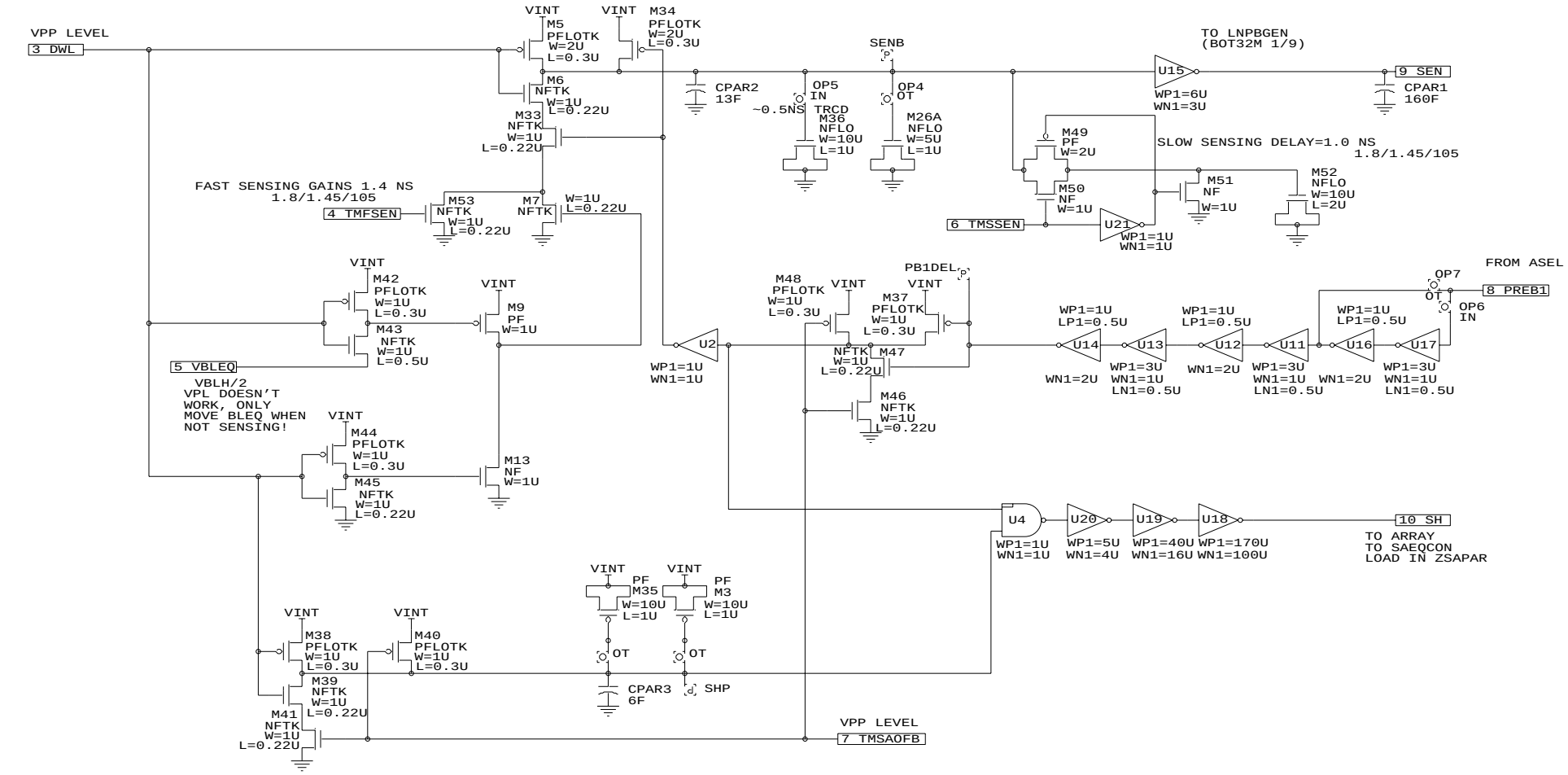
PREB2 =VPP AT PRECHARGE

SELECT INFORMATION IS LATCHED UNTIL PRECHARGE
TO ALLOW FUNCTION OF MULTIPLE WORD LINE SELECT MODE (TMWLS)



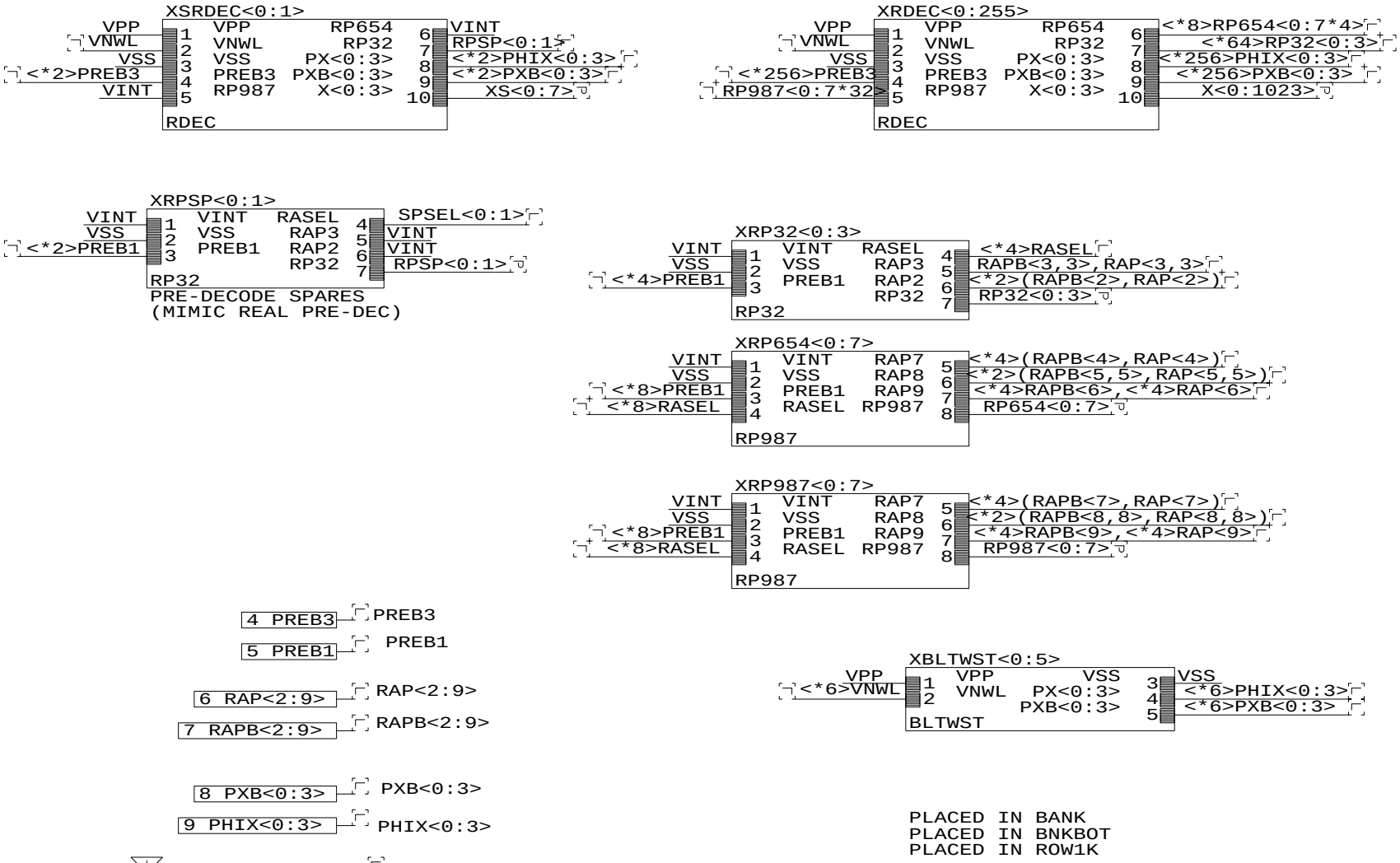
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title PXSEL GENERATOR (0:3) - (PHIX FRONT END)		
Size A	Document Number PXSEL	REV A
Date: November 7, 2001	Sheet 1 of 1	



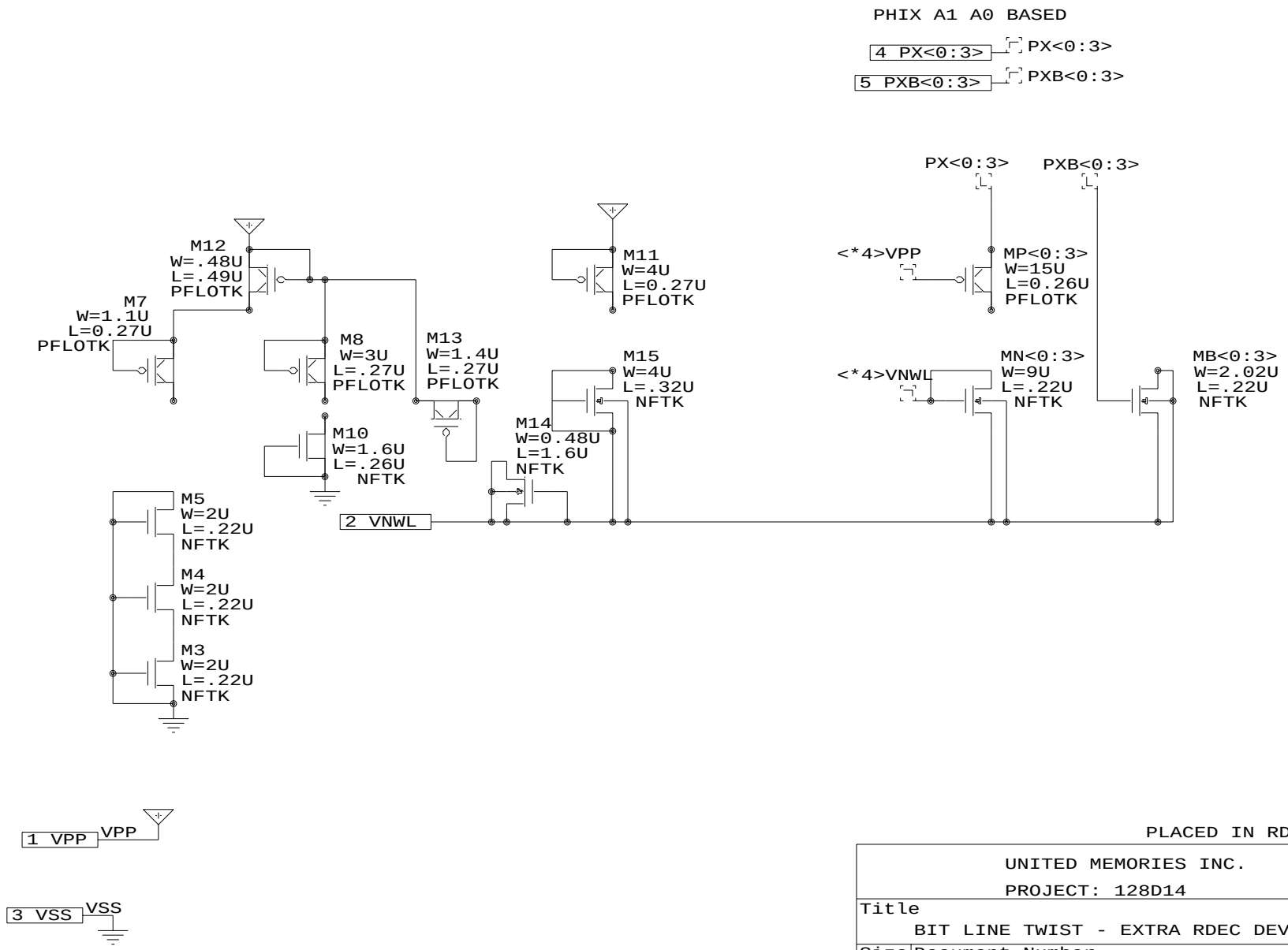
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
SEN and SH GENERATOR		
Size	Document Number	REV
B	SENSH	A
Date: November 7, 2001	Sheet 1 of 1	



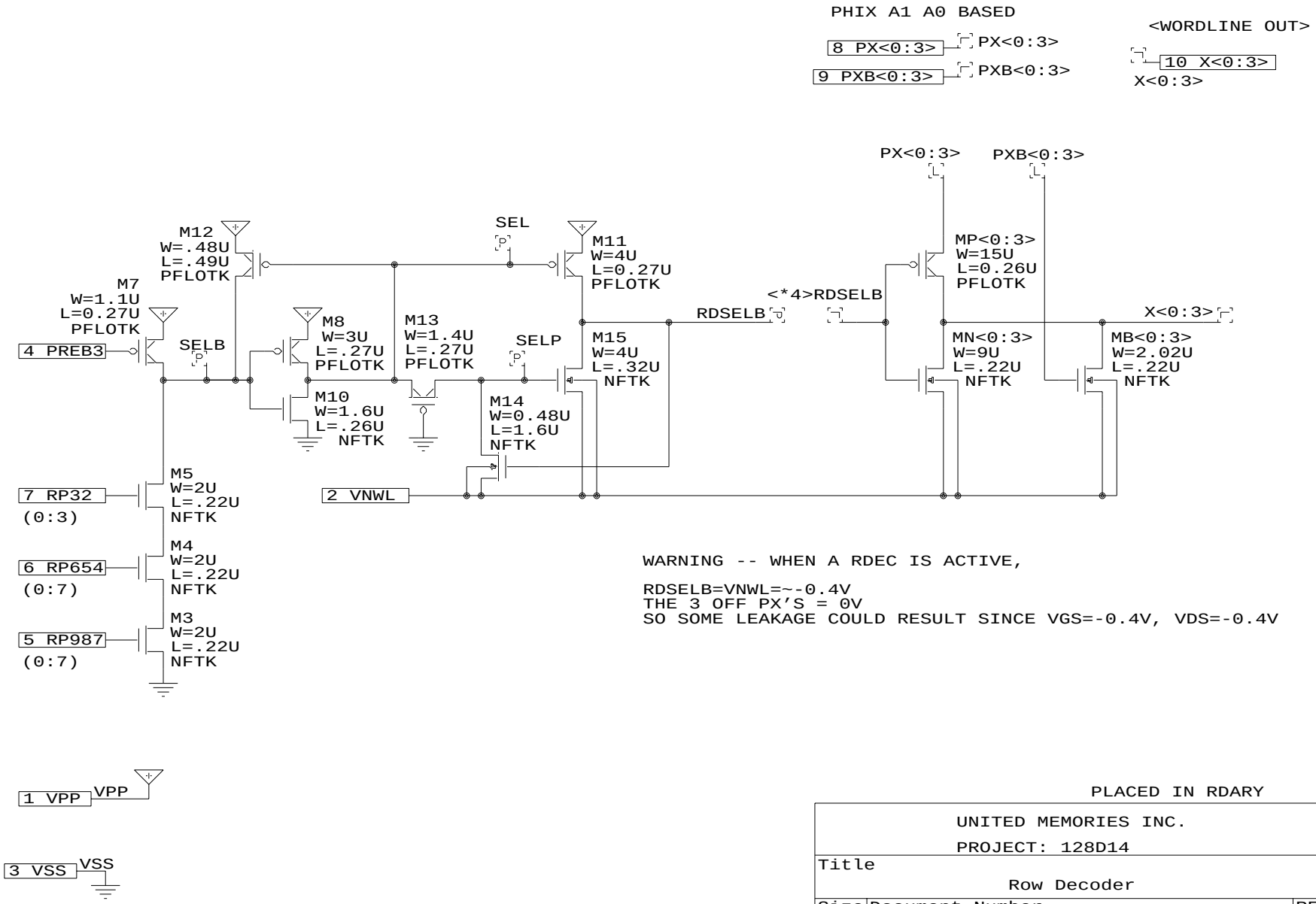
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	RDEC ARRAY	
Size A	Document Number RDARY	REV A
Date: September 7, 2001	Sheet 1 of 1	



PLACED IN RDARY

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title BIT LINE TWIST - EXTRA RDEC DEVICES		
Size A	Document Number BLTWST	REV A
Date: September 7, 2001	Sheet 1 of 1	

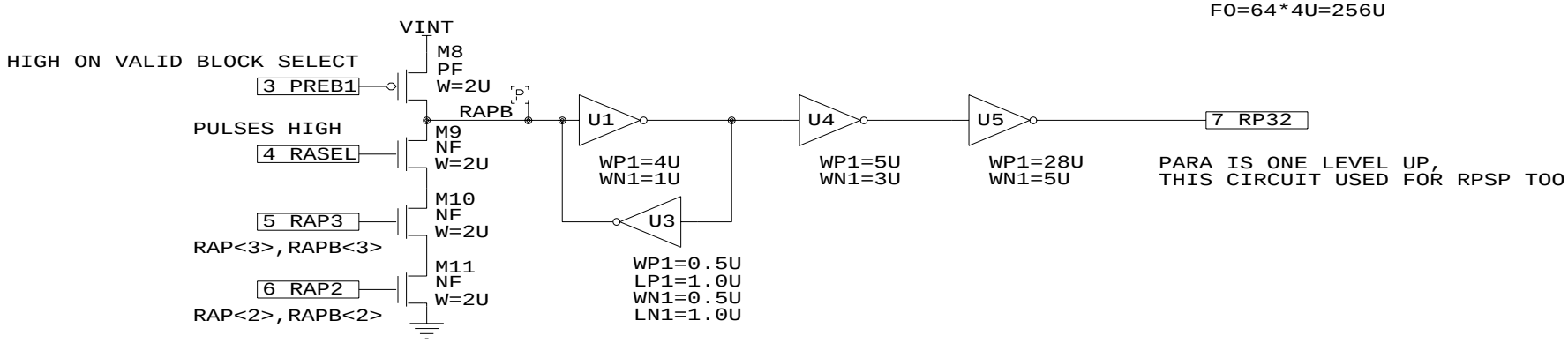


PLACED IN RDARY

UNITED MEMORIES INC. PROJECT: 128D14		
Title Row Decoder		
Size A	Document Number RDEC	REV A
Date: December 10, 2001	Sheet 1 of 1	

RASEL IS FOR NORMAL ADDRESS SELECTION, NOT SPARES

TO RDEC
256 TOTAL RDECS
EACH ADDRESS HITS 1/4
64 FOR EACH R32<X>
FO=64*4U=256U

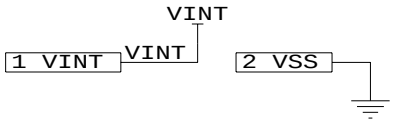


6X, R32<0:3>, RPSP<0:1>

GENERATES PREDECODED INPUTS TO RDECS
IFF A SPARE IS NOT TO BE SELECTED

OUTPUT STAYS LATCHED UNTIL PRECHARGE TO ALLOW

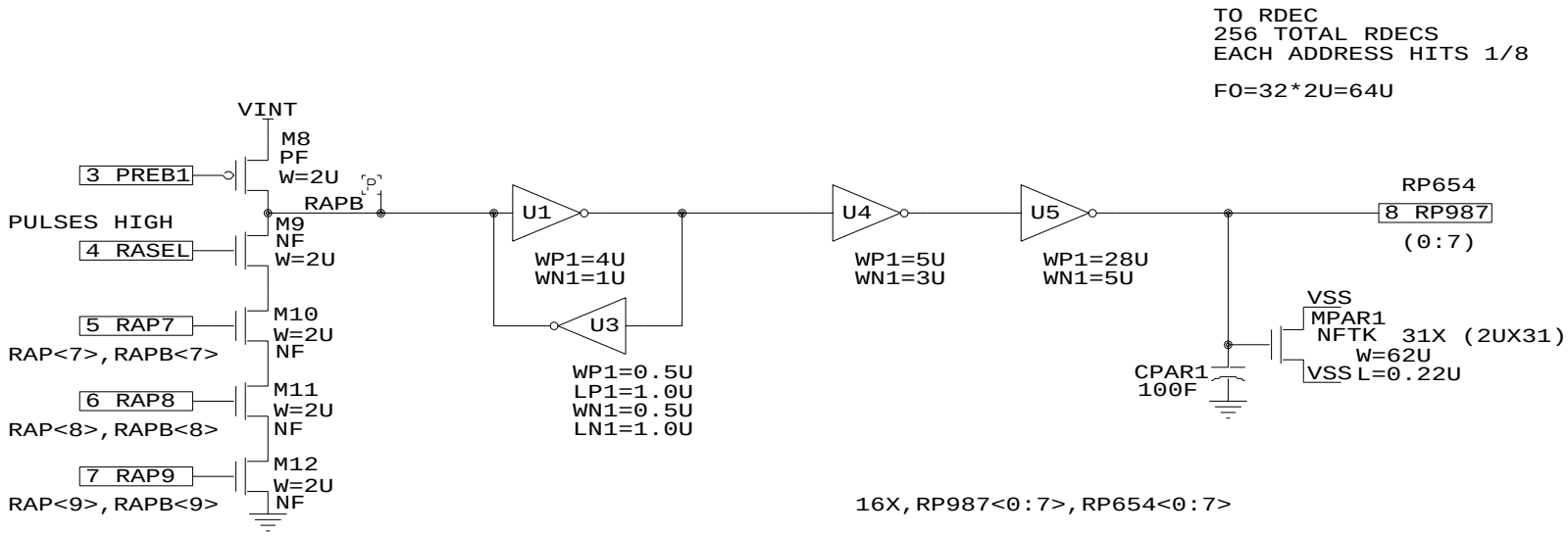
MULTIPLE WORLD LINE SELECT MODE (TMWLS)



PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN RDARY

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title ROW PRE-DECODER (2 INPUT) R32(0:3)		
Size A	Document Number RP32	REV A
Date: August 24, 2001	Sheet 1 of 1	

RASEL IS FOR NORMAL ADDRESS SELECTION, NOT SPARES

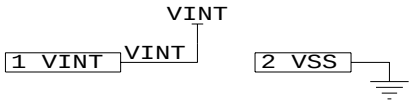


16X,RP987<0:7>,RP654<0:7>

GENERATES PREDECODED INPUTS TO RDECS
IFF A SPARE IS NOT TO BE SELECTED

OUTPUT STAYS LATCHED UNTIL PRECHARGE TO ALLOW

MULTIPLE WORLD LINE SELECT MODE (TMWLS)

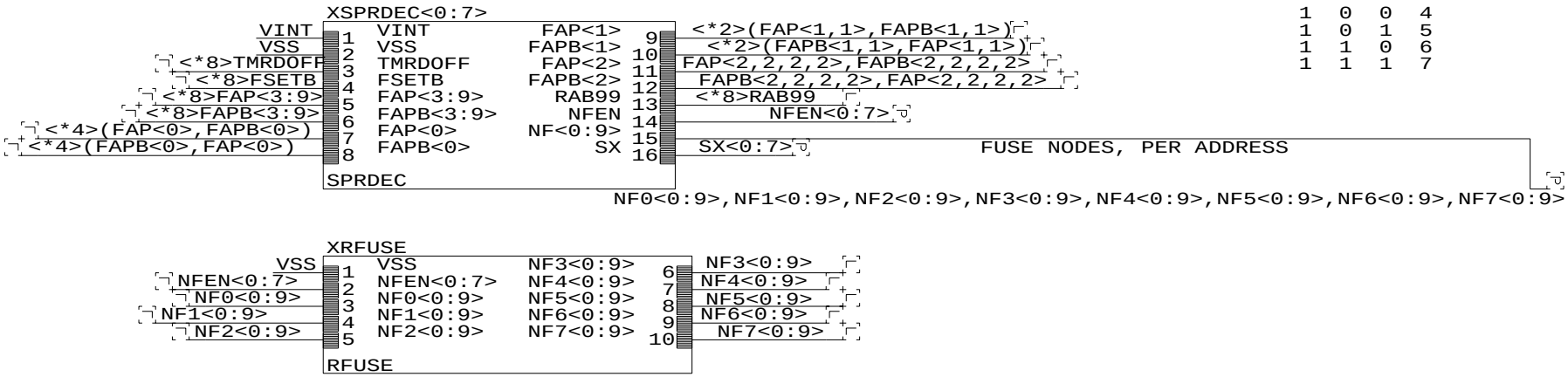


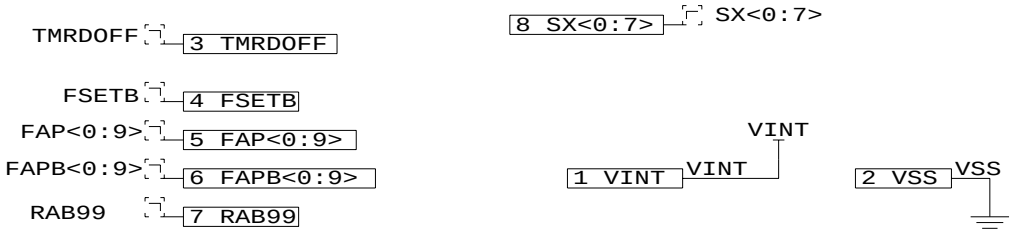
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN RDARY

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title ROW PRE-DECODER (3 INPUT) R987,R654		
Size A	Document Number RP987	REV A
Date: August 24, 2001	Sheet 1 of 1	

FAP 2,1,0 PROGRAMMED TO ALLOW PREFUSE TESTING OF SPARES

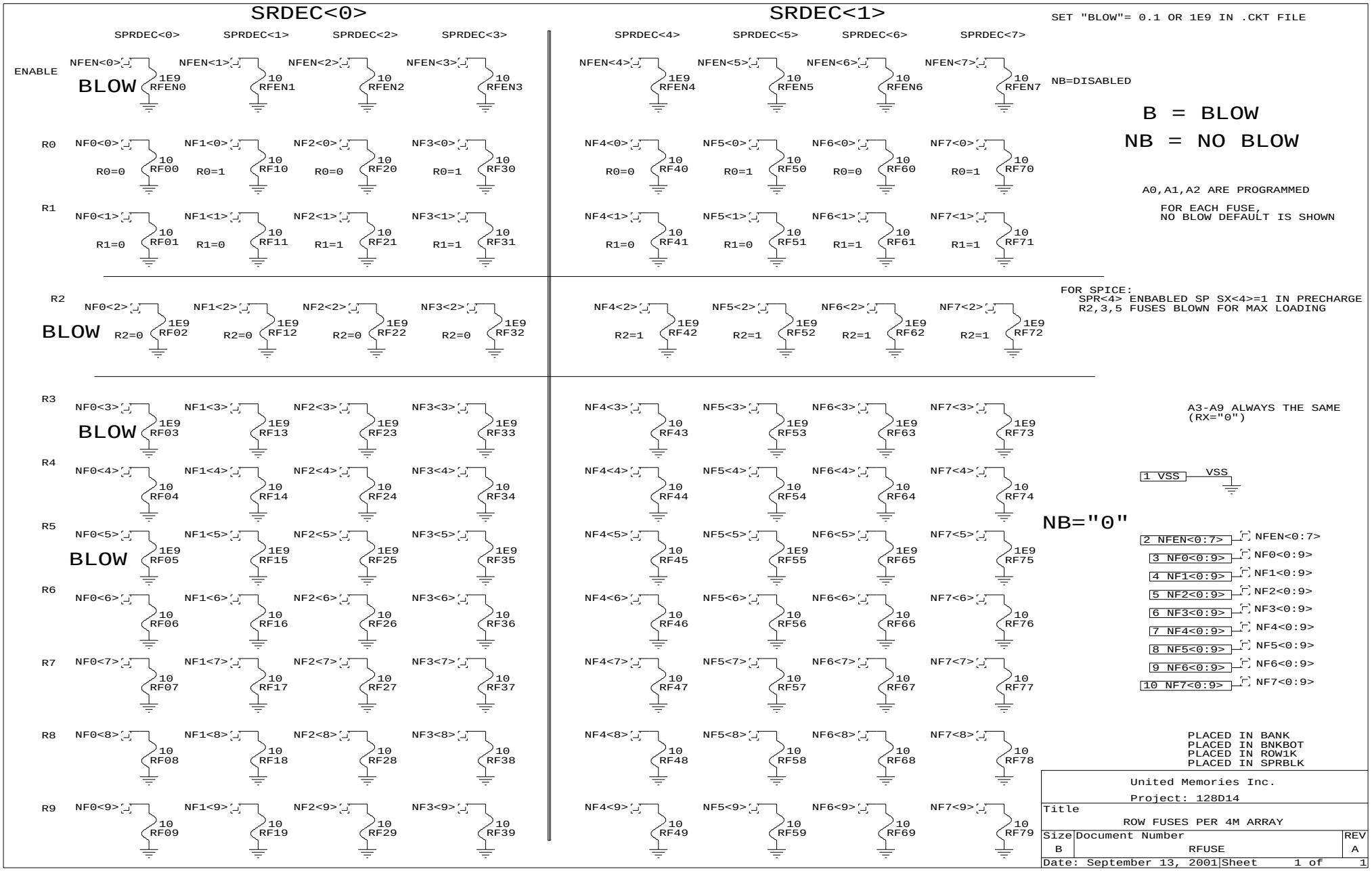
R2	R1	R0	SPARE
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

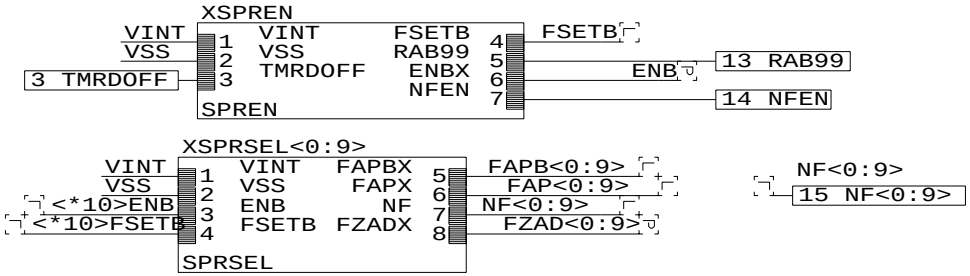




PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
SPARE ROW BLOCK (1X/4MEG)		
Size A	Document Number SPRBLK	REV A
Date: July 27, 2001	Sheet 1 of 1	


SRDEC<0>
SRDEC<1>
SET "BLOW"= 0.1 OR 1E9 IN .CKT FILE
SPRDEC<0> SPRDEC<1> SPRDEC<2> SPRDEC<3>
SPRDEC<4> SPRDEC<5> SPRDEC<6> SPRDEC<7>
ENABLE
NFEN<0> NFEN<1> NFEN<2> NFEN<3>
NFEN<4> NFEN<5> NFEN<6> NFEN<7>
BLOW
1E9 RFEN0
10 RFEN1 RFEN2 RFEN3 RFEN4 RFEN5 RFEN6 RFEN7
NB=DISABLED
B = BLOW
NB = NO BLOW
R0
NF0<0> NF1<0> NF2<0> NF3<0>
NF4<0> NF5<0> NF6<0> NF7<0>
R0=0 R0=1 R0=0 R0=1
10 RF00 RF10 RF20 RF30 RF40 RF50 RF60 RF70
A0,A1,A2 ARE PROGRAMMED
FOR EACH FUSE,
NO BLOW DEFAULT IS SHOWN
R1
NF0<1> NF1<1> NF2<1> NF3<1>
NF4<1> NF5<1> NF6<1> NF7<1>
R1=0 R1=0 R1=1 R1=1
10 RF01 RF11 RF21 RF31 RF41 RF51 RF61 RF71
R2
NF0<2> NF1<2> NF2<2> NF3<2>
NF4<2> NF5<2> NF6<2> NF7<2>
BLOW
R2=0 R2=0 R2=0 R2=0
1E9 RF02 RF12 RF22 RF32
R2=1 R2=1 R2=1 R2=1
1E9 RF42 RF52 RF62 RF72
FOR SPICE:
SPR<4> ENBABLED SP SX<4>=1 IN PRECHARGE
R2,3,5 FUSES BLOWN FOR MAX LOADING
R3
NF0<3> NF1<3> NF2<3> NF3<3>
NF4<3> NF5<3> NF6<3> NF7<3>
BLOW
1E9 RF03 RF13 RF23 RF33
10 RF43 RF53 RF63 RF73
A3-A9 ALWAYS THE SAME
(RX="0")
R4
NF0<4> NF1<4> NF2<4> NF3<4>
NF4<4> NF5<4> NF6<4> NF7<4>
10 RF04 RF14 RF24 RF34 RF44 RF54 RF64 RF74
1 VSS
VSS
R5
NF0<5> NF1<5> NF2<5> NF3<5>
NF4<5> NF5<5> NF6<5> NF7<5>
BLOW
1E9 RF05 RF15 RF25 RF35
10 RF45
1E9 RF55 RF65 RF75
NB="0"
2 NFEN<0:7>
NFEN<0:7>
3 NF0<0:9>
NF0<0:9>
4 NF1<0:9>
NF1<0:9>
5 NF2<0:9>
NF2<0:9>
6 NF3<0:9>
NF3<0:9>
7 NF4<0:9>
NF4<0:9>
8 NF5<0:9>
NF5<0:9>
9 NF6<0:9>
NF6<0:9>
10 NF7<0:9>
NF7<0:9>
R6
NF0<6> NF1<6> NF2<6> NF3<6>
NF4<6> NF5<6> NF6<6> NF7<6>
10 RF06 RF16 RF26 RF36 RF46 RF56 RF66 RF76
R7
NF0<7> NF1<7> NF2<7> NF3<7>
NF4<7> NF5<7> NF6<7> NF7<7>
10 RF07 RF17 RF27 RF37 RF47 RF57 RF67 RF77
R8
NF0<8> NF1<8> NF2<8> NF3<8>
NF4<8> NF5<8> NF6<8> NF7<8>
10 RF08 RF18 RF28 RF38 RF48 RF58 RF68 RF78
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN SPRBLK
R9
NF0<9> NF1<9> NF2<9> NF3<9>
NF4<9> NF5<9> NF6<9> NF7<9>
10 RF09 RF19 RF29 RF39 RF49 RF59 RF69 RF79
United Memories Inc.
Project: 128D14
Title
ROW FUSES PER 4M ARRAY
Size B
Document Number
RFUSE
REV A
Date: September 13, 2001
Sheet 1 of 1

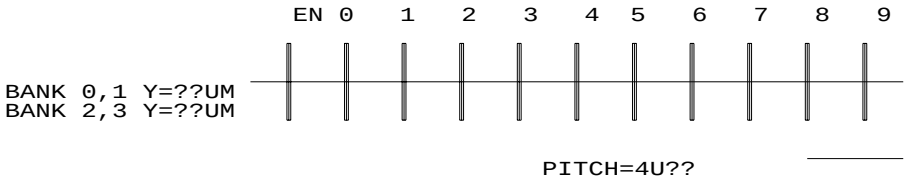


TO ENABLE SPARE ADDRESS

-BLOW ENABLE FUSE
-BLOW FUSE FOR EACH A9-A3 ADDRESS BIT THAT = "1"
A2A1A0 A8-A2

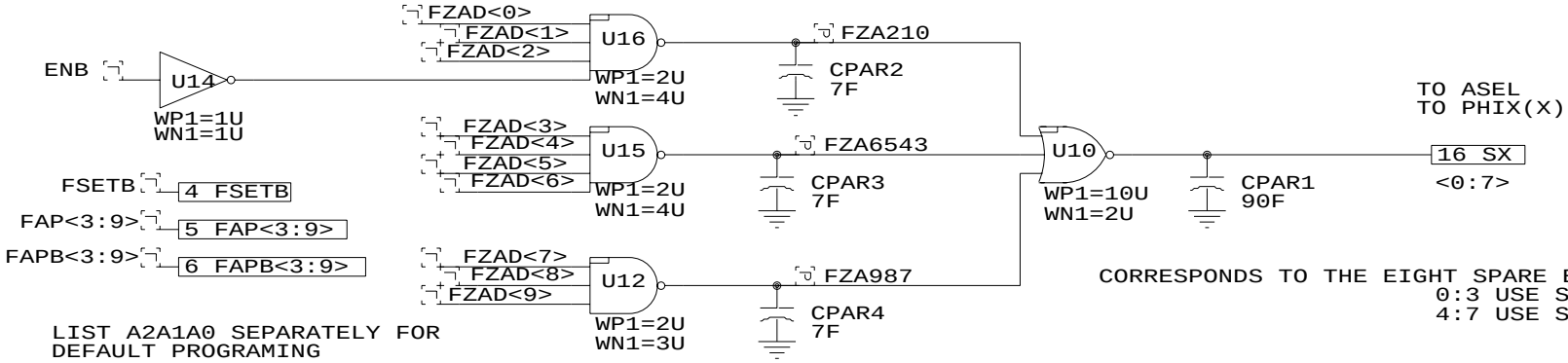
(SX 0 DEFAULT ADDRESS=000 0000..)
(SX 1 DEFAULT ADDRESS=001 0000..)
(SX 2 DEFAULT ADDRESS=010 0000..)
(SX 3 DEFAULT ADDRESS=011 0000..)

(SX 4 DEFAULT ADDRESS=100 0000..)
(SX 5 DEFAULT ADDRESS=101 0000..)
(SX 6 DEFAULT ADDRESS=110 0000..)
(SX 7 DEFAULT ADDRESS=111 0000..)



A2A1A0 DETERMINE DEFAULT
ADDRESS FOR TESTING SPARES

ALL FUSE NODES PASSED UP TO 1X PER 2M BLOCK

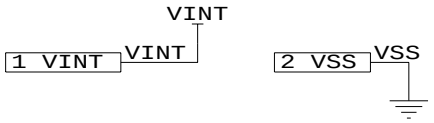


CORRESPONDS TO THE EIGHT SPARE ELEMENTS
0:3 USE SRDEC<0>
4:7 USE SRDEC<1>

FSETB — 4 FSETB
FAP<3:9> — 5 FAP<3:9>
FAPB<3:9> — 6 FAPB<3:9>

LIST A2A1A0 SEPARATELY FOR
DEFAULT PROGRAMING

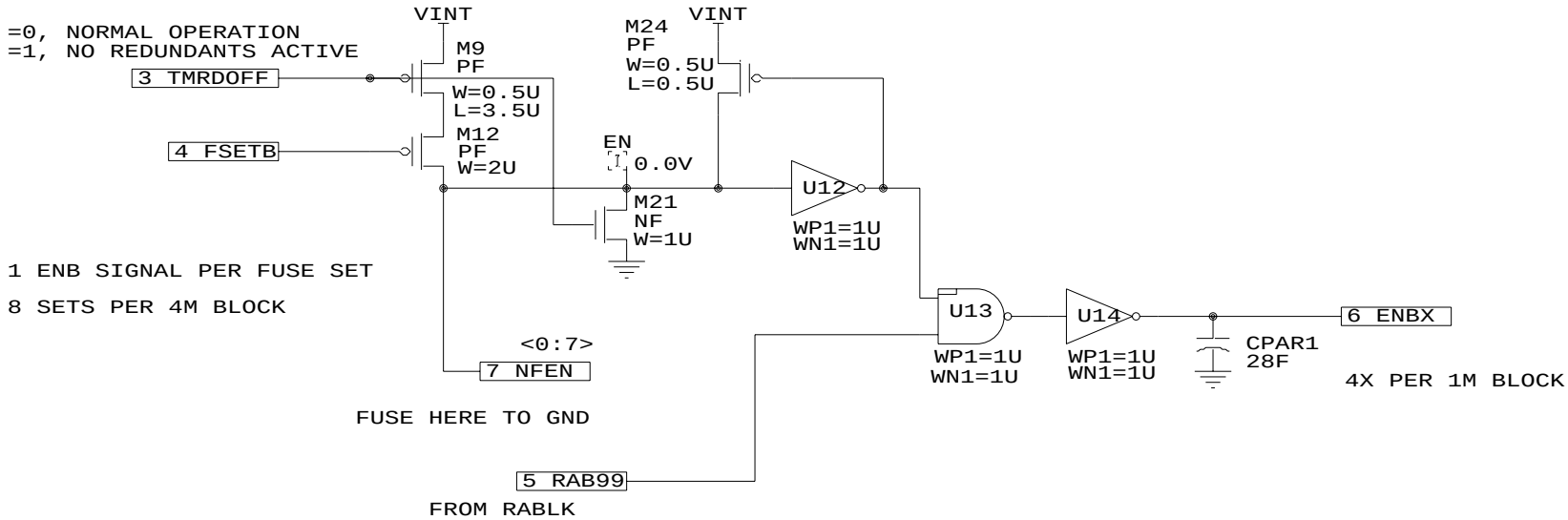
FAP<0> — 7 FAP<0>
FAPB<0> — 8 FAPB<0>
FAP<1> — 9 FAP<1>
FAPB<1> — 10 FAPB<1>
FAP<2> — 11 FAP<2>
FAPB<2> — 12 FAPB<2>



PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN SPRBLK

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
SPARE ROW DECODER (8X/4MEG)		
Size A	Document Number SPRDEC	REV A
Date: November 7, 2001	Sheet 1 of 1	

M21 (N-CHAN) NEEDED TO SUPPORT RDOFF MODE

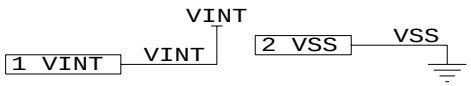


=1, NORMAL OPERATION OR TMRDEN=1 AND LDMPAD=0
=0, ALL REDUNDANTS ACTIVE,TMRDEN=1 AND LDMPAD=1
(LDMPAD NOT ACTIVE IN REDPAD MODE,
JUST COUNTING FROM RABUF<99>)

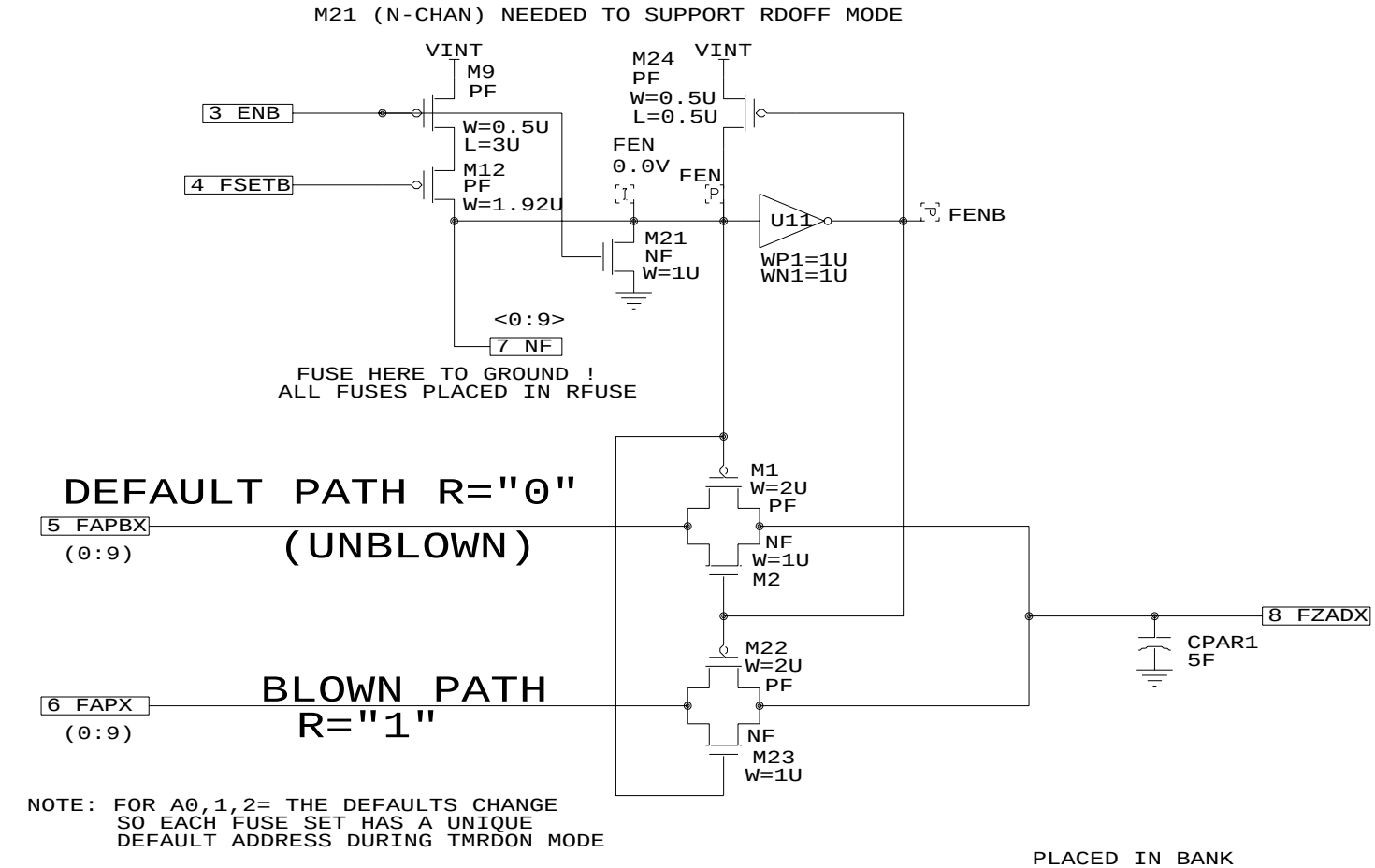
ALL FUSES PLACED IN "RFUSE"
TO ENABLE SPICE=LVS FUNCTION

BLOW THIS FUSE TO ENABLE A SPARE DECODER
(8X PER 4M BOT)

PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN SPRBLK
PLACED IN SPRDEC

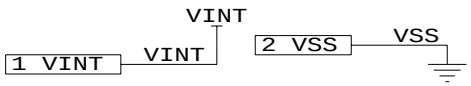


United Memories Inc.		
Project: 128D14		
Title		
SPARE ROW FUSE SET ENABLE		
Size A	Document Number SPREN	REV A
Date: November 7, 2001	Sheet 1 of 1	



NOTE: FOR A0,1,2= THE DEFAULTS CHANGE
SO EACH FUSE SET HAS A UNIQUE
DEFAULT ADDRESS DURING TMRDON MODE

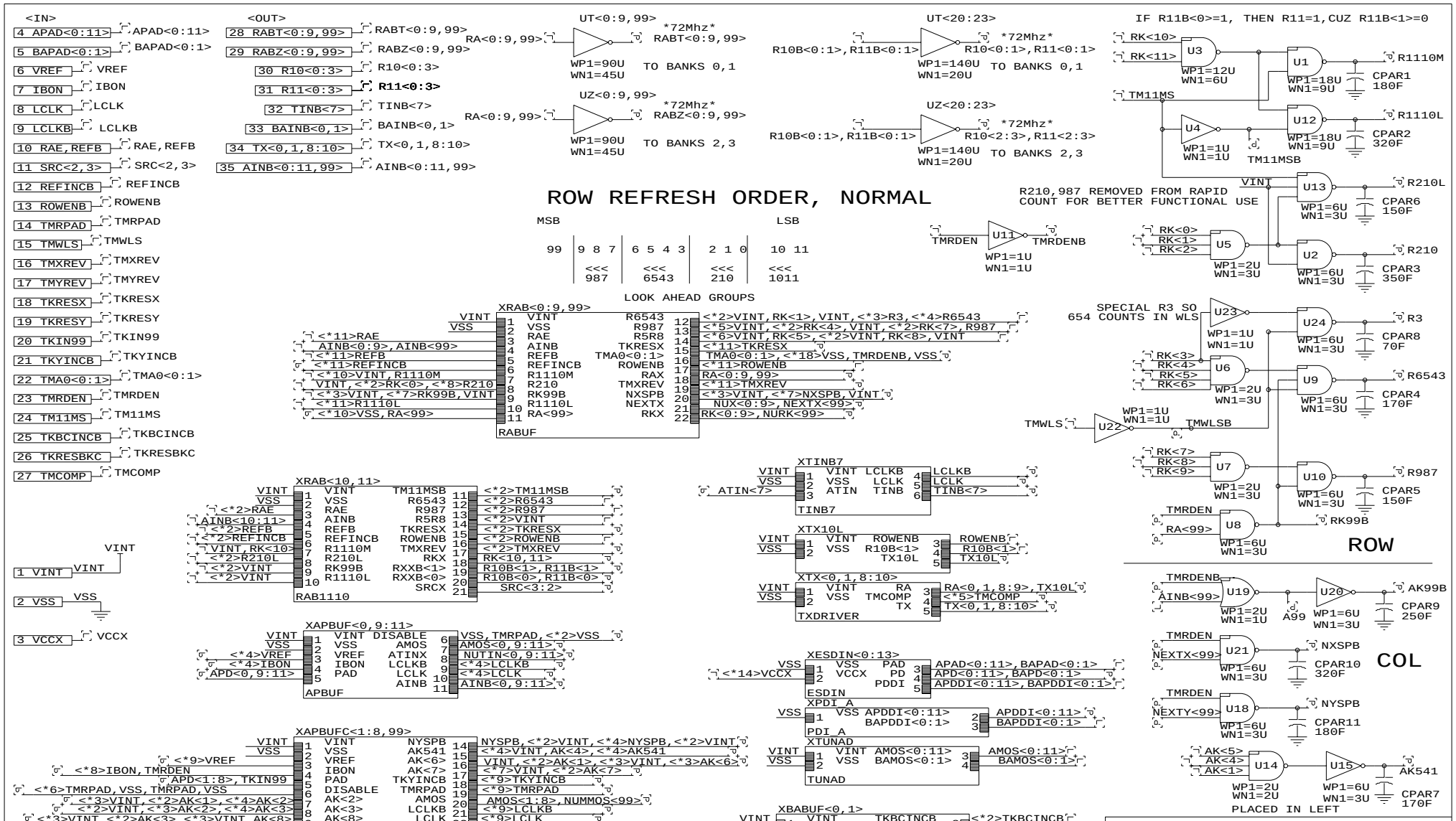
PLACED IN BANK
PLACED IN BNKBOT
PLACED IN ROW1K
PLACED IN SPRBLK
PLACED IN SPRDEC

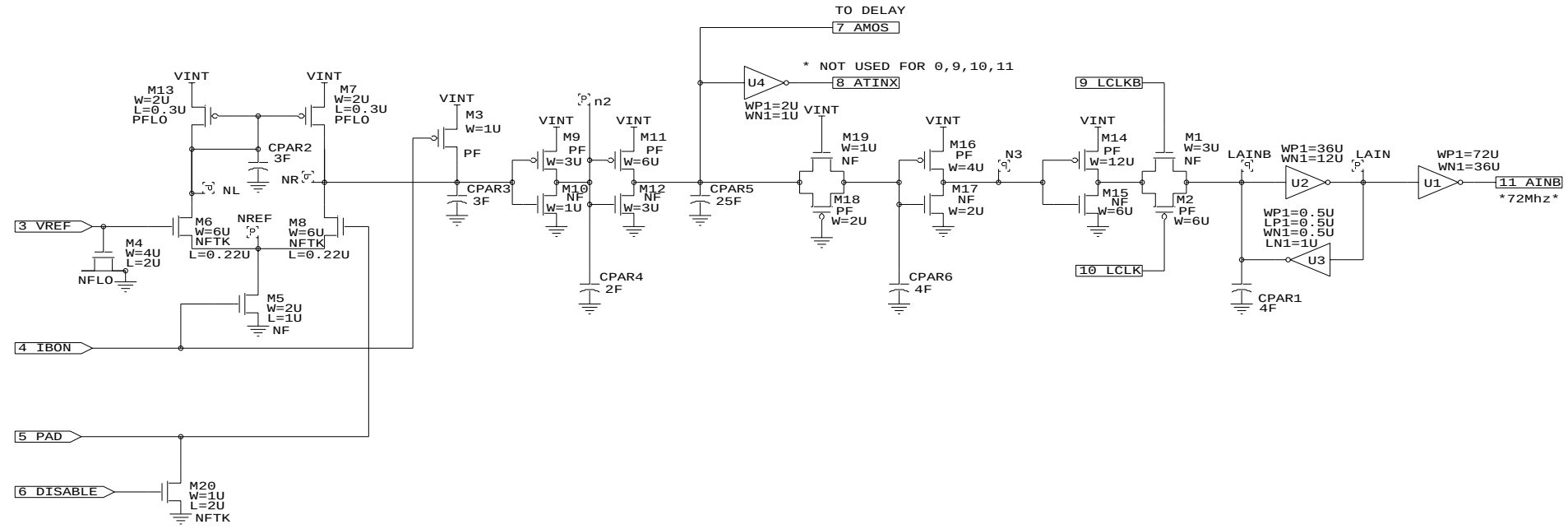


1 ENB SIGNAL PER FUSE SET

8 SETS PER 4M BLOCK

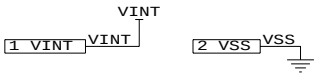
United Memories Inc. Project: 128D14		
Title SPARE ROW ADDRESS SELECT - 1 PER R0-R9		
Size A	Document Number SPRSEL	REV A
Date: September 13, 2001	Sheet 1 of 1	


ROW REFRESH ORDER, NORMAL
MSB
LSB
99 | 9 8 7 | 6 5 4 3 | 2 1 0 | 10 11
<<< 987 | <<< 6543 | <<< 210 | <<< 1011
LOOK AHEAD GROUPS
IF R11B<0>=1, THEN R11=1,CUZ R11B<1>=0
R210,987 REMOVED FROM RAPID COUNT FOR BETTER FUNCTIONAL USE
SPECIAL R3 SO 654 COUNTS IN WLS
ROW
COL
UNITED MEMORIES INC.
PROJECT: 128D14
Title
ROW ADDRESS LOGIC BLOCK
Size B
Document Number RABLK
REV A
Date: November 1, 2001
Sheet 1 of 1
NEVER DISABLE 99 WITH RPAD, BUT ONLY ENABLE (IBON) WITH TMRDEN
*ONLY ATIN<7> IS USED
PLACED IN LEFT



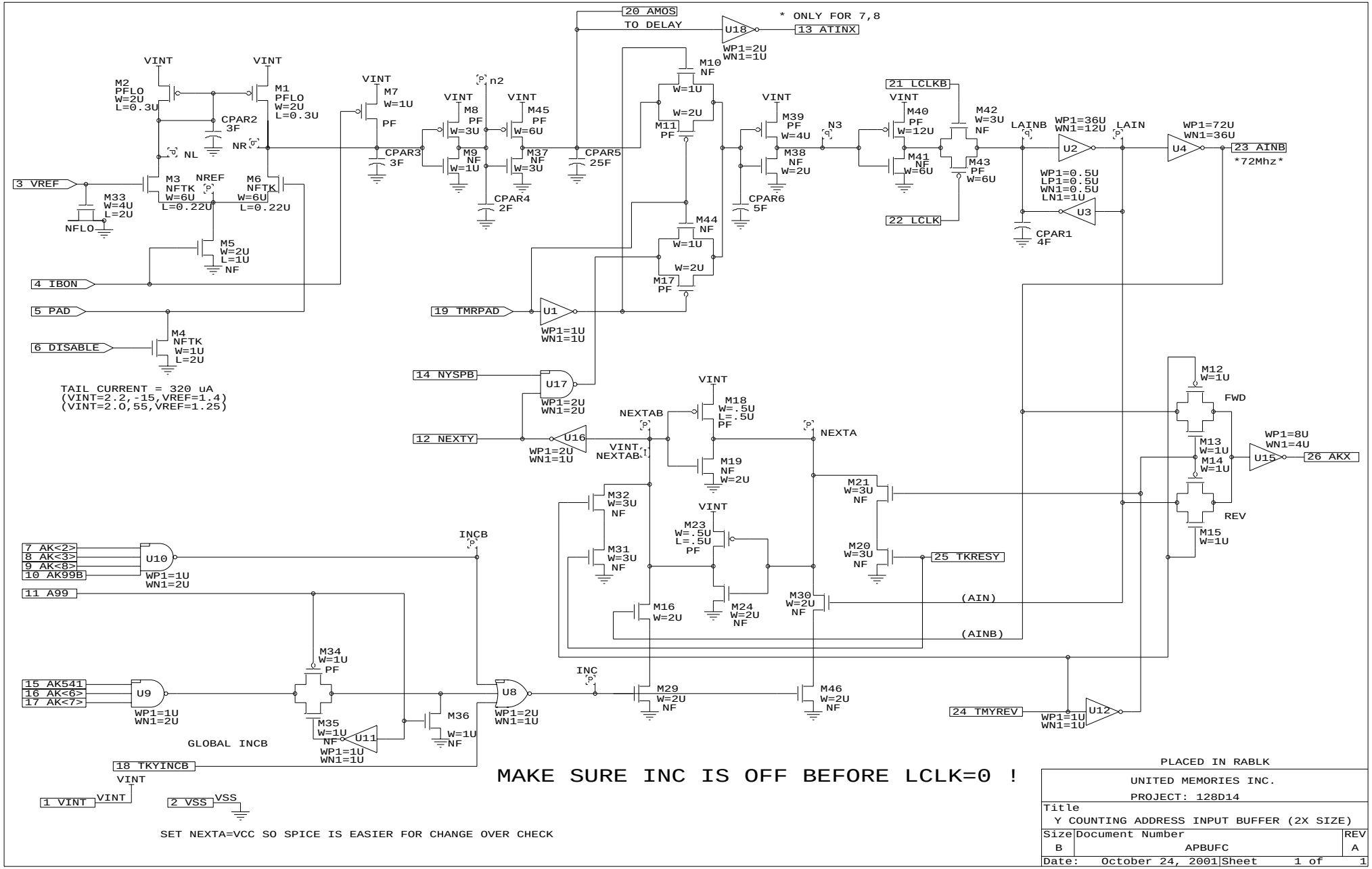
TAIL CURRENT = 320 uA
(VINT=2.2,-15,VREF=1.4)
(VINT=2.0,55,VREF=1.25)

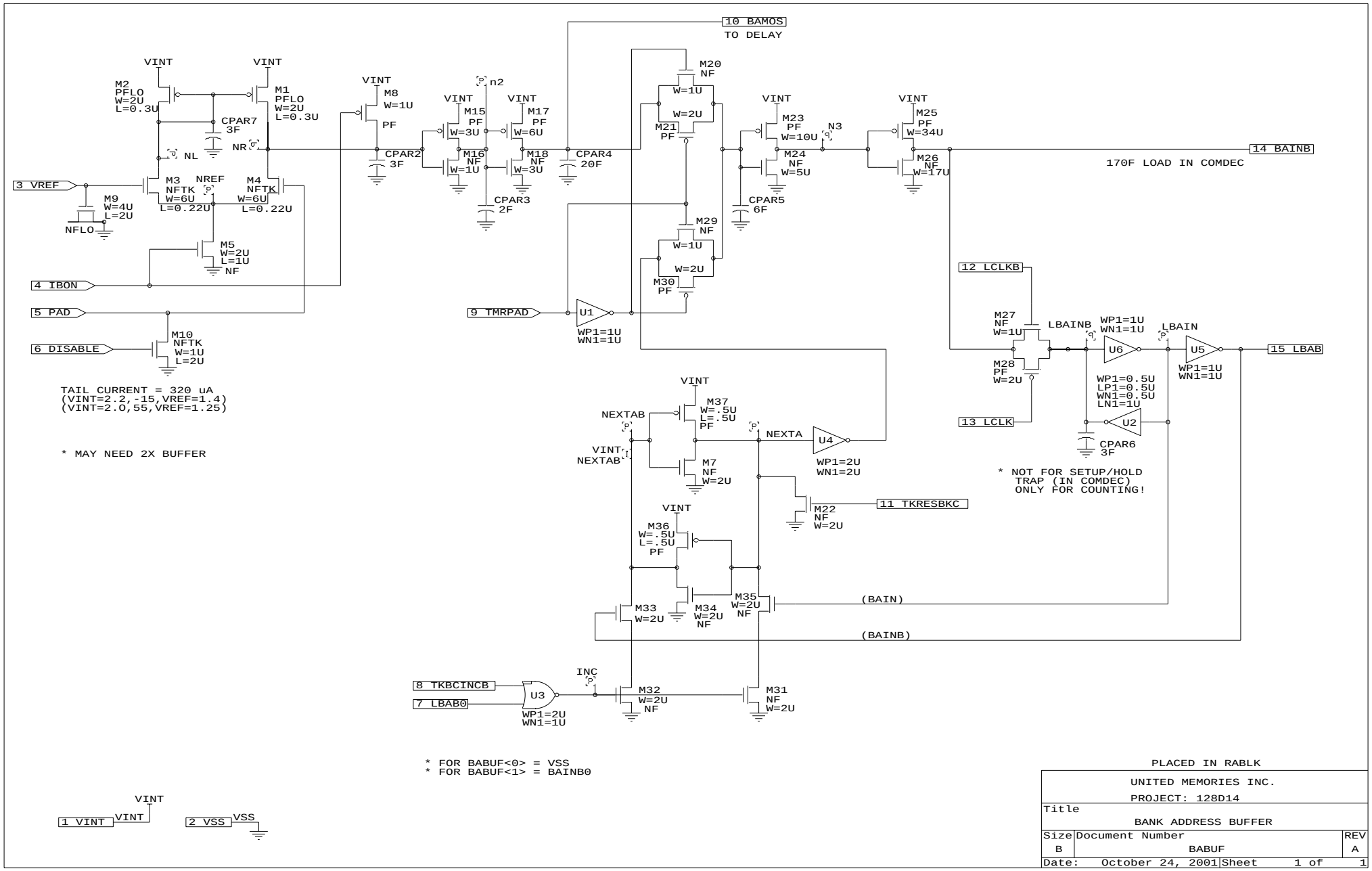
NON-COUNTING 0,9,11,10

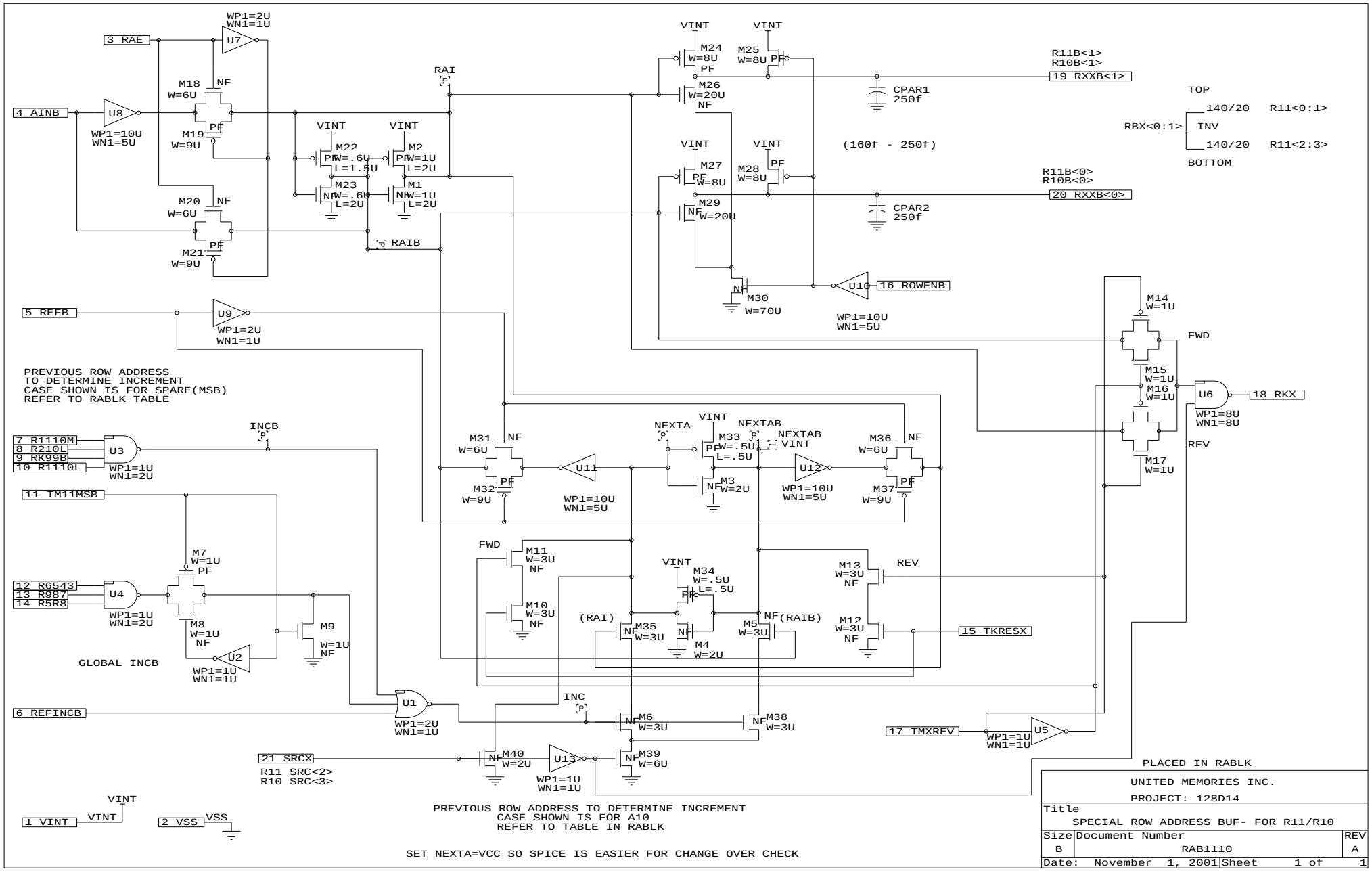


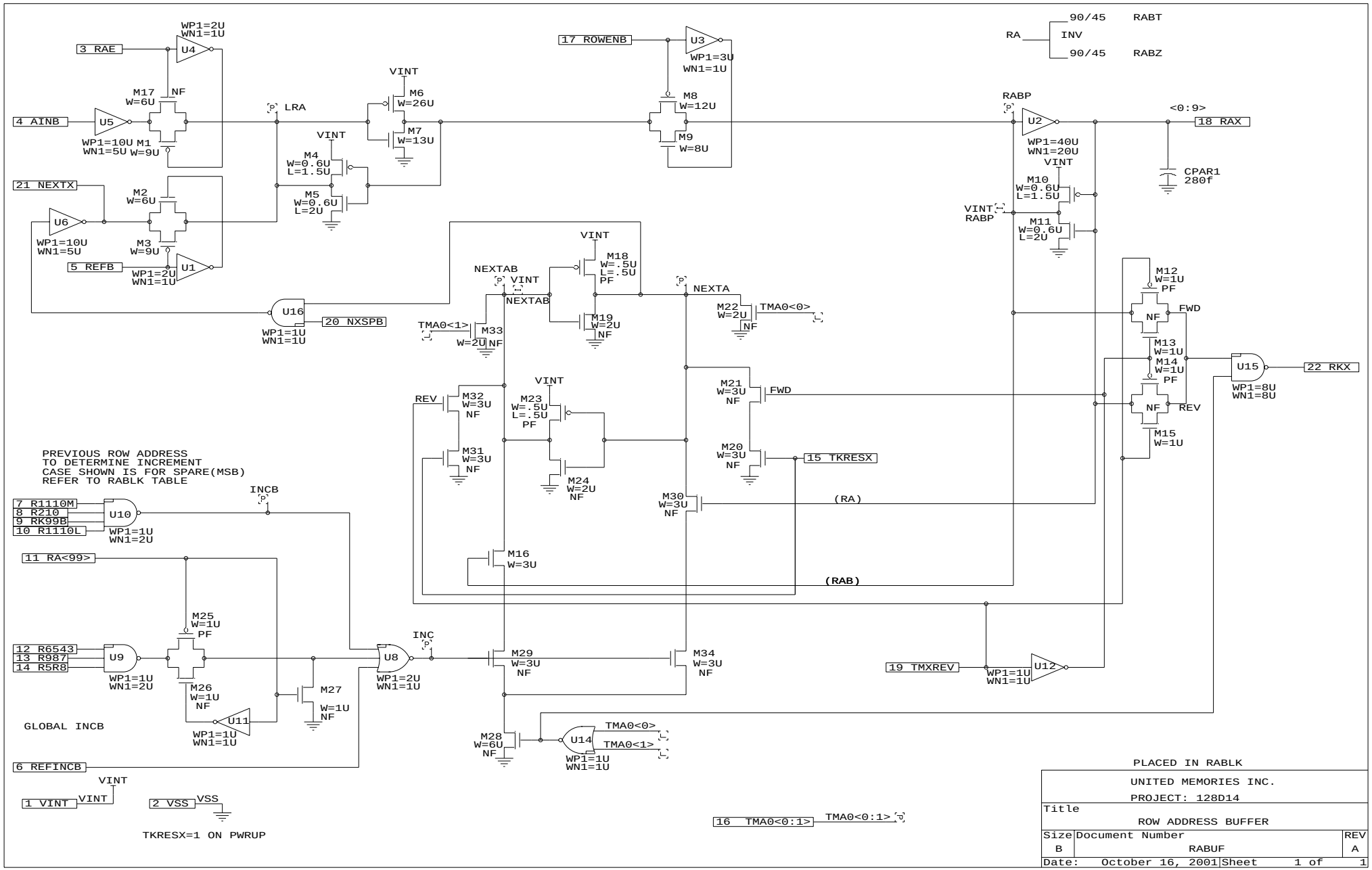
PLACED IN RABLK

UNITED MEMORIES INC.		
PROJECT: 128DDR		
Title ADDRESS INPUT BUFFER (1X SIZE)		
Size B	Document Number APBUF	REV A
Date: October 24, 2001	Sheet 1 of 1	


20 AMOS
TO DELAY
U18
WP1=2U
WN1=1U
* ONLY FOR 7,8
13 ATINX
VINT
M2
PFLO
W=2U
L=0.3U
M1
PFLO
W=2U
L=0.3U
CPAR2
3F
NR
NL
3 VREF
M3
NFTK
W=6U
L=0.22U
NREF
M6
NFTK
W=6U
L=0.22U
M33
W=4U
L=2U
NFLO
M5
W=2U
L=1U
NF
4 IBON
5 PAD
6 DISABLE
M4
NFTK
W=1U
L=2U
TAIL CURRENT = 320 uA
(VINT=2.2,-15,VREF=1.4)
(VINT=2.0,55,VREF=1.25)
M7
W=1U
PF
CPAR3
3F
n2
M8
PF
W=3U
M9
NF
W=1U
M45
PF
W=6U
M37
NF
W=3U
CPAR4
2F
CPAR5
25F
M10
NF
W=1U
W=2U
M11
PF
M44
NF
W=1U
W=2U
M17
PF
19 TMRPAD
U1
WP1=1U
WN1=1U
M39
PF
W=4U
M38
NF
W=2U
CPAR6
5F
N3
21 LCLKB
M40
PF
W=12U
M41
NF
W=6U
22 LCLK
M42
W=3U
NF
M43
PF
W=6U
LAINB
WP1=36U
WN1=12U
U2
LAIN
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
U3
CPAR1
4F
WP1=72U
WN1=36U
U4
23 AINB
72Mhz
14 NYSPB
U17
WP1=2U
WN1=2U
12 NEXTY
U16
WP1=2U
WN1=1U
NEXTAB
VINT,
NEXTAB
M18
W=.5U
L=.5U
PF
M19
NF
W=2U
NEXTA
M12
W=1U
FWD
M13
W=1U
M14
W=1U
REV
M15
W=1U
WP1=8U
WN1=4U
U15
26 AKX
M32
W=3U
NF
M31
W=3U
NF
M23
W=.5U
L=.5U
PF
M24
W=2U
NF
M16
W=2U
M21
W=3U
NF
M20
W=3U
NF
25 TKRESY
M30
W=2U
NF
(AIN)
(AINB)
7 AK<2>
8 AK<3>
9 AK<8>
10 AK99B
U10
WP1=1U
WN1=2U
INCB
11 A99
15 AK541
16 AK<6>
17 AK<7>
U9
WP1=1U
WN1=2U
M34
W=1U
PF
M35
W=1U
NF
U11
WP1=1U
WN1=1U
M36
W=1U
NF
U8
WP1=2U
WN1=1U
INC
M29
W=2U
NF
M46
W=2U
NF
24 TMYREV
U12
WP1=1U
WN1=1U
GLOBAL INCB
18 TKYINCB
MAKE SURE INC IS OFF BEFORE LCLK=0 !
1 VINT
2 VSS
VSS
SET NEXTA=VCC SO SPICE IS EASIER FOR CHANGE OVER CHECK
PLACED IN RABLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
Y COUNTING ADDRESS INPUT BUFFER (2X SIZE)
Size
B
Document Number
APBUFC
REV
A
Date: October 24, 2001
Sheet 1 of 1


10 BAMOS
TO DELAY
VINT
M2
PFLO
W=2U
L=0.3U
M1
PFLO
W=2U
L=0.3U
CPAR7
3F
NL
NR
3 VREF
M3
NFTK
W=6U
L=0.22U
NREF
M4
NFTK
W=6U
L=0.22U
M9
W=4U
L=2U
NFLO
M5
W=2U
L=1U
NF
4 IBON
5 PAD
6 DISABLE
M10
NFTK
W=1U
L=2U
TAIL CURRENT = 320 uA
(VINT=2.2,-15,VREF=1.4)
(VINT=2.0,55,VREF=1.25)
* MAY NEED 2X BUFFER
M8
W=1U
PF
CPAR2
3F
n2
M15
PF
W=3U
M16
NF
W=1U
M17
PF
W=6U
M18
NF
W=3U
CPAR3
2F
CPAR4
20F
M20
NF
W=1U
W=2U
M21
PF
M29
NF
W=1U
W=2U
M30
PF
9 TMRPAD
U1
WP1=1U
WN1=1U
M23
PF
W=10U
N3
M24
NF
W=5U
CPAR5
6F
M25
PF
W=34U
M26
NF
W=17U
14 BAINB
170F LOAD IN COMDEC
12 LCLKB
M27
NF
W=1U
M28
PF
W=2U
LBAINB
WP1=1U
WN1=1U
U6
LBAIN
U5
WP1=1U
WN1=1U
15 LBAB
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
U2
CPAR6
3F
13 LCLK
* NOT FOR SETUP/HOLD
TRAP (IN COMDEC)
ONLY FOR COUNTING!
NEXTAB
M37
W=.5U
L=.5U
PF
NEXTA
U4
WP1=2U
WN1=2U
M7
NF
W=2U
11 TKRESBKC
M22
NF
W=2U
M36
W=.5U
L=.5U
PF
M33
W=2U
M34
W=2U
NF
M35
W=2U
NF
(BAIN)
(BAINB)
INC
8 TKBCINCB
7 LBAB0
U3
WP1=2U
WN1=1U
M32
W=2U
NF
M31
NF
W=2U
* FOR BABUF<0> = VSS
* FOR BABUF<1> = BAINB0
1 VINT
2 VSS
VSS
PLACED IN RABLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
BANK ADDRESS BUFFER
Size B
Document Number
BABUF
REV A
Date: October 24, 2001
Sheet 1 of 1


3 RAE
4 AINB
5 REFB
6 REFINCB
7 R1110M
8 R210L
9 RK99B
10 R1110L
11 TM11MSB
12 R6543
13 R987
14 R5R8
15 TKRESX
16 ROWENB
17 TMXREV
18 RKX
19 RXXB<1>
20 RXXB<0>
21 SRCX
R11 SRC<2>
R10 SRC<3>
1 VINT
2 VSS
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
WP1=2U
WN1=1U
WP1=10U
WN1=5U
WP1=1U
WN1=2U
WP1=8U
WN1=8U
RAI
RAIB
INCB
INC
(RAI)
(RAIB)
FWD
REV
NEXTA
NEXTAB
VINT
VSS
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
M28
M29
M30
M31
M32
M33
M34
M35
M36
M37
M38
M39
M40
CPAR1
250f
CPAR2
250f
(160f - 250f)
R11B<1>
R10B<1>
R11B<0>
R10B<0>
TOP
140/20
R11<0:1>
RBX<0:1>
INV
140/20
R11<2:3>
BOTTOM
PREVIOUS ROW ADDRESS
TO DETERMINE INCREMENT
CASE SHOWN IS FOR SPARE(MSB)
REFER TO RABLK TABLE
GLOBAL INCB
PREVIOUS ROW ADDRESS TO DETERMINE INCREMENT
CASE SHOWN IS FOR A10
REFER TO TABLE IN RABLK
SET NEXTA=VCC SO SPICE IS EASIER FOR CHANGE OVER CHECK
PLACED IN RABLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
SPECIAL ROW ADDRESS BUF- FOR R11/R10
Size B
Document Number
RAB1110
REV A
Date: November 1, 2001
Sheet 1 of 1

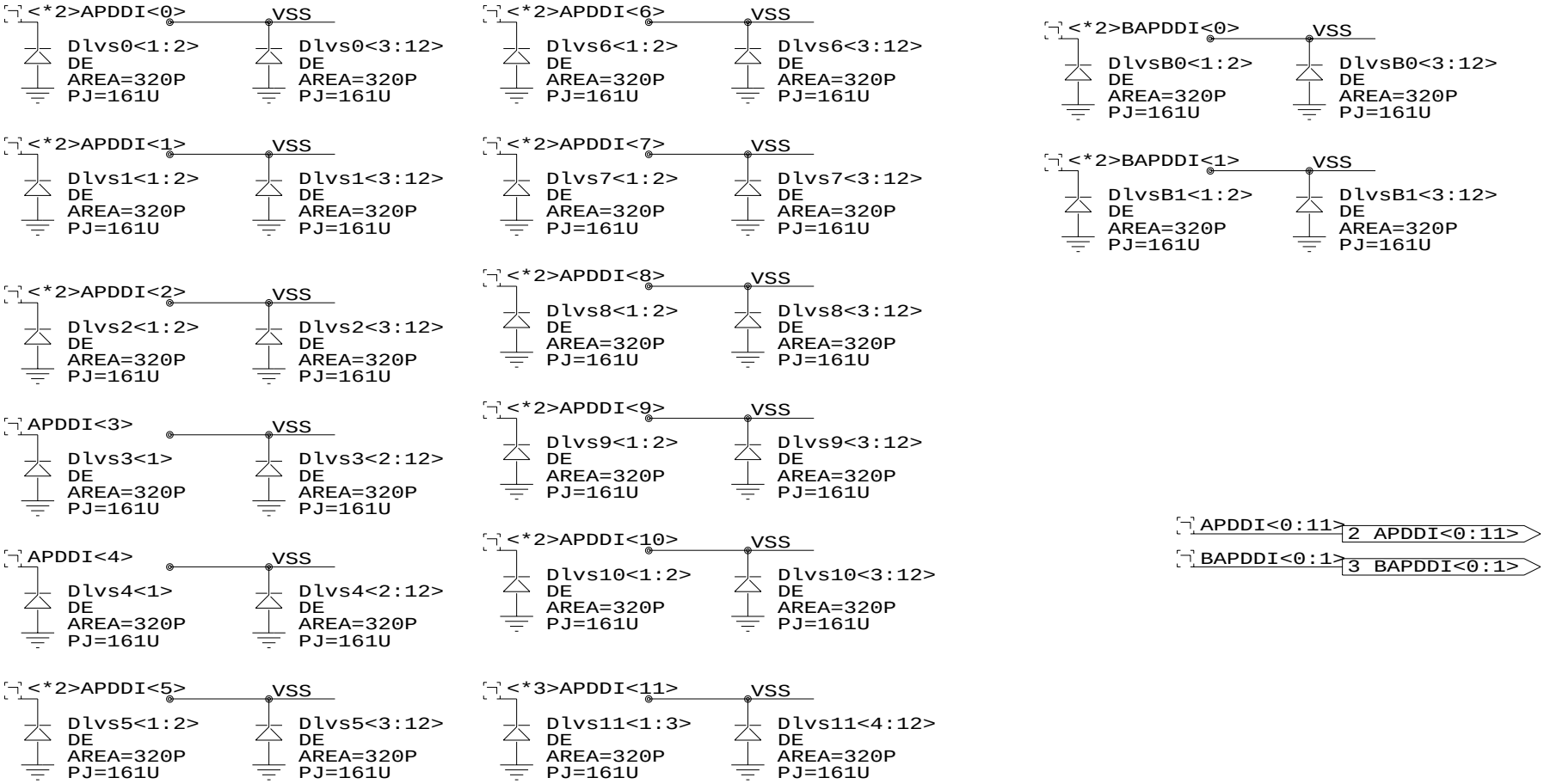


PLACED IN RABLK

UNITED MEMORIES INC.

PROJECT: 128D14

Title		
	ROW ADDRESS BUFFER	
Size B	Document Number RABUF	REV A
Date: October 16, 2001	Sheet 1 of 1	



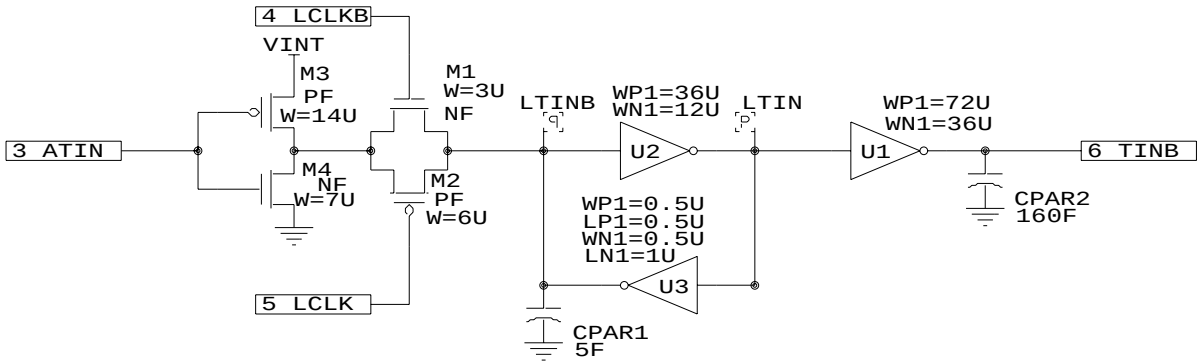
12 WELL DIODES UNDER THE PADS

THESE DIODES ARE TO ADD PAD CAPACITANCE

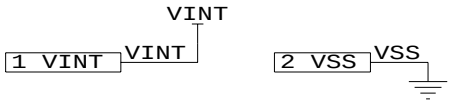
1 VSS VSS

PLACED IN RABLK

United Memories Inc. PROJECT: 128D14		
Title PAD DIODES FOR DM PINS		
Size A	Document Number PDI_A	REV A
Date: October 3, 2001	Sheet 1 of 1	

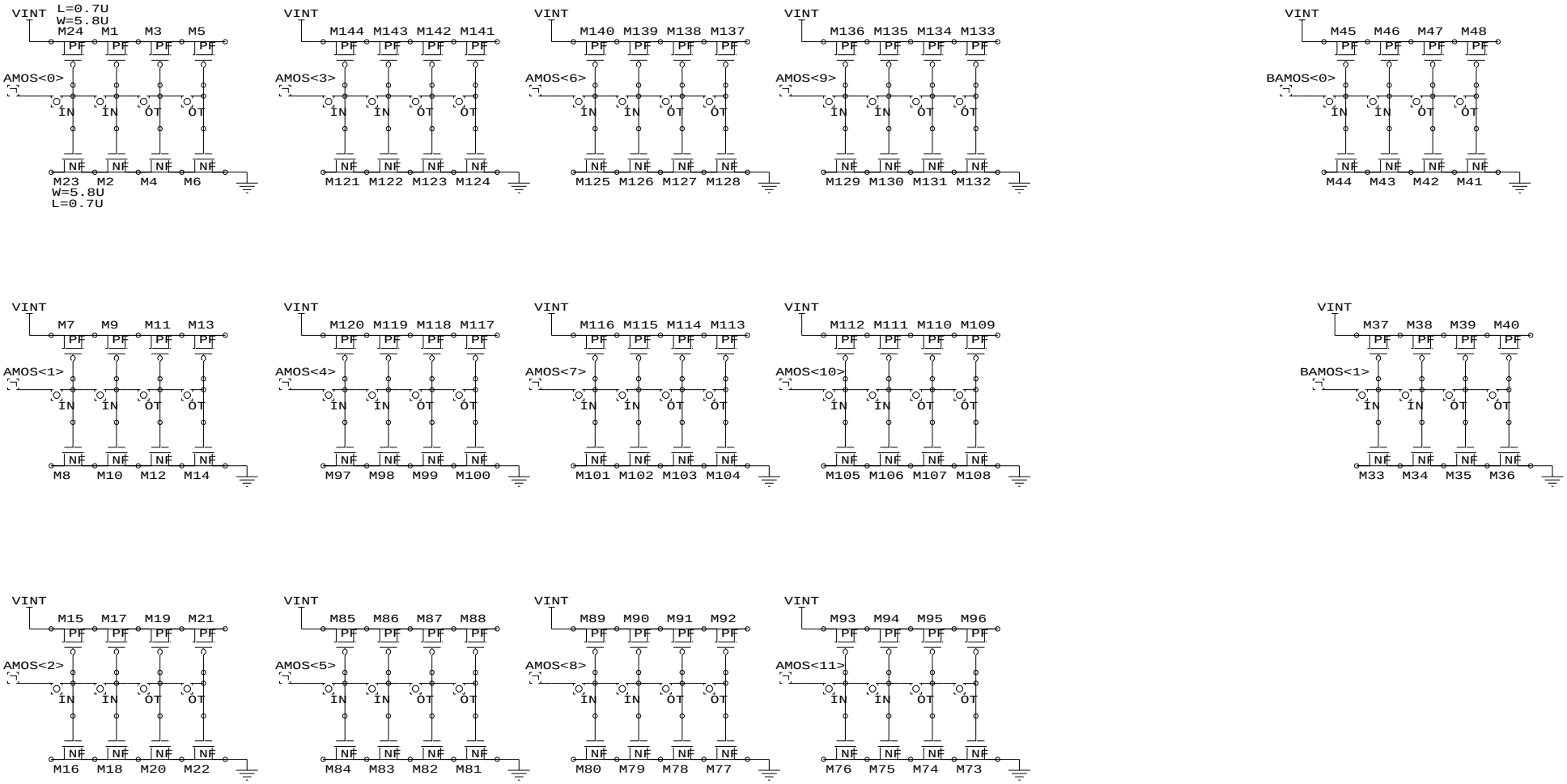


A7 - HAS COUNTING BUFFER
BUT INPUT ALSO WIRED
FOR TEST EVALUATION



PLACED IN RABLK

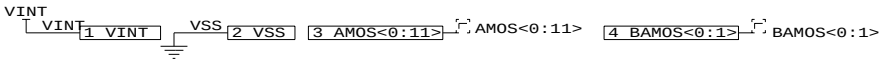
UNITED MEMORIES INC. PROJECT:128D14		
Title TINB DRIVER/LATCH FOR A7		
Size A	Document Number TINB7	REV A
Date: October 16, 2001	Sheet 1 of 1	



ABOUT 100-200 PS/CAP

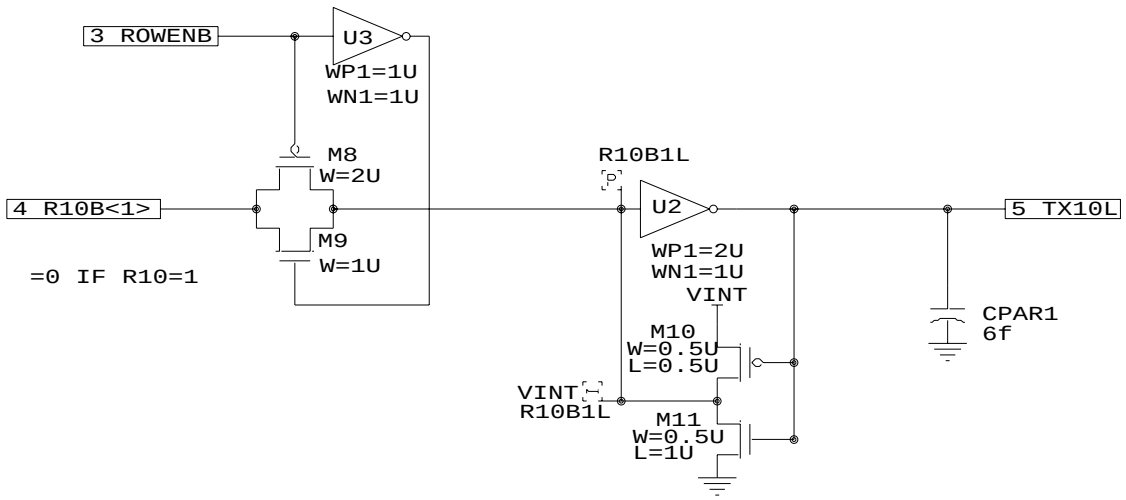
P-CHAN W=5.8U L=0.7U

N-CHAN W=5.8U L=0.7U

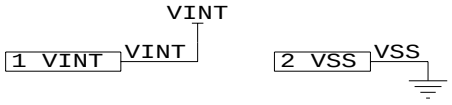


PLACED IN RABLK

United Memories, Inc.		
PROJECT: 128DDR		
Title TUNING CIRCUIT FOR 13 ADDRESS INPUTS		
Size B	Document Number TUNAD	REV A
Date: October 24, 2001	Sheet 1 of 1	



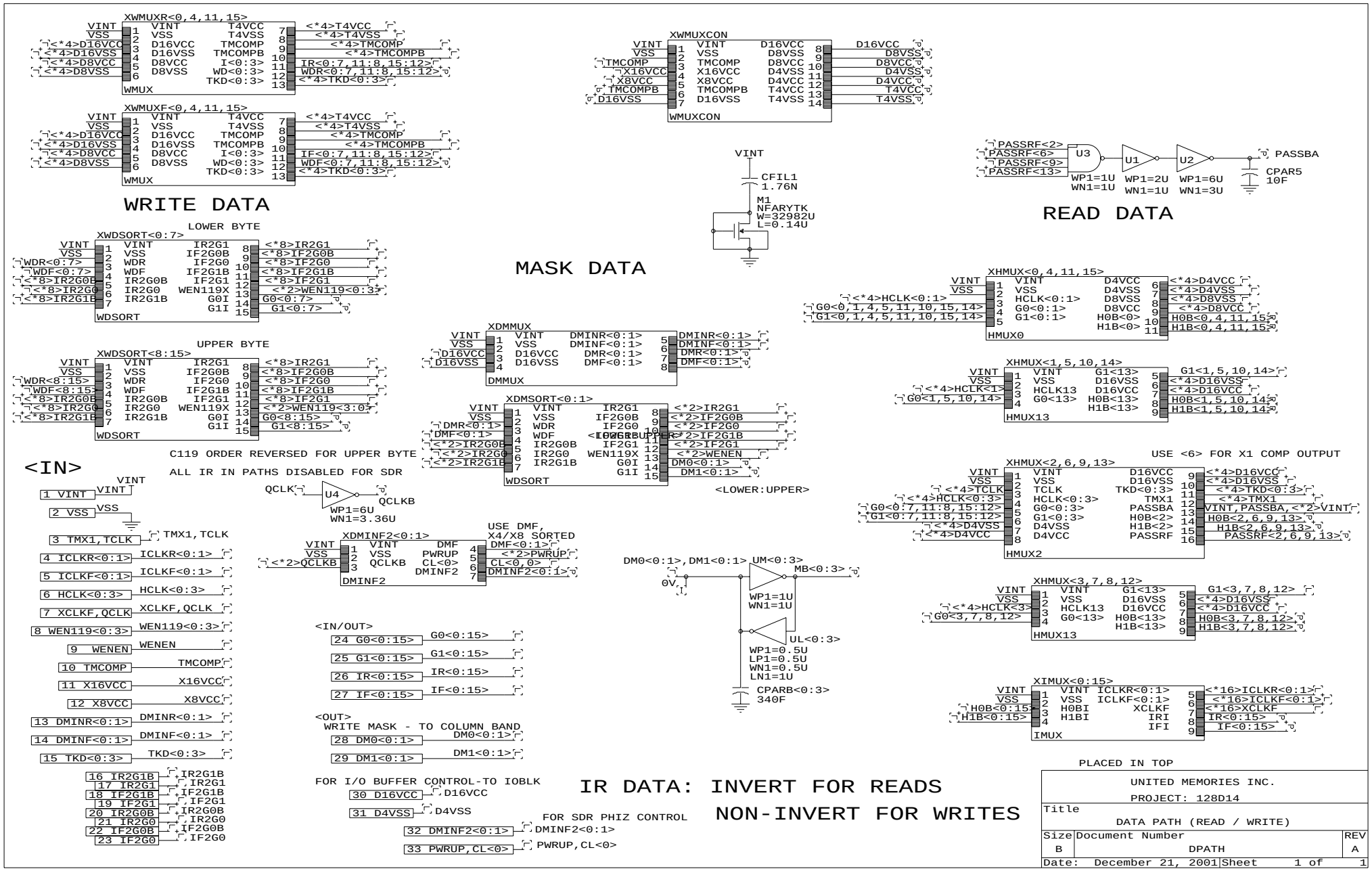
PLACED IN RABLK

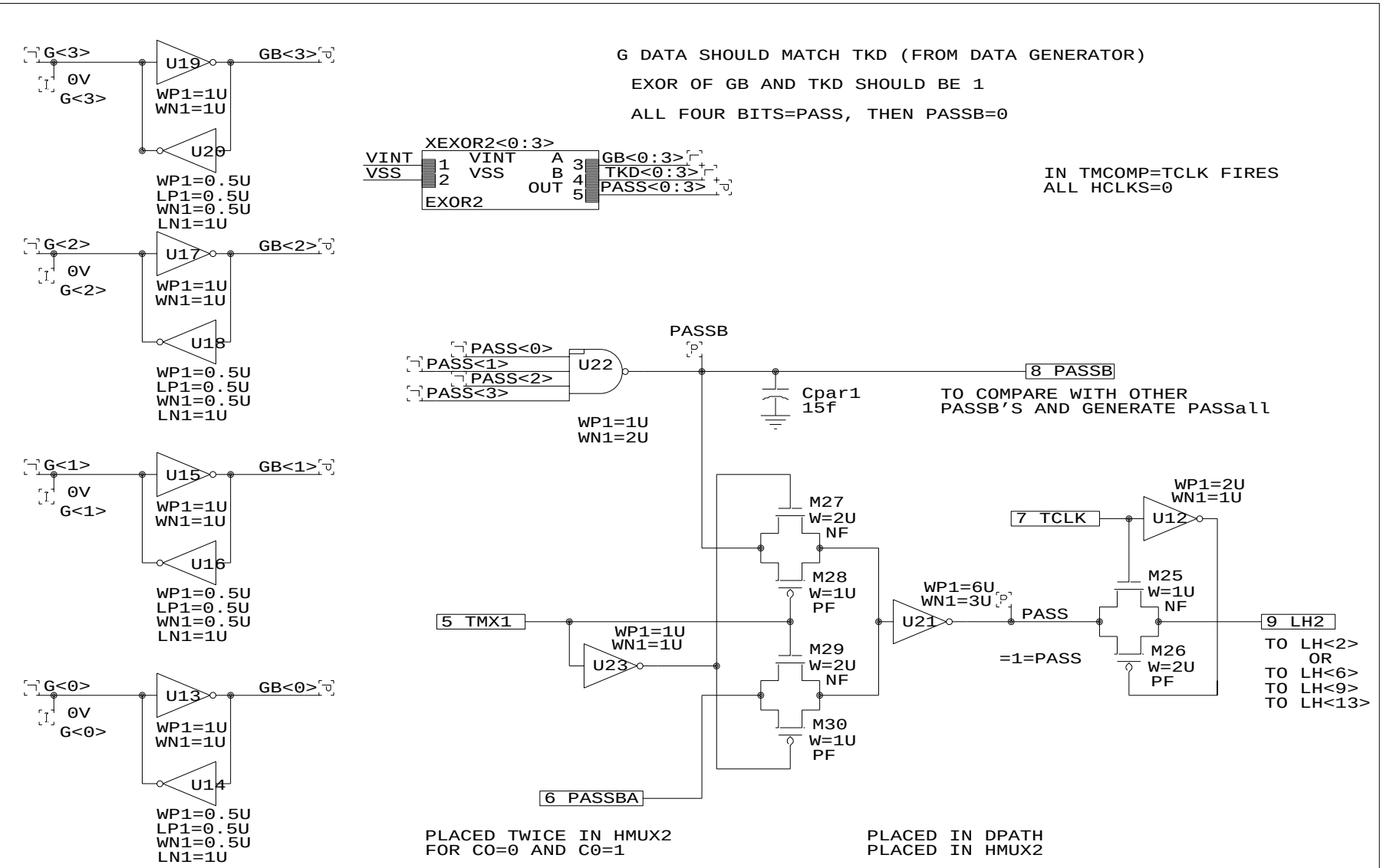


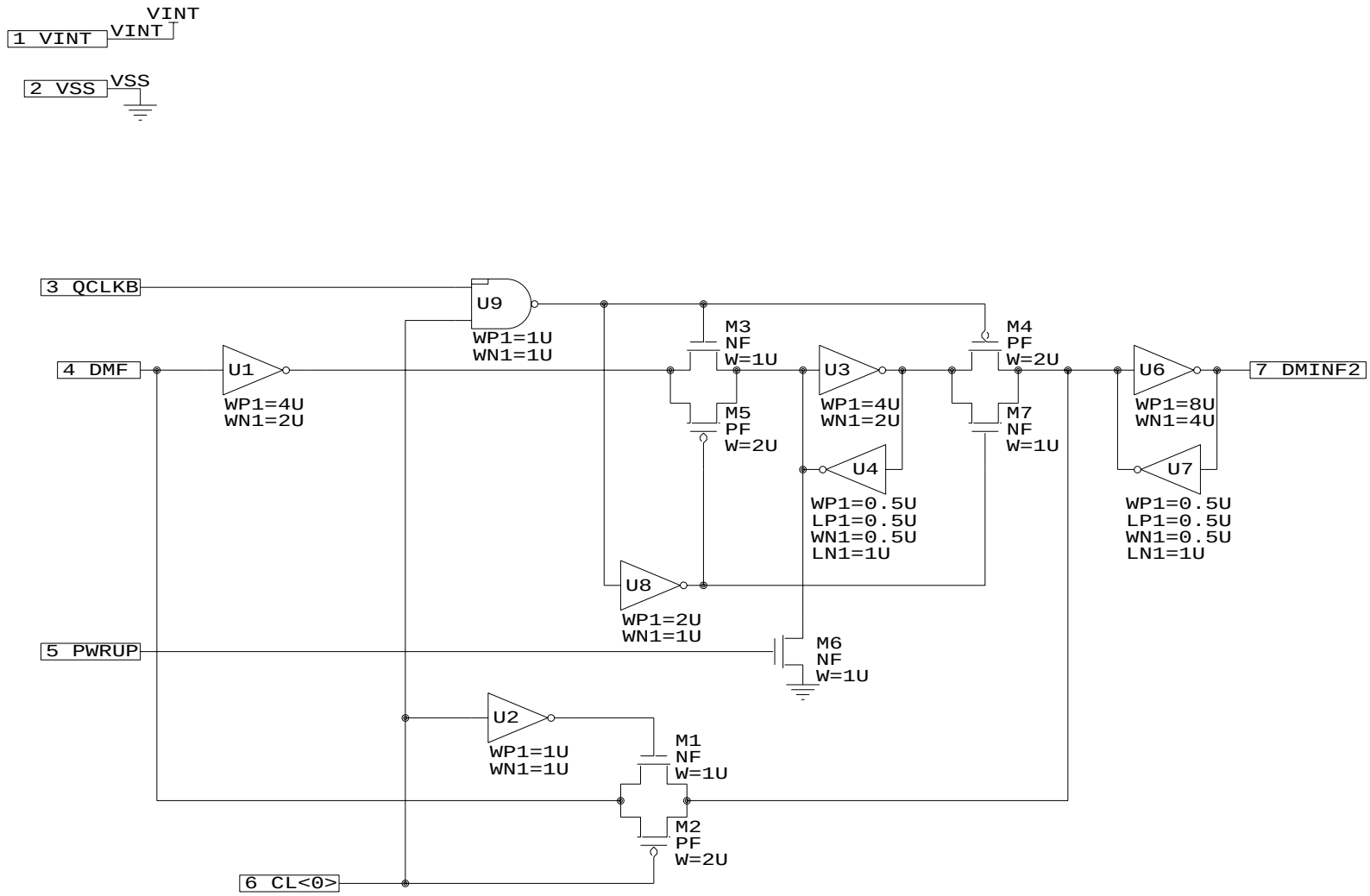
UNITED MEMORIES INC. PROJECT: 128D14		
Title TX10 LATCH		
Size A	Document Number TX10L	REV A
Date: October 16, 2001	Sheet 1 of 1	

PLACED IN RABLK

UNITED MEMORIES INC. PROJECT: 128D14		
Title PROVIDE ROW ADDRESS TO TDATA GENERATOR		
Size A	Document Number TXDRIVER	REV A
Date: October 12, 2001	Sheet 1 of 1	

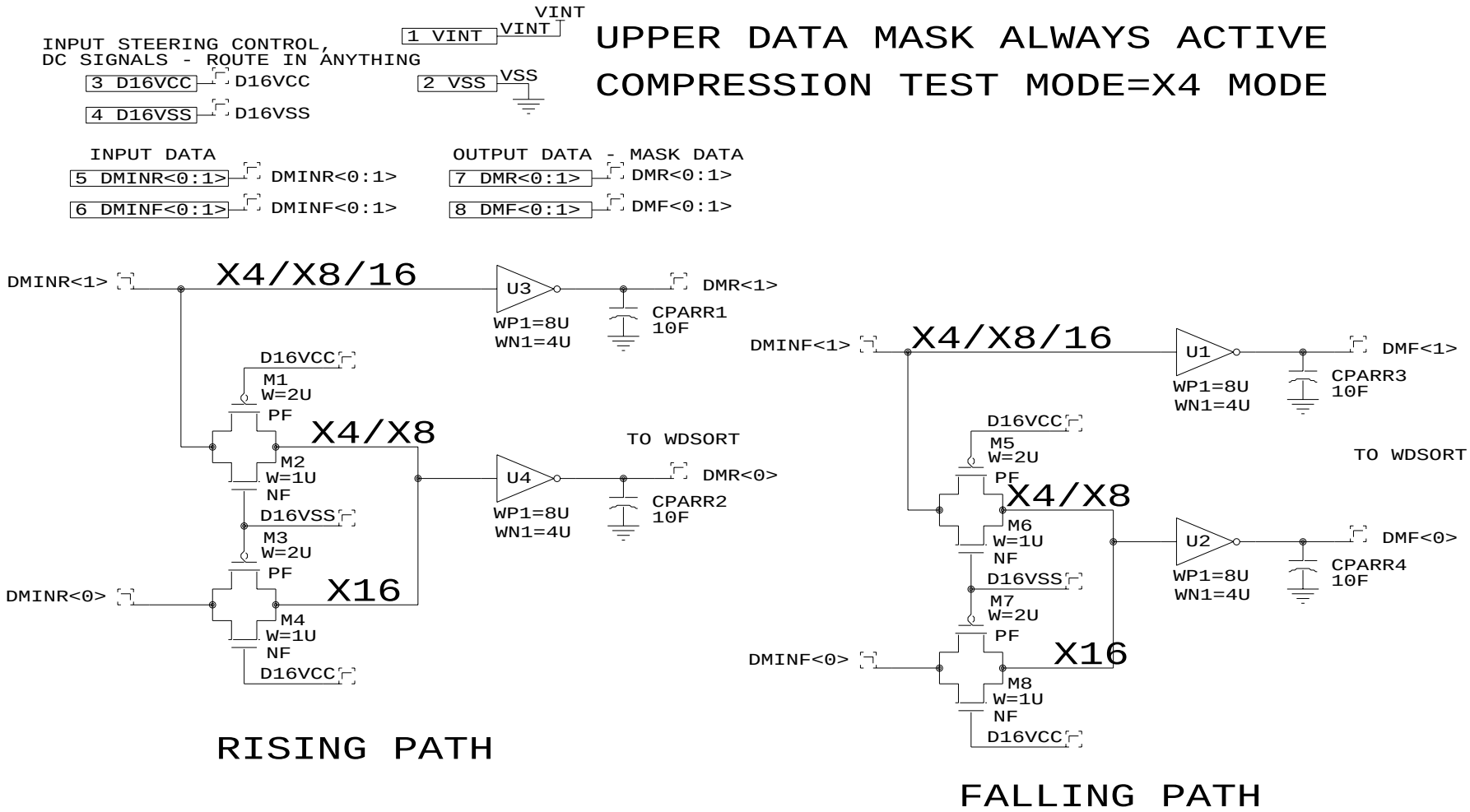

XWMUXR<0,4,11,15>
WMUX
XWMUXF<0,4,11,15>
WMUX
WRITE DATA
XWMUXCON
WMUXCON
VINT
CFIL1
1.76N
M1
NFARYTK
W=32982U
L=0.14U
MASK DATA
PASSRF<2>
PASSRF<6>
PASSRF<9>
PASSRF<13>
U3
U1
U2
WP1=1U
WN1=1U
WP1=2U
WN1=1U
WP1=6U
WN1=3U
PASSBA
CPAR5
10F
READ DATA
LOWER BYTE
XWDSORT<0:7>
WDSORT
UPPER BYTE
XWDSORT<8:15>
WDSORT
XDMMUX
DMMUX
XDMSORT<0:1>
WDSORT
XHMUX<0,4,11,15>
HMUX0
XHMUX<1,5,10,14>
HMUX13
C119 ORDER REVERSED FOR UPPER BYTE
ALL IR IN PATHS DISABLED FOR SDR
<IN>
QCLK
U4
QCLKB
WP1=6U
WN1=3.36U
XDMINF2<0:1>
DMINF2
USE DMF,
X4/X8 SORTED
<LOWER:UPPER>
USE <6> FOR X1 COMP OUTPUT
XHMUX<2,6,9,13>
HMUX2
DM0<0:1>,DM1<0:1>
UM<0:3>
MB<0:3>
0V
WP1=1U
WN1=1U
UL<0:3>
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
CPARB<0:3>
340F
XHMUX<3,7,8,12>
HMUX13
XIMUX<0:15>
IMUX
<IN/OUT>
<OUT>
WRITE MASK - TO COLUMN BAND
FOR I/O BUFFER CONTROL-TO IOBLK
FOR SDR PHIZ CONTROL
IR DATA: INVERT FOR READS
NON-INVERT FOR WRITES
PLACED IN TOP
UNITED MEMORIES INC.
PROJECT: 128D14
Title
DATA PATH (READ / WRITE)
Size B
Document Number
DPATH
REV A
Date: December 21, 2001
Sheet 1 of 1


G<3>
0V
G<3>
U19
GB<3>
WP1=1U
WN1=1U
U20
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
G<2>
0V
G<2>
U17
GB<2>
WP1=1U
WN1=1U
U18
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
G<1>
0V
G<1>
U15
GB<1>
WP1=1U
WN1=1U
U16
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
G<0>
0V
G<0>
U13
GB<0>
WP1=1U
WN1=1U
U14
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
G DATA SHOULD MATCH TKD (FROM DATA GENERATOR)
EXOR OF GB AND TKD SHOULD BE 1
ALL FOUR BITS=PASS, THEN PASSB=0
XEXOR2<0:3>
VINT
VSS
1
2
VINT
VSS
A
B
OUT
3
4
5
GB<0:3>
TKD<0:3>
PASS<0:3>
EXOR2
IN TMCOMP=TCLK FIRES
ALL HCLKS=0
PASS<0>
PASS<1>
PASS<2>
PASS<3>
U22
PASSB
8 PASSB
Cpar1
15f
TO COMPARE WITH OTHER
PASSB'S AND GENERATE PASSall
WP1=1U
WN1=2U
M27
W=2U
NF
M28
W=1U
PF
M29
W=2U
NF
M30
W=1U
PF
5 TMX1
WP1=1U
WN1=1U
U23
6 PASSBA
WP1=6U
WN1=3U
U21
PASS
=1=PASS
7 TCLK
WP1=2U
WN1=1U
U12
M25
W=1U
NF
M26
W=2U
PF
9 LH2
TO LH<2>
OR
TO LH<6>
TO LH<9>
TO LH<13>
PLACED TWICE IN HMUX2
FOR CO=0 AND C0=1
PLACED IN DPATH
PLACED IN HMUX2
G-LINE LATCHES PLACED HERE
1 VINT
2 VSS
VINT
VINT
VSS
3 G<0:3>
4 TKD<0:3>
G<0:3>
TKD<0:3>
United Memories Inc.
Project: 128D14
Title
Compression Test Mode Data Generator
Size
A
Document Number
CTMDAT
REV
A
Date: October 16, 2001
Sheet 1 of 1



PLACED DPATH

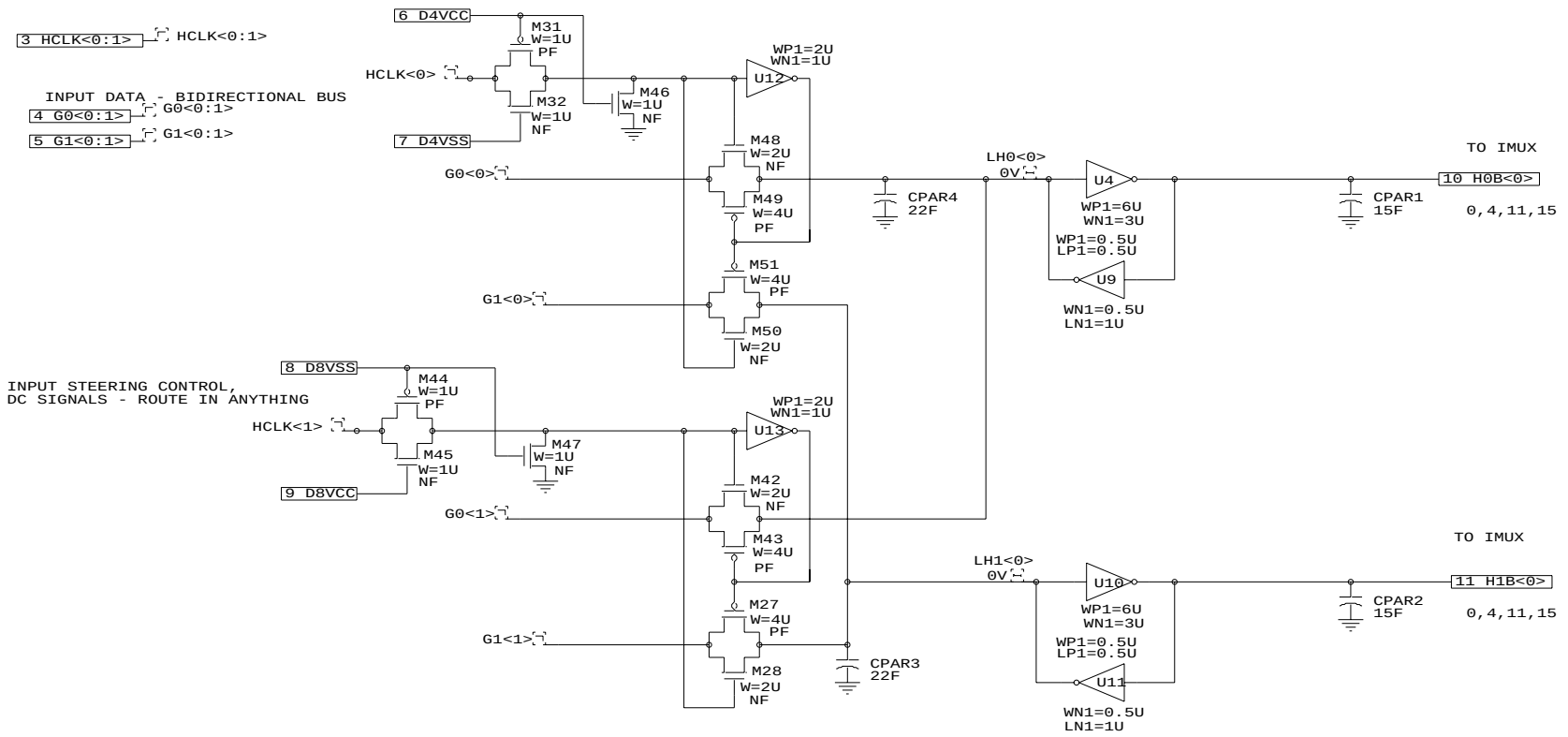
UNITED MEMORIES INC. PROJECT:128D14		
Title DATA MASK INVERTER/BUFFER (FOR CL<0> ONLY)		
Size A	Document Number DMINF2	REV A
Date: November 7, 2001	Sheet 1 of 1	



PLACED DPATH

UNITED MEMORIES INC. PROJECT:128D14		
Title DATA MASK MUX POINT (X4/X8 VS. X16)		
Size A	Document Number DMMUX	REV A
Date: October 16, 2001	Sheet 1 of 1	

STEERING CLK, BASED ON SHIFTED C119 INFORMATION



	C119	<0>	<1>	<2>	<3>
L-BYTE	IO	<0>	<1>	<2>	<3>
	IO	<4>	<5>	<6>	<7>
U-BYTE	IO	<11>	<10>	<9>	<8>
	IO	<15>	<14>	<13>	<12>
		X8		X8 X4	

FOR X16 / ALL ON PLACED IN DPATH

1 VINT — VINT

2 VSS — VSS

(LH CPARS REFLECT HMUX2 CASE)

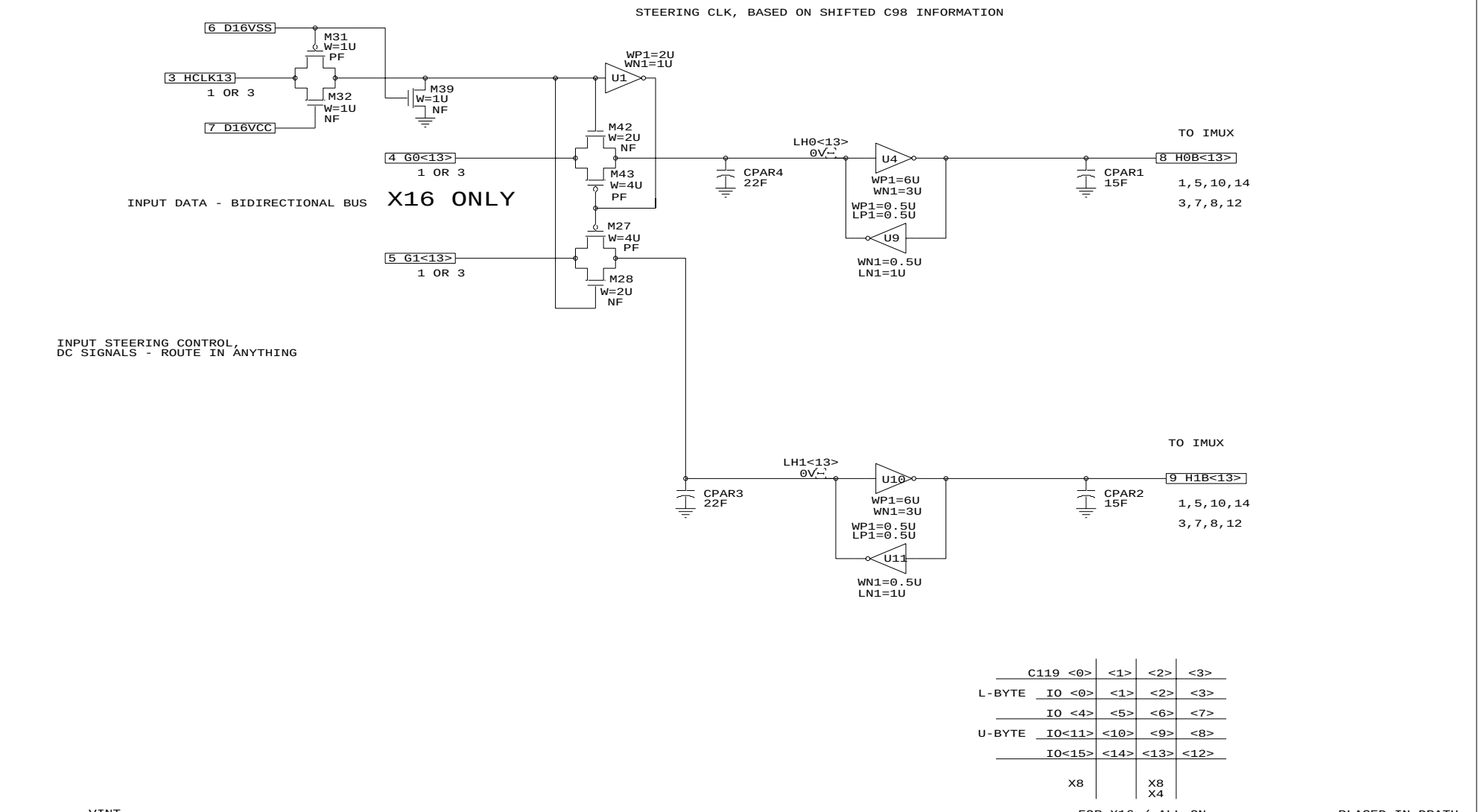
UNITED MEMORIES INC.

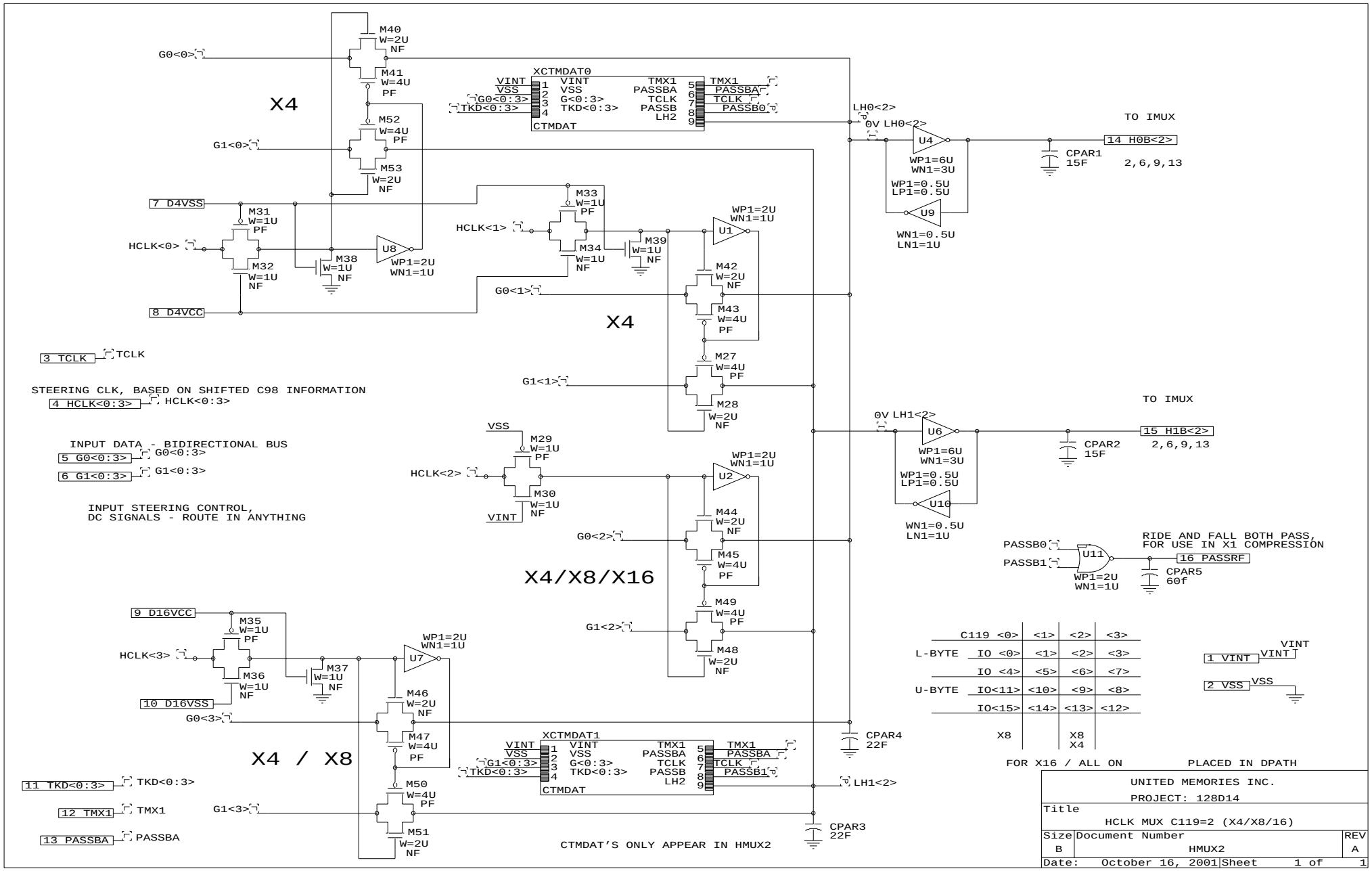
PROJECT: 128D14

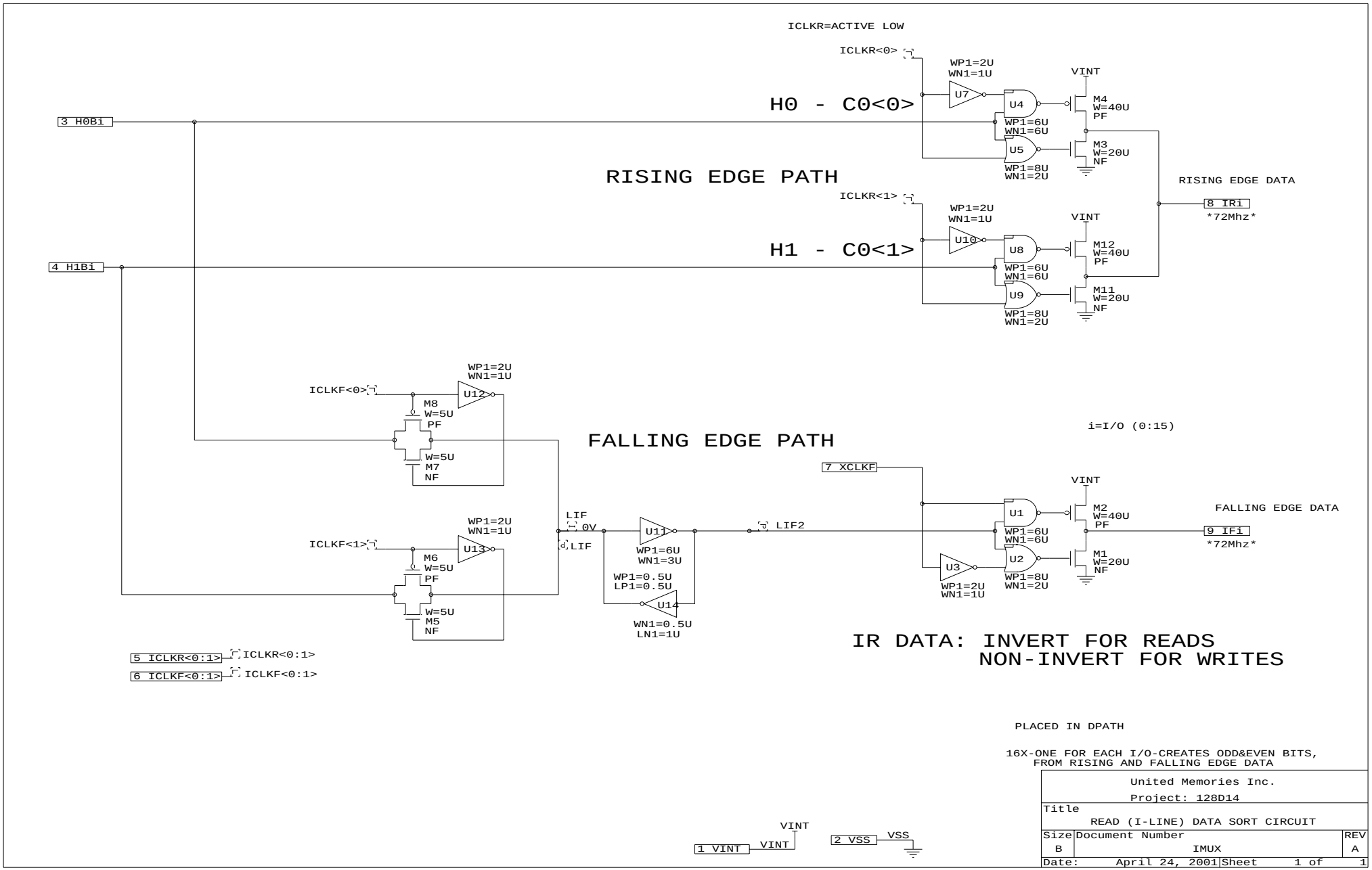
Title: HCLK MUX C119=0 (X4/X8/16)

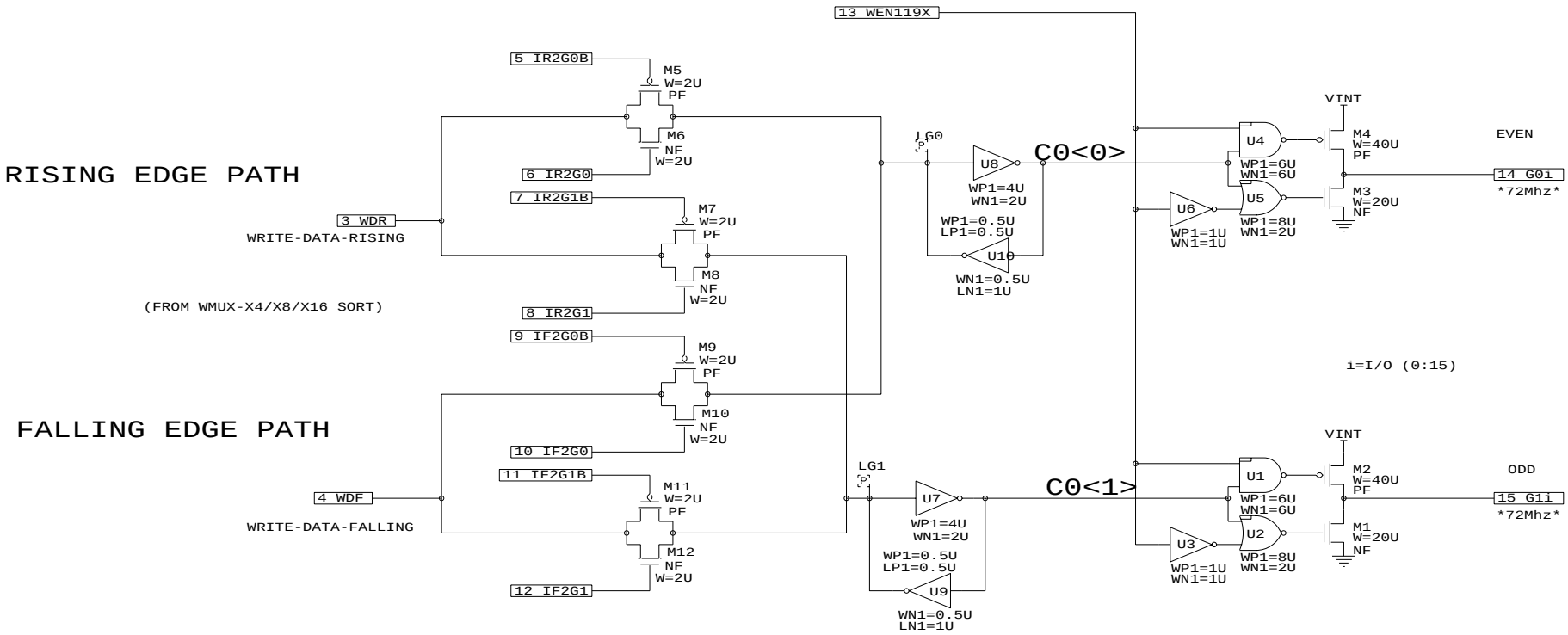
Size	Document Number	REV
B	HMUX0	A

Date: October 16, 2001 | Sheet 1 of 1


STEERING CLK, BASED ON SHIFTED C98 INFORMATION
6 D16VSS
M31
W=1U
PF
3 HCLK13
1 OR 3
M32
W=1U
NF
7 D16VCC
M39
W=1U
NF
WP1=2U
WN1=1U
U1
M42
W=2U
NF
4 G0<13>
1 OR 3
M43
W=4U
PF
INPUT DATA - BIDIRECTIONAL BUS
X16 ONLY
M27
W=4U
PF
5 G1<13>
1 OR 3
M28
W=2U
NF
LH0<13>
0V
CPAR4
22F
U4
WP1=6U
WN1=3U
WP1=0.5U
LP1=0.5U
U9
WN1=0.5U
LN1=1U
TO IMUX
8 H0B<13>
CPAR1
15F
1,5,10,14
3,7,8,12
INPUT STEERING CONTROL,
DC SIGNALS - ROUTE IN ANYTHING
LH1<13>
0V
CPAR3
22F
U10
WP1=6U
WN1=3U
WP1=0.5U
LP1=0.5U
U11
WN1=0.5U
LN1=1U
TO IMUX
9 H1B<13>
CPAR2
15F
1,5,10,14
3,7,8,12
C119 <0> <1> <2> <3>
L-BYTE IO <0> <1> <2> <3>
IO <4> <5> <6> <7>
U-BYTE IO<11> <10> <9> <8>
IO<15> <14> <13> <12>
X8
X8
X4
FOR X16 / ALL ON
PLACED IN DPATH
VINT
1 VINT
VINT
2 VSS
VSS
(LH CPARS REFLECT HMUX2 CASE=WC)
UNITED MEMORIES INC.
PROJECT: 128D14
Title
HCLK MUX C119=1,3 (X4/X8/16)
Size B
Document Number
HMUX13
REV A
Date: October 16, 2001
Sheet 1 of 1


X4
X4
X4/X8/X16
X4 / X8
XCTMDAT0
CTMDAT
XCTMDAT1
CTMDAT
VINT
VSS
G0<0:3>
TKD<0:3>
G<0:3>
TKD<0:3>
TMX1
PASSBA
TCLK
PASSB
LH2
PASSB0
PASSB1
G0<0>
G1<0>
G0<1>
G1<1>
G0<2>
G1<2>
G0<3>
G1<3>
HCLK<0>
HCLK<1>
HCLK<2>
HCLK<3>
7 D4VSS
8 D4VCC
9 D16VCC
10 D16VSS
3 TCLK
TCLK
STEERING CLK, BASED ON SHIFTED C98 INFORMATION
4 HCLK<0:3>
HCLK<0:3>
INPUT DATA - BIDIRECTIONAL BUS
5 G0<0:3>
G0<0:3>
6 G1<0:3>
G1<0:3>
INPUT STEERING CONTROL,
DC SIGNALS - ROUTE IN ANYTHING
11 TKD<0:3>
TKD<0:3>
12 TMX1
TMX1
13 PASSBA
PASSBA
M40 W=2U NF
M41 W=4U PF
M52 W=4U PF
M53 W=2U NF
M31 W=1U PF
M32 W=1U NF
M38 W=1U NF
U8 WP1=2U WN1=1U
M33 W=1U PF
M34 W=1U NF
M39 W=1U NF
U1 WP1=2U WN1=1U
M42 W=2U NF
M43 W=4U PF
M27 W=4U PF
M28 W=2U NF
M29 W=1U PF
M30 W=1U NF
U2 WP1=2U WN1=1U
M44 W=2U NF
M45 W=4U PF
M49 W=4U PF
M48 W=2U NF
M35 W=1U PF
M36 W=1U NF
M37 W=1U NF
U7 WP1=2U WN1=1U
M46 W=2U NF
M47 W=4U PF
M50 W=4U PF
M51 W=2U NF
LH0<2>
0V LH0<2>
U4 WP1=6U WN1=3U
WP1=0.5U LP1=0.5U
U9 WN1=0.5U LN1=1U
TO IMUX
14 H0B<2>
CPAR1 15F
2,6,9,13
0V LH1<2>
U6 WP1=6U WN1=3U
WP1=0.5U LP1=0.5U
U10 WN1=0.5U LN1=1U
TO IMUX
15 H1B<2>
CPAR2 15F
2,6,9,13
PASSB0
PASSB1
U11 WP1=2U WN1=1U
RIDE AND FALL BOTH PASS,
FOR USE IN X1 COMPRESSION
16 PASSRF
CPAR5 60f
CPAR4 22F
CPAR3 22F
LH1<2>
C119 <0> <1> <2> <3>
L-BYTE IO <0> <1> <2> <3>
IO <4> <5> <6> <7>
U-BYTE IO<11> <10> <9> <8>
IO<15> <14> <13> <12>
X8 X8 X4
FOR X16 / ALL ON
PLACED IN DPATH
1 VINT
VINT
2 VSS
VSS
CTMDAT'S ONLY APPEAR IN HMUX2
UNITED MEMORIES INC.
PROJECT: 128D14
Title
HCLK MUX C119=2 (X4/X8/16)
Size B
Document Number
HMUX2
REV A
Date: October 16, 2001
Sheet 1 of 1

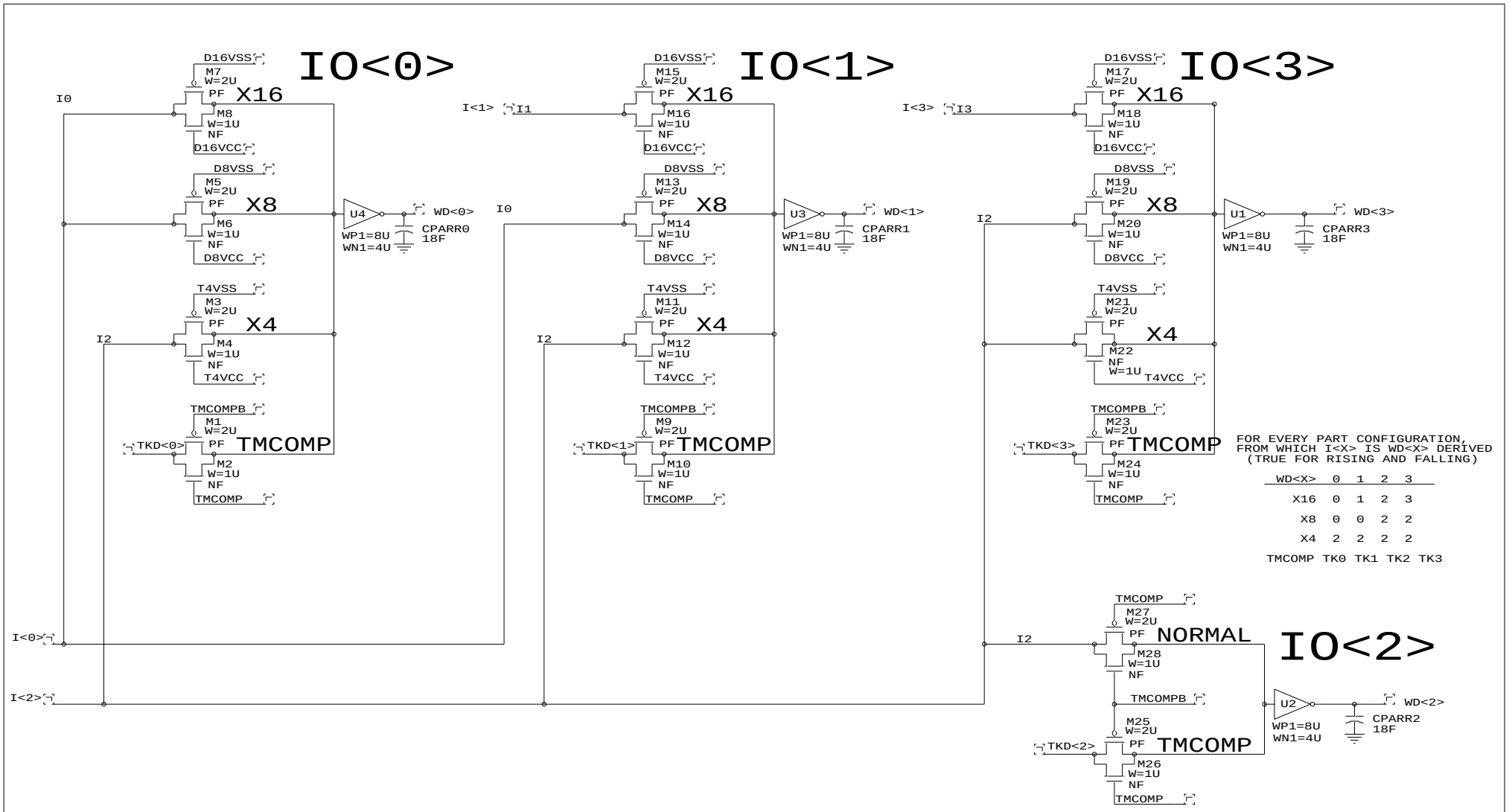

ICLKR=ACTIVE LOW
ICLKR<0>
WP1=2U
WN1=1U
VINT
U7
U4
M4
W=40U
PF
H0 - C0<0>
3 H0Bi
WP1=6U
WN1=6U
U5
M3
W=20U
NF
WP1=8U
WN1=2U
RISING EDGE PATH
RISING EDGE DATA
ICLKR<1>
8 IRi
72Mhz
WP1=2U
WN1=1U
VINT
U10
U8
M12
W=40U
PF
H1 - C0<1>
4 H1Bi
WP1=6U
WN1=6U
U9
M11
W=20U
NF
WP1=8U
WN1=2U
WP1=2U
WN1=1U
ICLKF<0>
U12
M8
W=5U
PF
W=5U
M7
NF
FALLING EDGE PATH
i=I/O (0:15)
7 XCLKF
VINT
U1
M2
W=40U
PF
FALLING EDGE DATA
LIF
0V
LIF2
9 IFi
72Mhz
WP1=2U
WN1=1U
ICLKF<1>
U13
LIF
U11
WP1=6U
WN1=6U
WP1=6U
WN1=3U
M6
W=5U
PF
U2
M1
W=20U
NF
WP1=0.5U
LP1=0.5U
U3
WP1=8U
WN1=2U
WP1=2U
WN1=1U
U14
WN1=0.5U
LN1=1U
W=5U
M5
NF
IR DATA: INVERT FOR READS
NON-INVERT FOR WRITES
5 ICLKR<0:1>
ICLKR<0:1>
6 ICLKF<0:1>
ICLKF<0:1>
PLACED IN DPATH
16X-ONE FOR EACH I/O-CREATES ODD&EVEN BITS,
FROM RISING AND FALLING EDGE DATA
VINT
1 VINT
VINT
2 VSS
VSS
United Memories Inc.
Project: 128D14
Title
READ (I-LINE) DATA SORT CIRCUIT
Size
B
Document Number
IMUX
REV
A
Date: April 24, 2001
Sheet 1 of 1

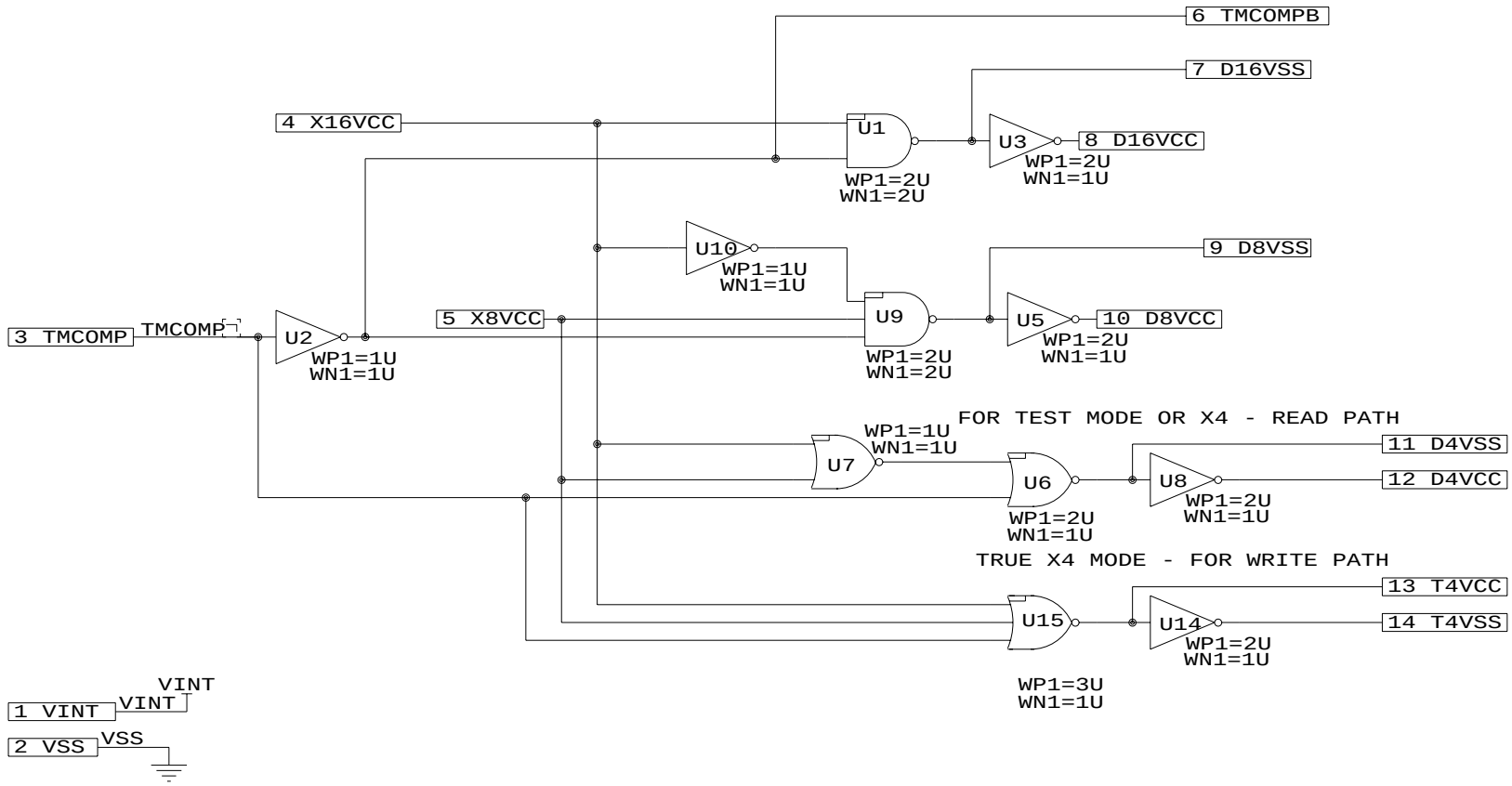


PLACED IN DPATH

16X-ONE FOR EACH I/O-CREATES ODD&EVEN BITS,
FROM RISING AND FALLING EDGE DATA

United Memories Inc.		
Project: 128D14		
Title	WRITE DATA SORT CIRCUIT	
Size B	Document Number WDSORT	REV A
Date: July 6, 2001	Sheet 1 of 1	


IO<0>
IO<1>
IO<3>
IO<2>
X16
X8
X4
TMCOMP
NORMAL
D16VSS
D16VCC
D8VSS
D8VCC
T4VSS
T4VCC
TMCOMPB
TMCOMP
PF
NF
W=2U
W=1U
M7
M8
M5
M6
M3
M4
M1
M2
M15
M16
M13
M14
M11
M12
M9
M10
M17
M18
M19
M20
M21
M22
M23
M24
M27
M28
M25
M26
I0
I1
I2
I3
I<0>
I<1>
I<2>
I<3>
TKD<0>
TKD<1>
TKD<3>
TKD<2>
U4
U3
U1
U2
WP1=8U
WN1=4U
WD<0>
WD<1>
WD<3>
WD<2>
CPARR0
CPARR1
CPARR3
CPARR2
18F
FOR EVERY PART CONFIGURATION,
FROM WHICH I<X> IS WD<X> DERIVED
(TRUE FOR RISING AND FALLING)
WD<X> 0 1 2 3
X16 0 1 2 3
X8 0 0 2 2
X4 2 2 2 2
TMCOMP TK0 TK1 TK2 TK3
1 VINT
2 VSS
VINT
INPUT STEERING CONTROL,
DC SIGNALS - ROUTE IN ANYTHING
3 D16VCC D16VCC
4 D16VSS D16VSS
5 D8VCC D8VCC
6 D8VSS D8VSS
7 T4VCC D4VCC
8 T4VSS D4VSS
9 TMCOMP TMCOMP
10 TMCOMPB TMCOMPB
IR OR IF
INPUT DATA - BIDIRECTIONAL BUS
11 I<0:3> I<0:3>
WDR OR WDF
OUTPUT DATA - WRITE DATA
12 WD<0:3> WD<0:3>
13 TKD<0:3> TKD<0:3>
PLACED IN DPATH
UNITED MEMORIES INC.
PROJECT:128DDR
Title
WRITE DATA MUX POINT (X4/X8/16) (Ir and If)
Size B
Document Number WMUX
REV A
Date: October 16, 2001
Sheet 1 of 1

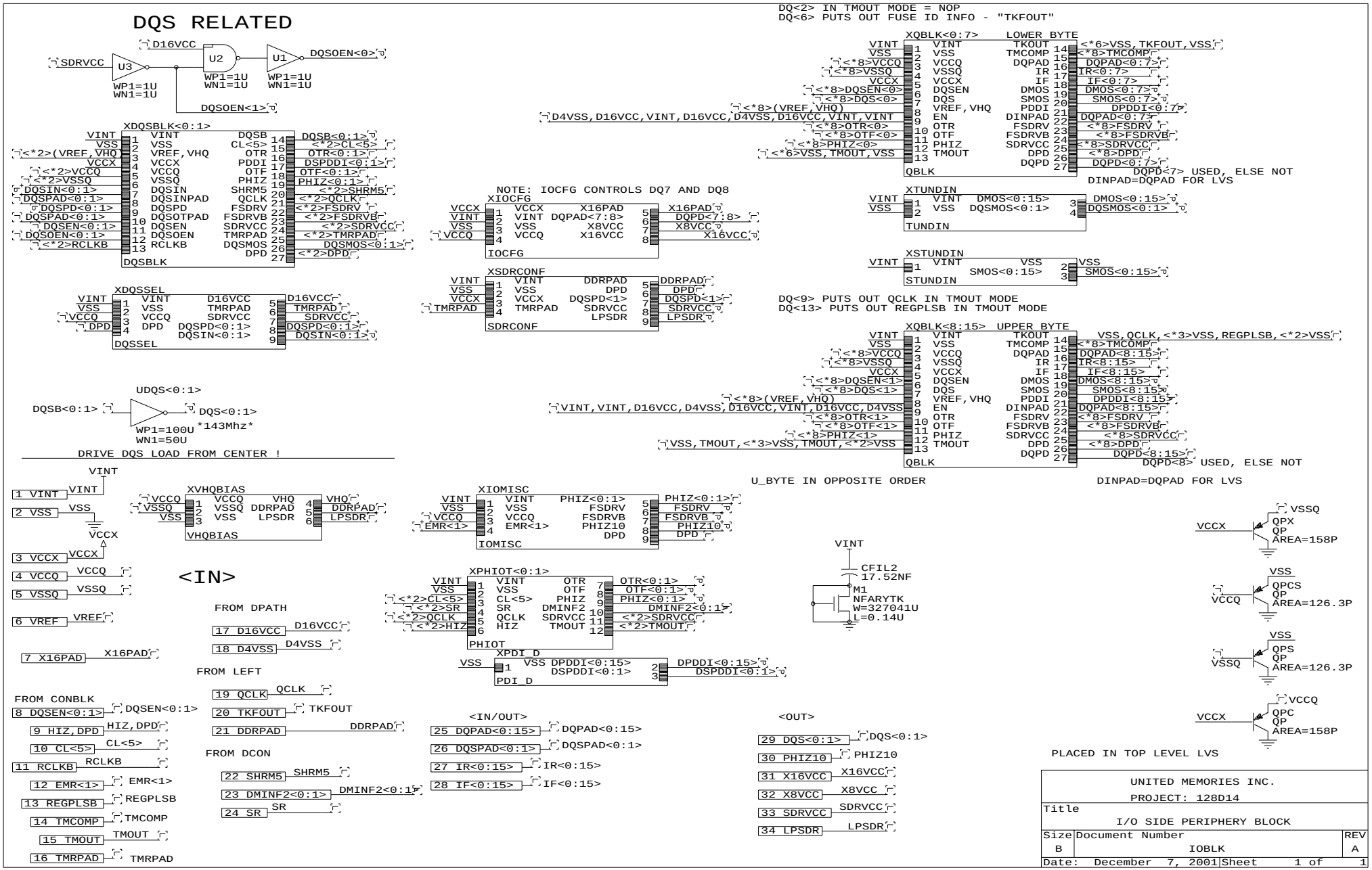


X16VCC AND X8VCC ARE NOW GENERATED
IN IOBLK/IOCFG,
THEY ARE NOT CONNECTED DIRECTLY
TO OPTION PADS.
JAF 8/15/01

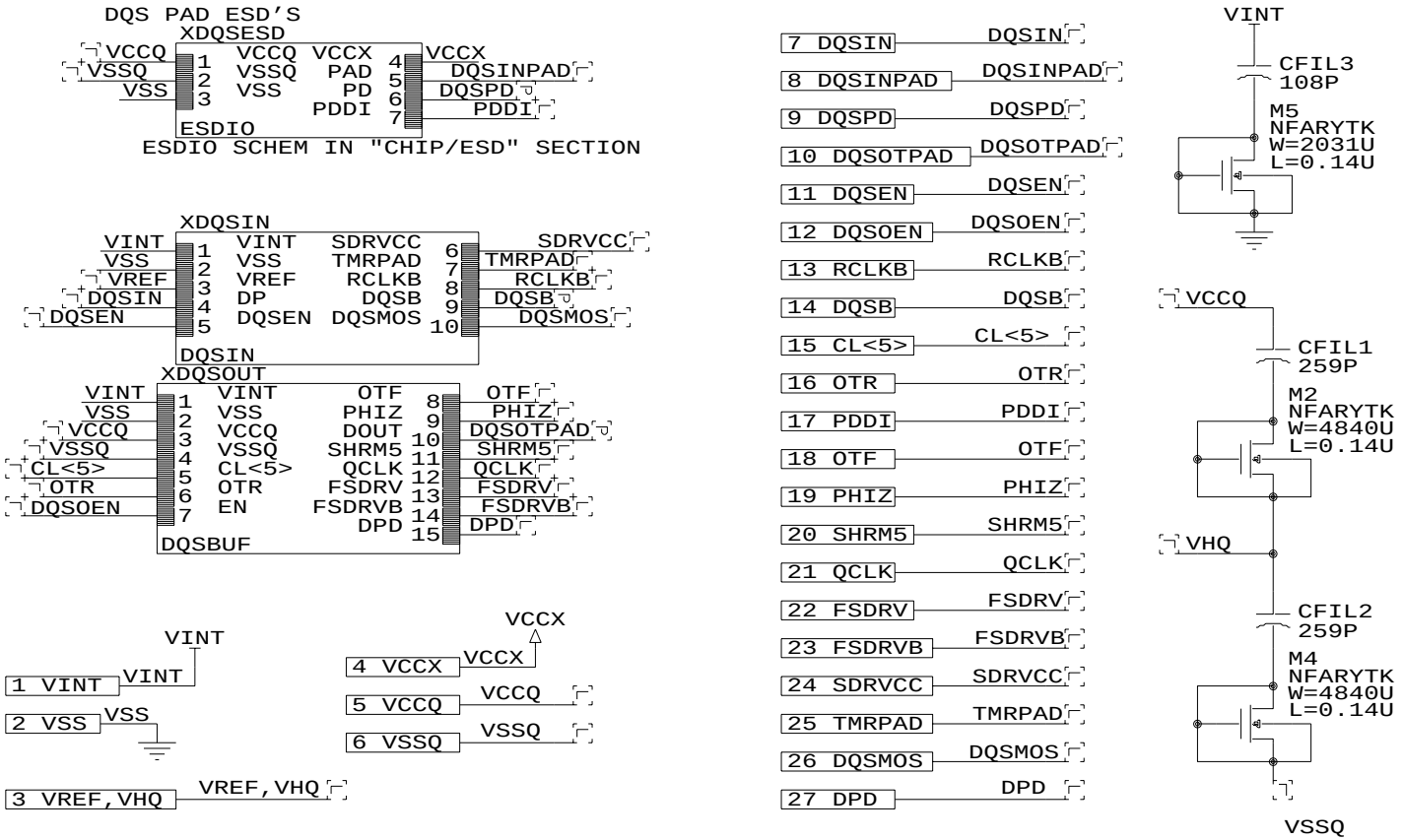
PLACED IN DPATH

UNITED MEMORIES INC. PROJECT: 128D14		
Title WMUX CONTROL LOGIC		
Size A	Document Number WMUXCON	REV A
Date: August 15, 2001	Sheet 1 of 1	

DQS RELATED

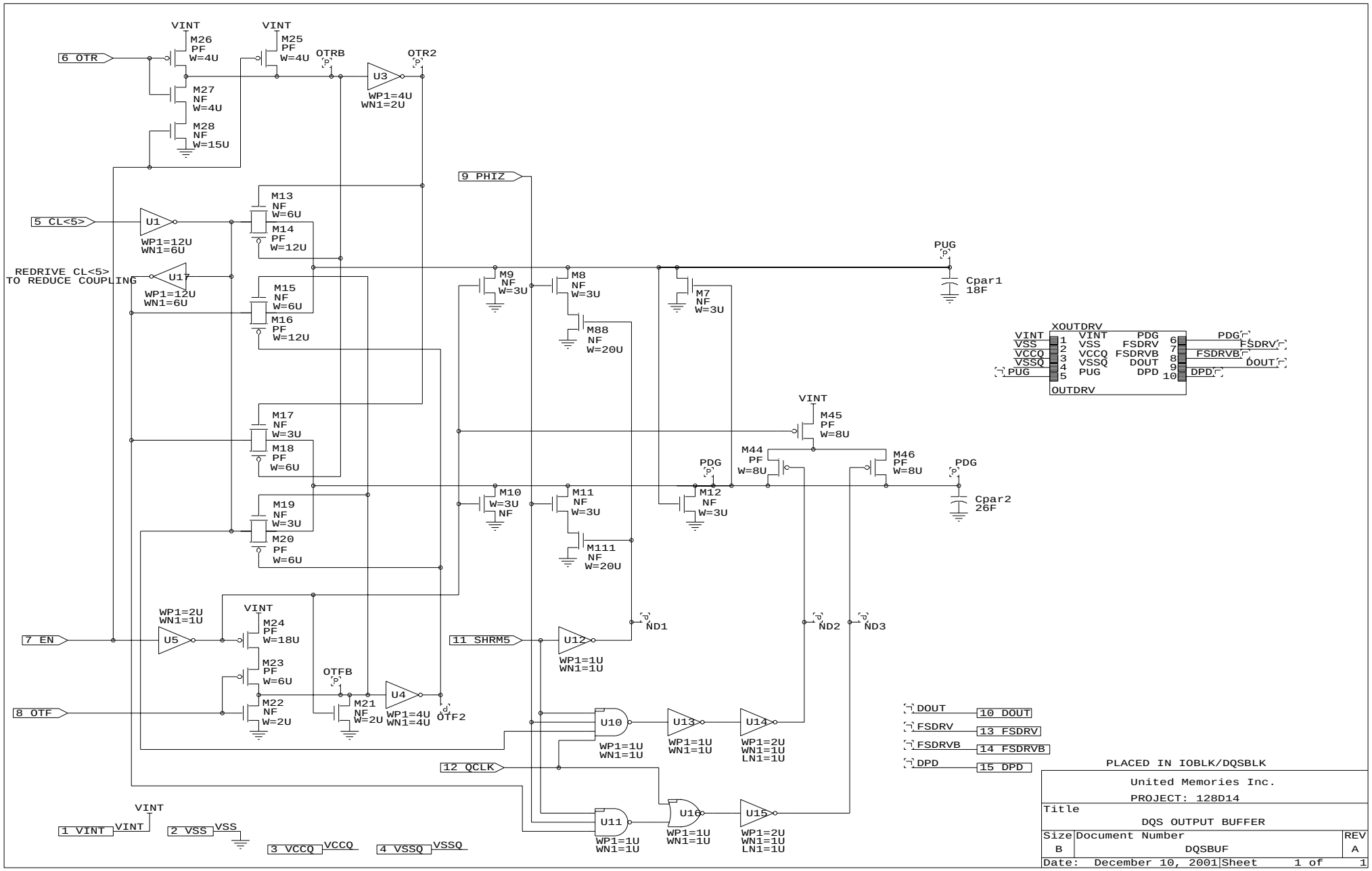


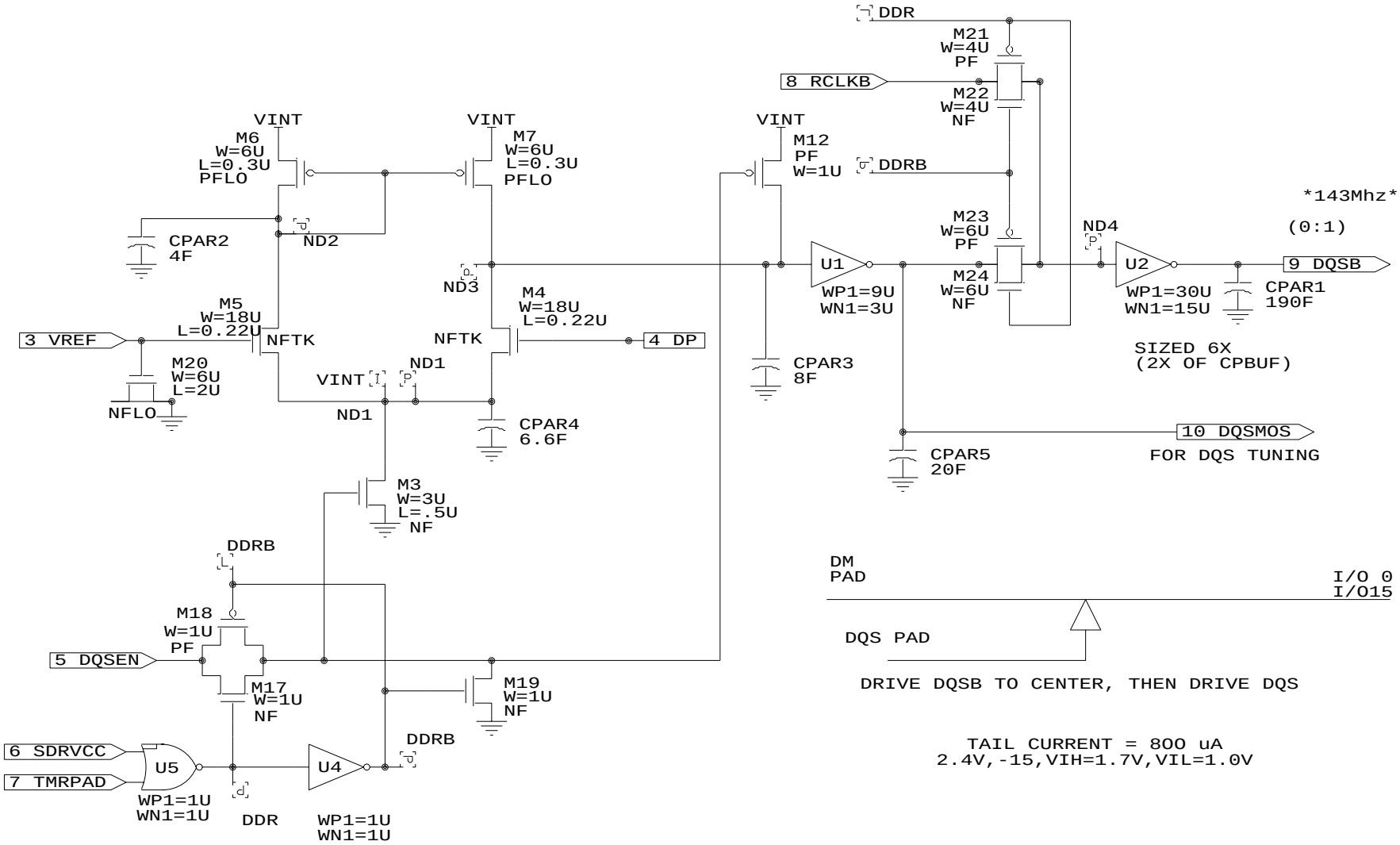
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	I/O SIDE PERIPHERY BLOCK	
Size B	Document Number IOBLK	REV A
Date: December 7, 2001	Sheet 1 of 1	



PLACED IN IOBLK

UNITED MEMORIES INC. PROJECT: 128D14		
Title DQS BLOCK		
Size A	Document Number DQSBLK	REV A
Date: December 7, 2001	Sheet 1 of 1	


6 OTR
VINT
M26
PF
W=4U
M27
NF
W=4U
M28
NF
W=15U
M25
PF
W=4U
OTRB
OTR2
U3
WP1=4U
WN1=2U
9 PHIZ
5 CL<5>
U1
WP1=12U
WN1=6U
M13
NF
W=6U
M14
PF
W=12U
REDRIVE CL<5>
TO REDUCE COUPLING
U17
WP1=12U
WN1=6U
M15
NF
W=6U
M16
PF
W=12U
M17
NF
W=3U
M18
PF
W=6U
M19
NF
W=3U
M20
PF
W=6U
M9
NF
W=3U
M8
NF
W=3U
M88
NF
W=20U
M7
NF
W=3U
PUG
Cpar1
18F
XOUTDRV
VINT
VSS
VCCQ
VSSQ
PUG
OUTDRV
PDG
FSDRV
FSDRVB
DOUT
DPD
M45
PF
W=8U
M44
PF
W=8U
M46
PF
W=8U
M10
W=3U
NF
M11
NF
W=3U
M111
NF
W=20U
M12
NF
W=3U
Cpar2
26F
WP1=2U
WN1=1U
U5
7 EN
M24
PF
W=18U
M23
PF
W=6U
M22
NF
W=2U
OTFB
M21
NF
W=2U
U4
WP1=4U
WN1=4U
OTF2
8 OTF
11 SHRM5
U12
WP1=1U
WN1=1U
ND1
ND2
ND3
U10
WP1=1U
WN1=1U
U13
WP1=1U
WN1=1U
U14
WP1=2U
WN1=1U
LN1=1U
12 QCLK
U11
WP1=1U
WN1=1U
U16
WP1=1U
WN1=1U
U15
WP1=2U
WN1=1U
LN1=1U
DOUT
10 DOUT
FSDRV
13 FSDRV
FSDRVB
14 FSDRVB
DPD
15 DPD
1 VINT
2 VSS
3 VCCQ
4 VSSQ
PLACED IN IOBLK/DQSBLK
United Memories Inc.
PROJECT: 128D14
Title
DQS OUTPUT BUFFER
Size
B
Document Number
DQSBUF
REV
A
Date: December 10, 2001
Sheet 1 of 1



PLACED IN IOBLK/DQSBLK

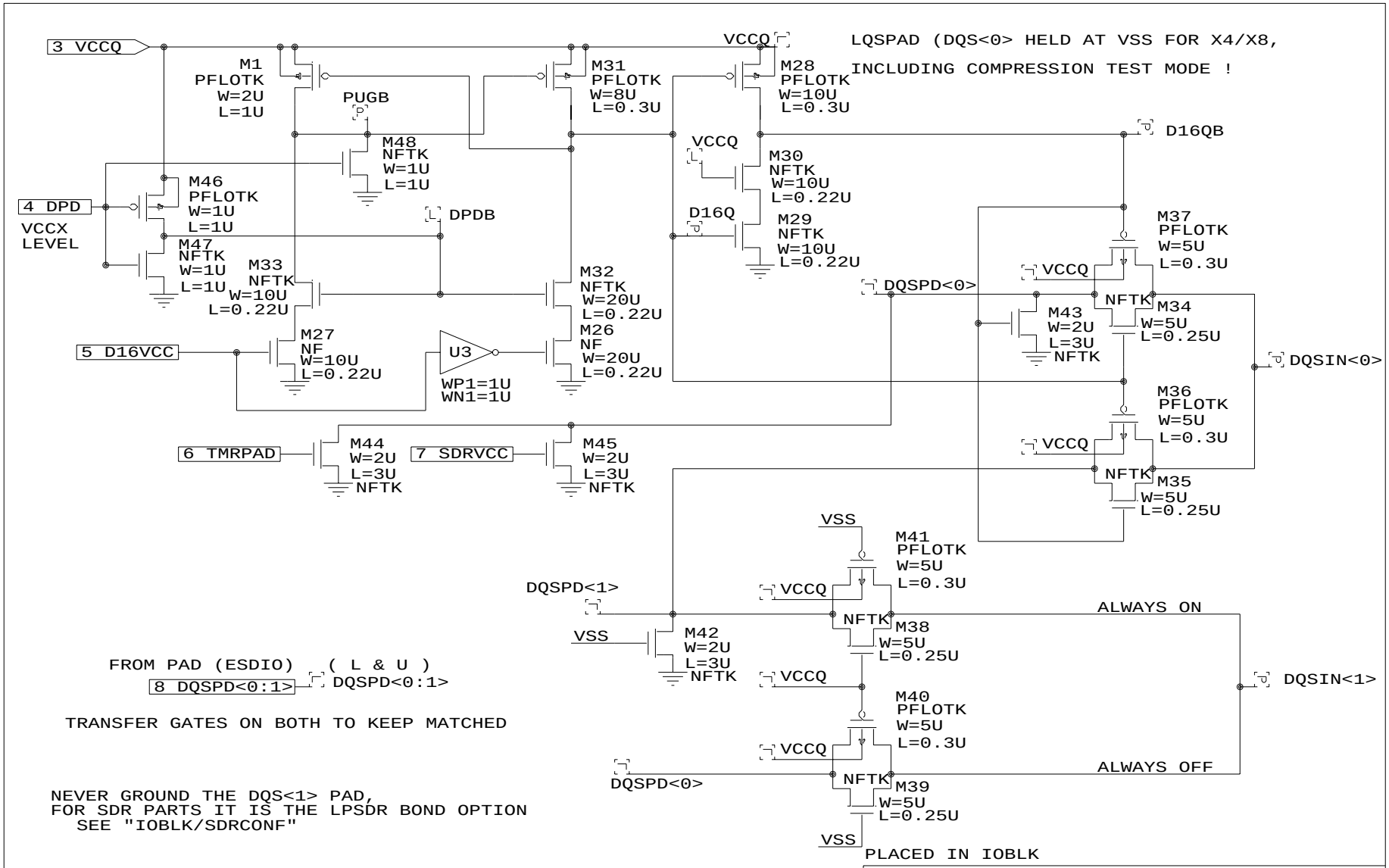
GROUND DQS PADS IF NOT USED,
IN RPAD, TOGGLE DQS TO FOOL DQSEN/GLW CIRCUIT

VINT

1 VINT VINT

2 VSS VSS

United Memories Inc. PROJECT: 128D14		
Title DQS INPUT BUFFER - SSTL		
Size A	Document Number DQSIN	REV A
Date: November 1, 2001	Sheet 1 of 1	



UNITED MEMORIES INC.

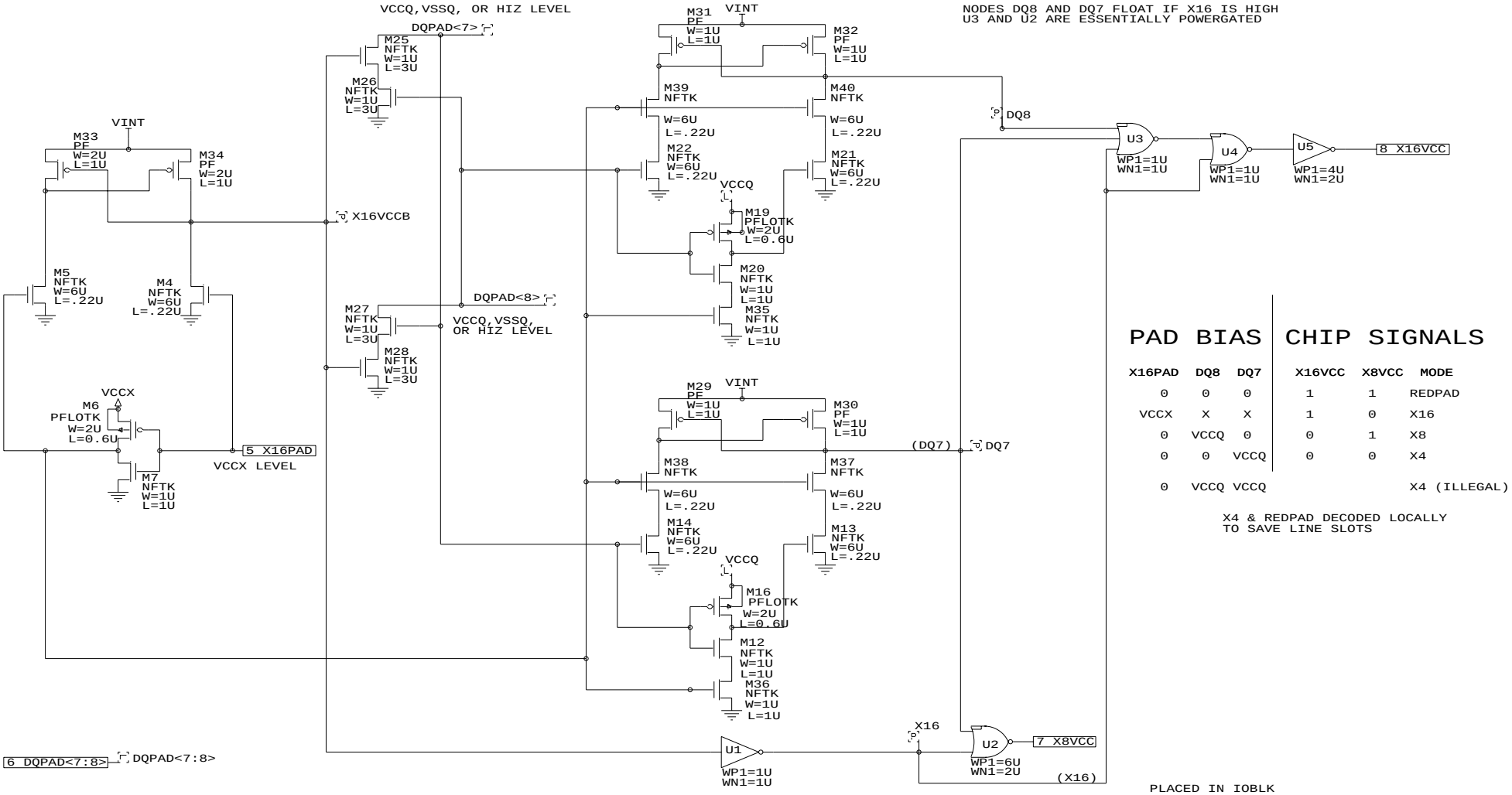
PROJECT: 128D14

Title

SELECTION FOR DQS (L ONLY USED FOR X16)

Size	Document Number	REV
A	DQSSEL	A

Date: November 1, 2001 Sheet 1 of 1



PAD BIAS | CHIP SIGNALS

X16PAD	DQ8	DQ7	X16VCC	X8VCC	MODE
0	0	0	1	1	REDPAD
VCCX	X	X	1	0	X16
0	VCCQ	0	0	1	X8
0	0	VCCQ	0	0	X4
0	VCCQ	VCCQ			X4 (ILLEGAL)

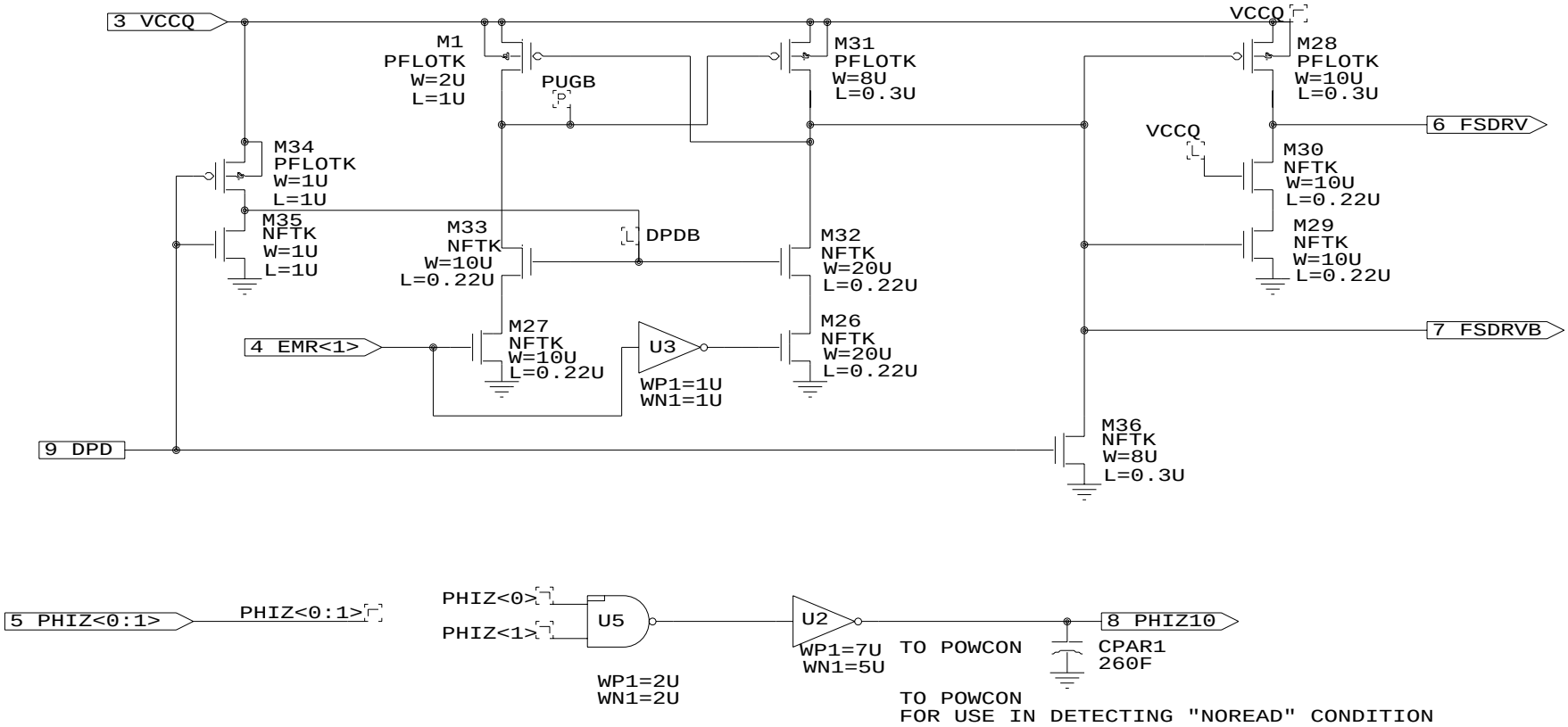
X4 & REDPAD DECODED LOCALLY
TO SAVE LINE SLOTS

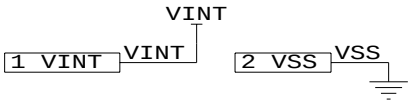
** EN SIGNAL FOR DQPADS(7,8) = VINT
SO ONLY THIS CIRCUIT CONTROLS THEM!

1 VCCX VCCX
2 VINT VINT
3 VSS
4 VCCQ VCCQ

PLACED IN IOBLK

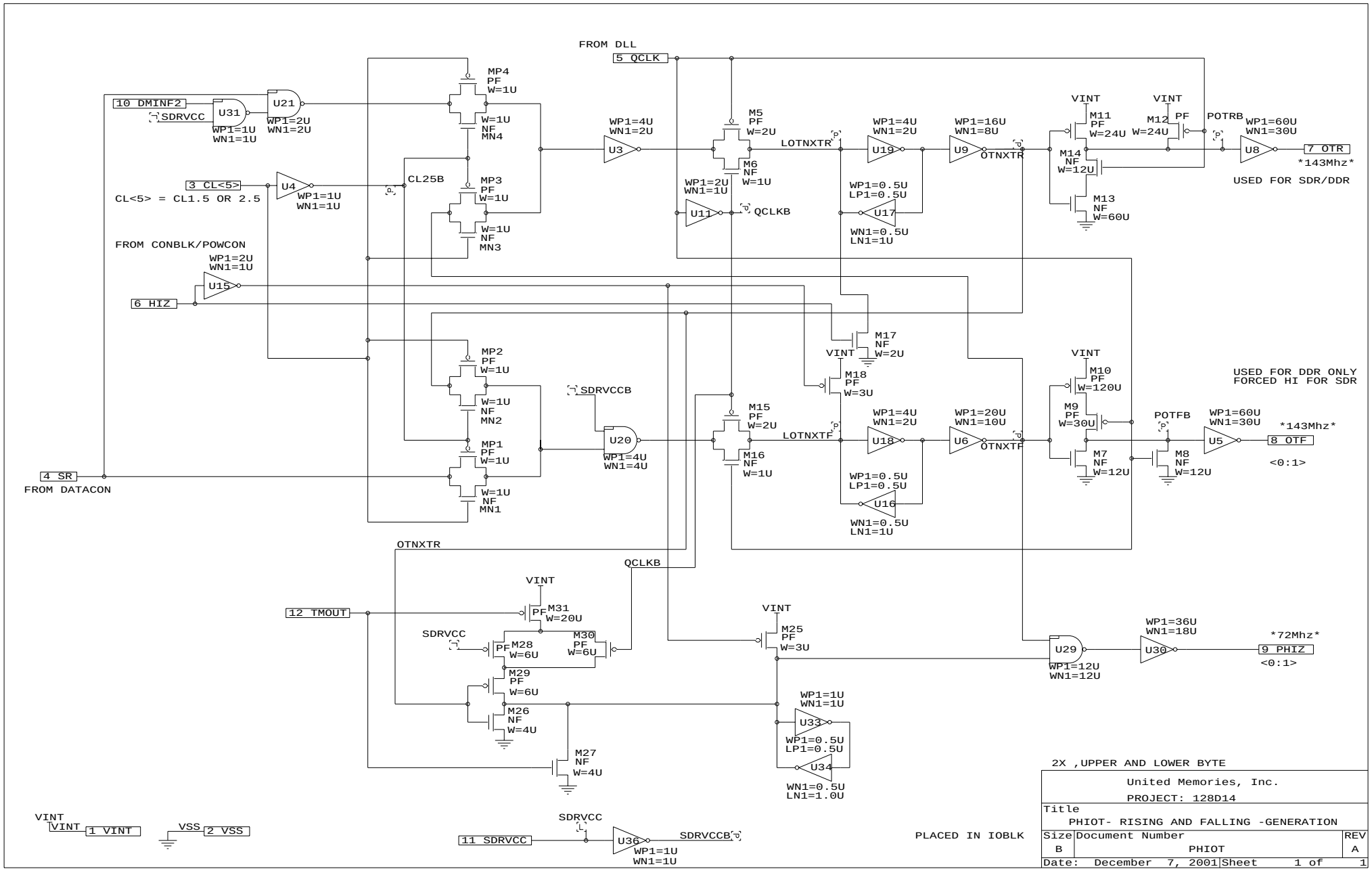
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title: I/O CONFIGURATION (X16/X8)		
Size: B	Document Number: IOCFG	REV: A
Date: October 30, 2001	Sheet 1 of 1	

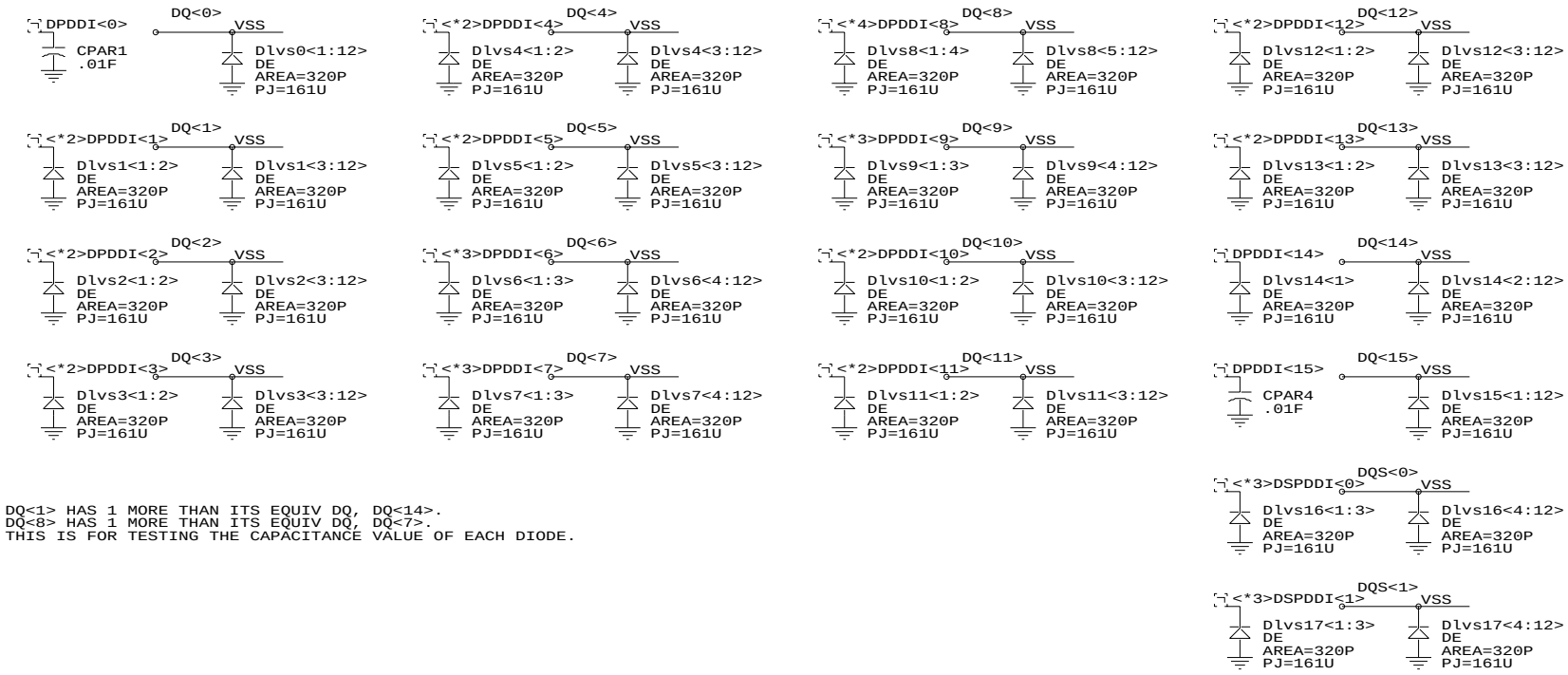




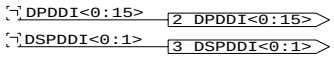
PLACED IN IOBLK

United Memories Inc. PROJECT: 128D14		
Title IO MISC CKTS		
Size A	Document Number IOMISC	REV A
Date: October 29, 2001	Sheet 1 of 1	


FROM DLL
5 QCLK
10 DMINF2
SDRVCC
U31
WP1=1U
WN1=1U
U21
WP1=2U
WN1=2U
MP4
PF
W=1U
W=1U
NF
MN4
3 CL<5>
U4
WP1=1U
WN1=1U
CL<5> = CL1.5 OR 2.5
CL25B
MP3
PF
W=1U
W=1U
NF
MN3
FROM CONBLK/POWCON
WP1=2U
WN1=1U
U15
6 HIZ
MP2
PF
W=1U
W=1U
NF
MN2
MP1
PF
W=1U
W=1U
NF
MN1
4 SR
FROM DATACON
SDRVCCB
U20
WP1=4U
WN1=4U
WP1=4U
WN1=2U
U3
M5
PF
W=2U
M6
NF
W=1U
WP1=2U
WN1=1U
U11
QCLKB
LOTNXTR
WP1=4U
WN1=2U
U19
WP1=16U
WN1=8U
U9
OTNXTR
WP1=0.5U
LP1=0.5U
U17
WN1=0.5U
LN1=1U
VINT
M11
PF
W=24U
M12
PF
W=24U
POTRB
WP1=60U
WN1=30U
U8
7 OTR
143Mhz
M14
NF
W=12U
M13
NF
W=60U
USED FOR SDR/DDR
M17
NF
W=2U
M18
PF
W=3U
M15
PF
W=2U
M16
NF
W=1U
LOTNXTF
WP1=4U
WN1=2U
U18
WP1=20U
WN1=10U
U6
OTNXTF
WP1=0.5U
LP1=0.5U
U16
WN1=0.5U
LN1=1U
M10
PF
W=120U
M9
PF
W=30U
M7
NF
W=12U
USED FOR DDR ONLY
FORCED HI FOR SDR
POTFB
M8
NF
W=12U
WP1=60U
WN1=30U
U5
143Mhz
8 OTF
<0:1>
OTNXTR
QCLKB
VINT
12 TMOUT
PF M31
W=20U
SDRVCC
PF M28
W=6U
M30
PF
W=6U
M29
PF
W=6U
M26
NF
W=4U
M27
NF
W=4U
VINT
M25
PF
W=3U
WP1=1U
WN1=1U
U33
WP1=0.5U
LP1=0.5U
U34
WN1=0.5U
LN1=1.0U
U29
WP1=12U
WN1=12U
WP1=36U
WN1=18U
U30
72Mhz
9 PHIZ
<0:1>
VINT
VINT
1 VINT
VSS
2 VSS
SDRVCC
11 SDRVCC
U36
WP1=1U
WN1=1U
SDRVCCB
PLACED IN IOBLK
2X ,UPPER AND LOWER BYTE
United Memories, Inc.
PROJECT: 128D14
Title
PHIOT- RISING AND FALLING -GENERATION
Size
B
Document Number
PHIOT
REV
A
Date: December 7, 2001
Sheet 1 of 1

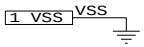


DQ<1> HAS 1 MORE THAN ITS EQUIV DQ, DQ<14>.
DQ<8> HAS 1 MORE THAN ITS EQUIV DQ, DQ<7>.
THIS IS FOR TESTING THE CAPACITANCE VALUE OF EACH DIODE.



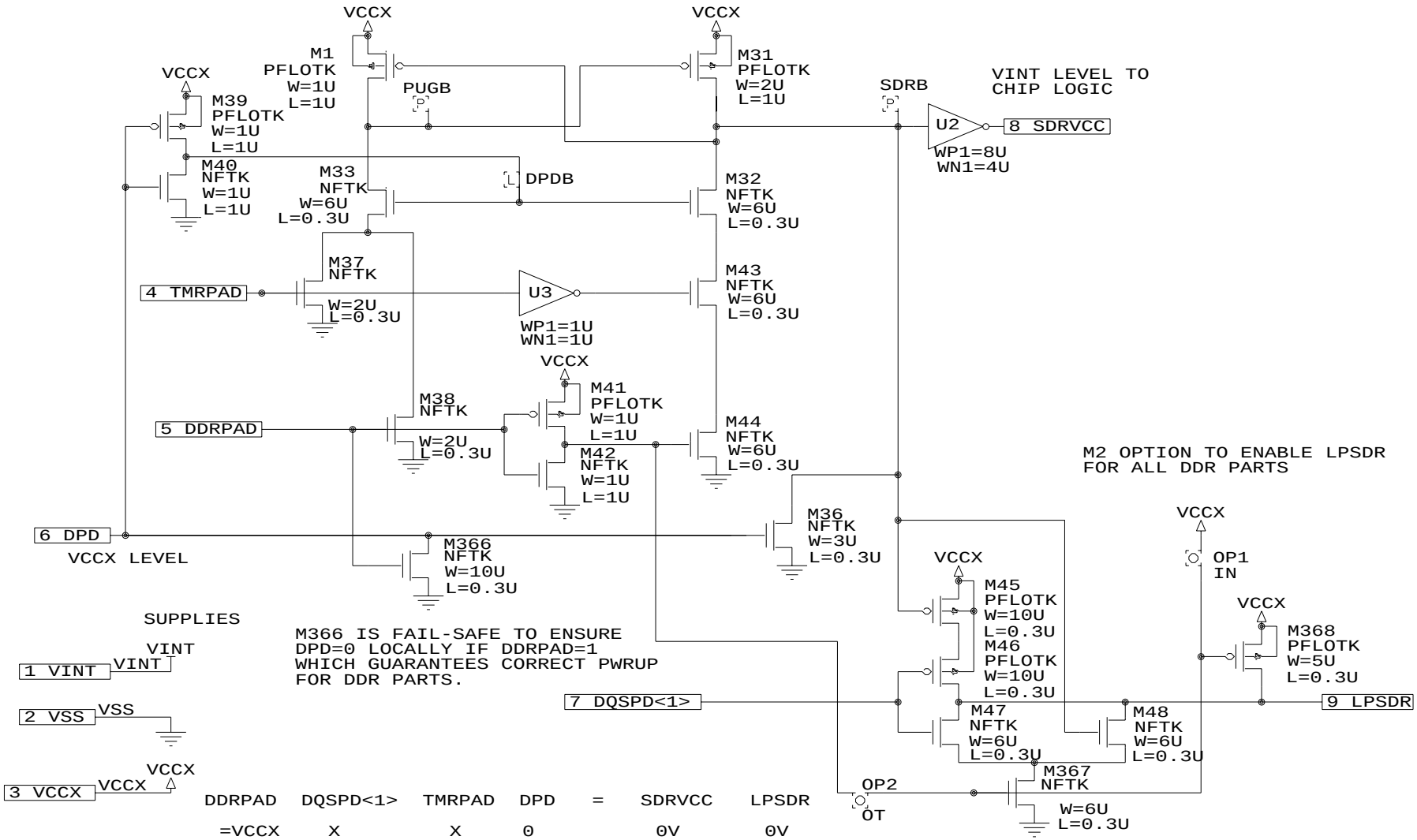
12 WELL DIODES UNDER THE PADS

THESE DIODES ARE TO ADD PAD CAPACITANCE



PLACED IN IOBLK

United Memories Inc.		
PROJECT: 128D14		
Title		
IO AND DQS PAD DIODES		
Size	Document Number	REV
B	PDI_D	A5
Date: September 22, 2001	Sheet 1 of 1	



DDRPAD	DQSPD<1>	TMRPAD	DPD	=	SDRVCC	LPSDR
=VCCX	X	X	0		0V	0V
X	X	VINT	0		0V	0V
0V	VCCQ	0	0		VINT	0V
(FOR NORMAL SDR, VCCQ=VCCX)						
VSSQ	VSSQ	0	0		VINT	VCCX
VSSQ	VSSQ	0	VCCX		VINT	VCCX

**DPD CAN'T EQUAL "1" UNLESS LPSDR IS SET

PLACED IN IOBLK

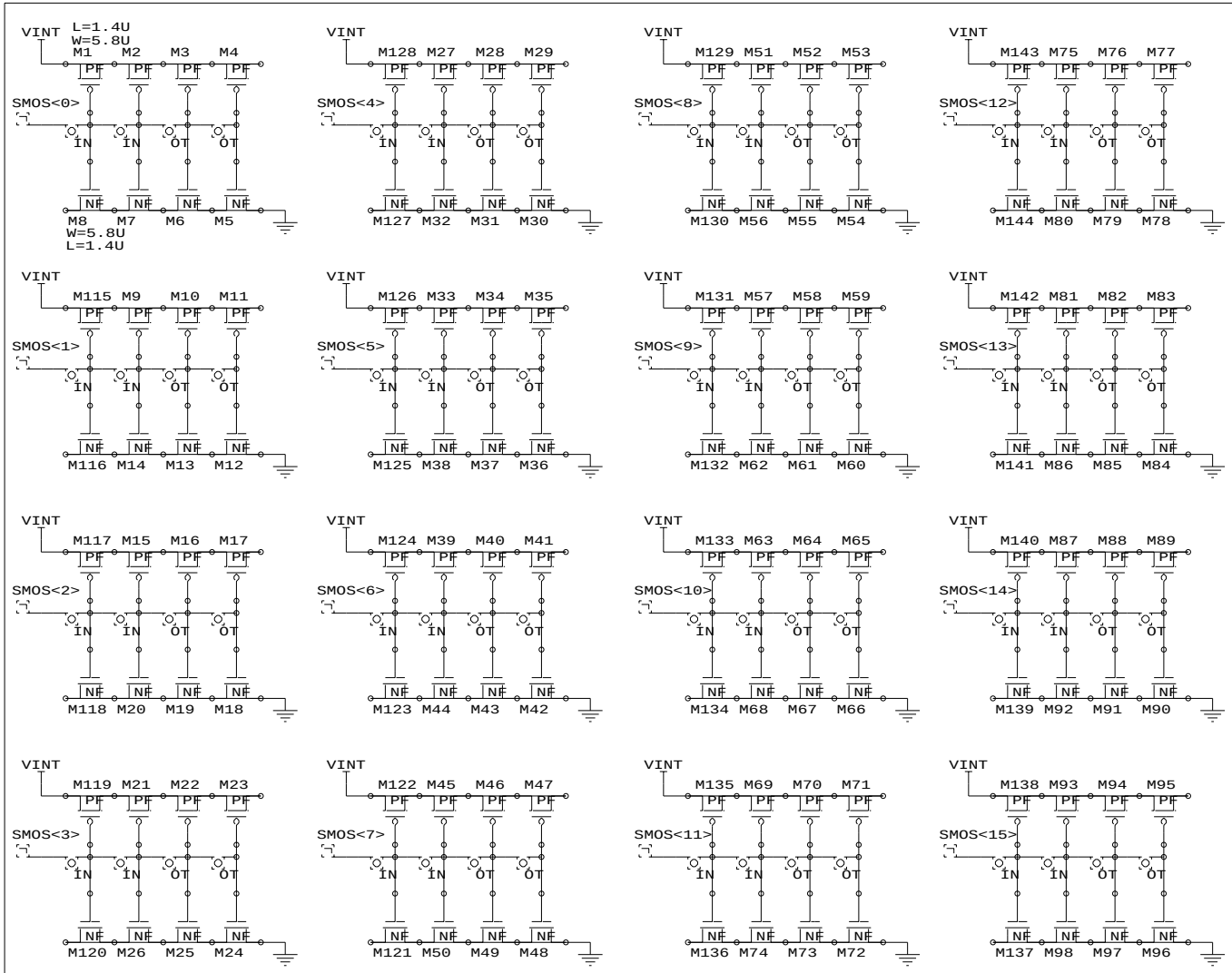
UNITED MEMORIES INC.

PROJECT:128D14

Title: SDRVCC / LPSDR GENERATION

Size	Document Number	REV
A	SDRCONF	A

Date: November 21, 2001 Sheet 1 of 1



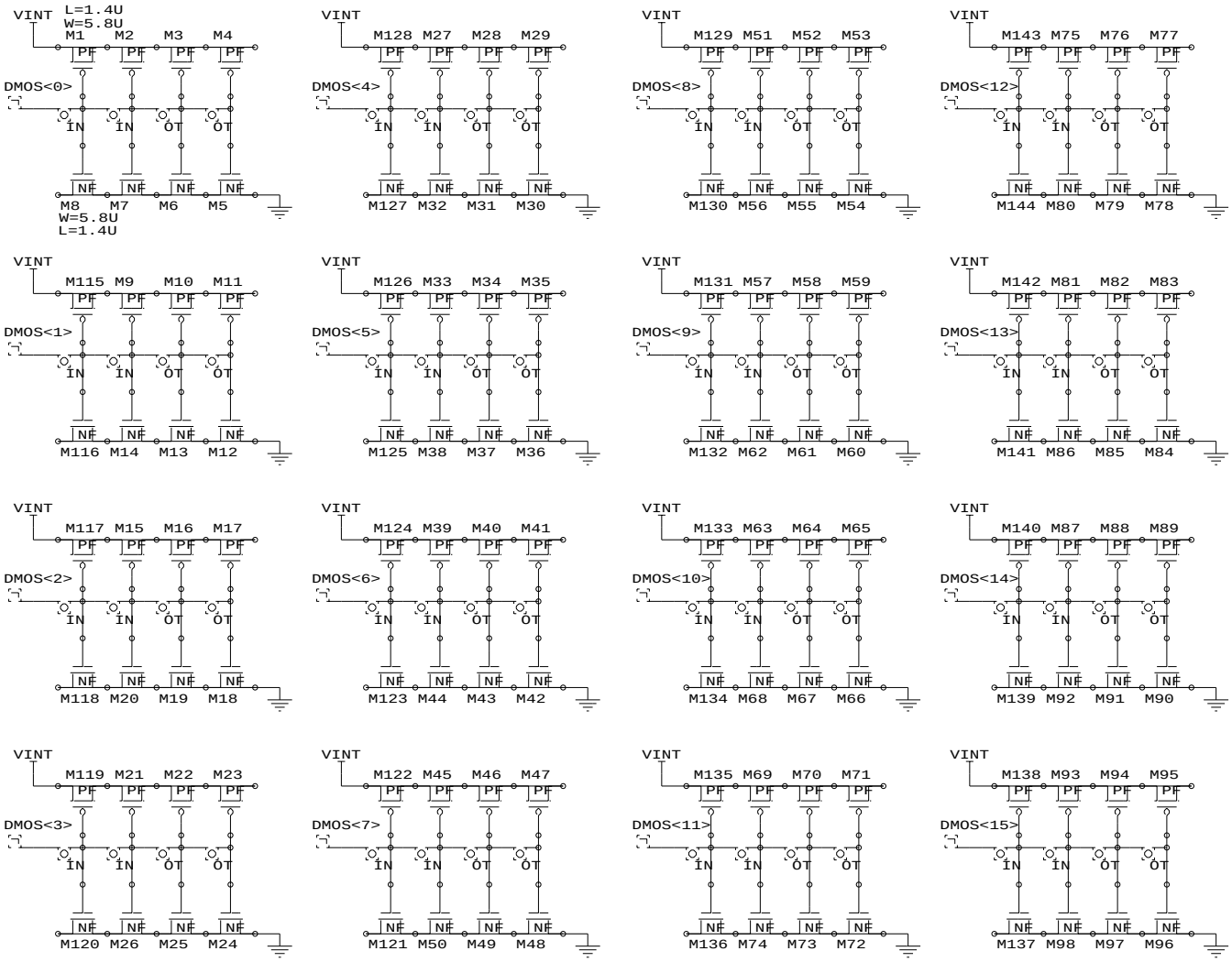
SIZED FOR 100PS/GATE

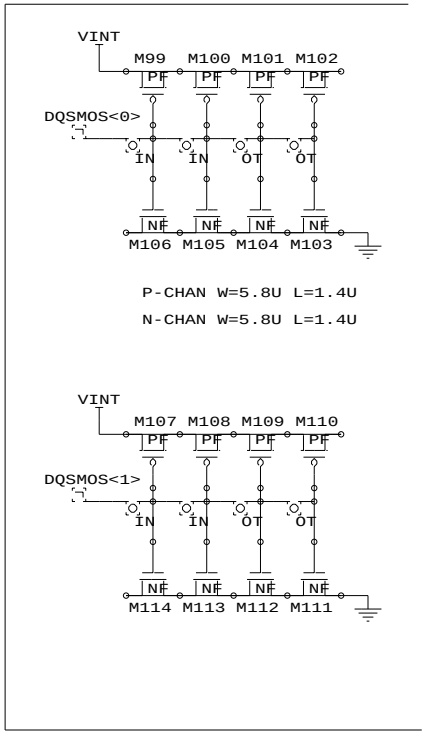
PLACED IN IOBLK

P-CHAN W=5.8U L=1.4U

N-CHAN W=5.8U L=1.4U

United Memories, Inc.		
PROJECT: 128D14		
Title TUNING CIRCUIT FOR DATA - SDR MODE		
Size B	Document Number STUNDIN	REV A4
Date: November 7, 2001	Sheet 1 of 1	



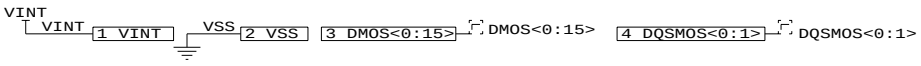


SIZED FOR 100PS/GATE

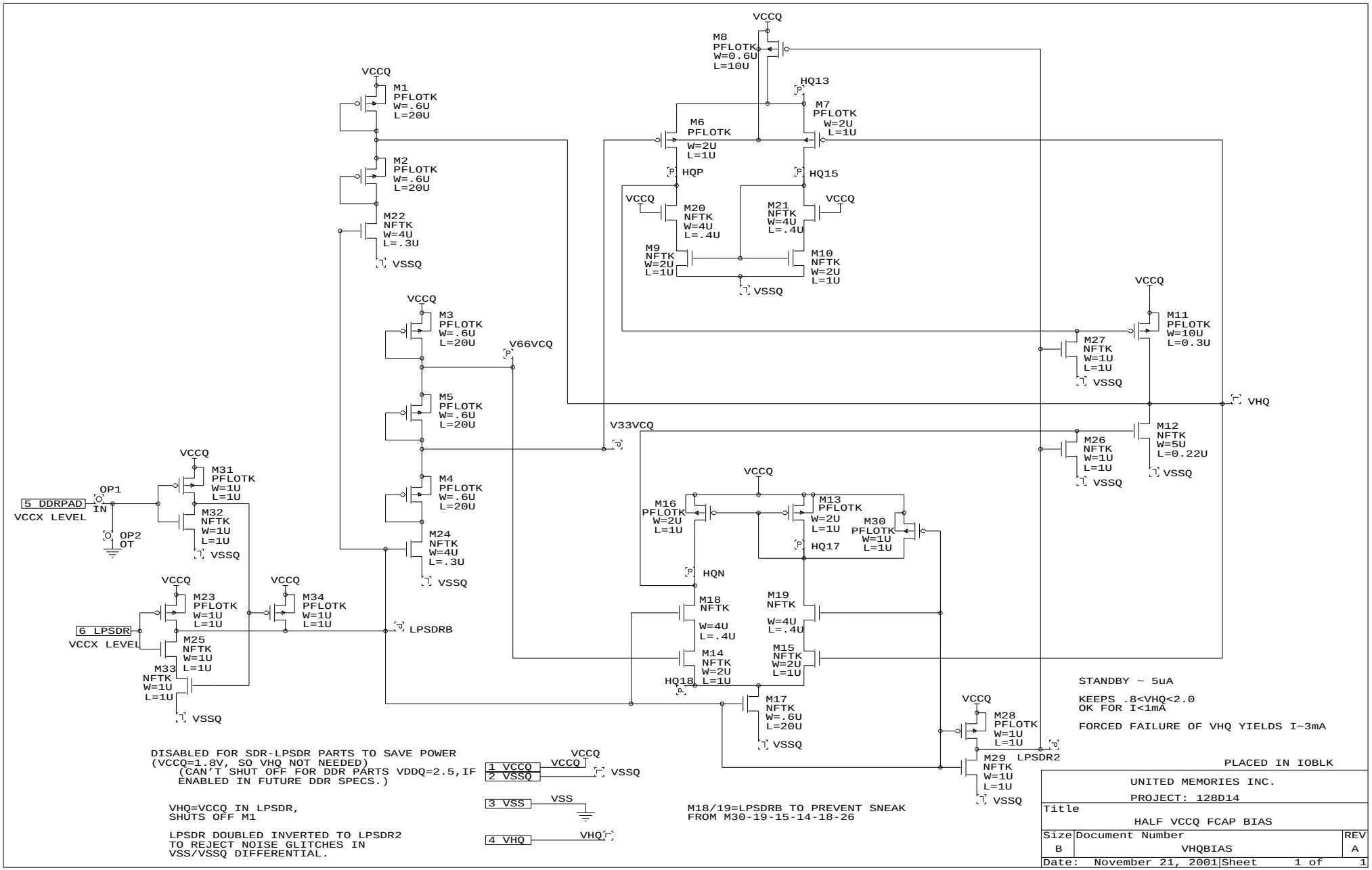
PLACED IN IOBLK

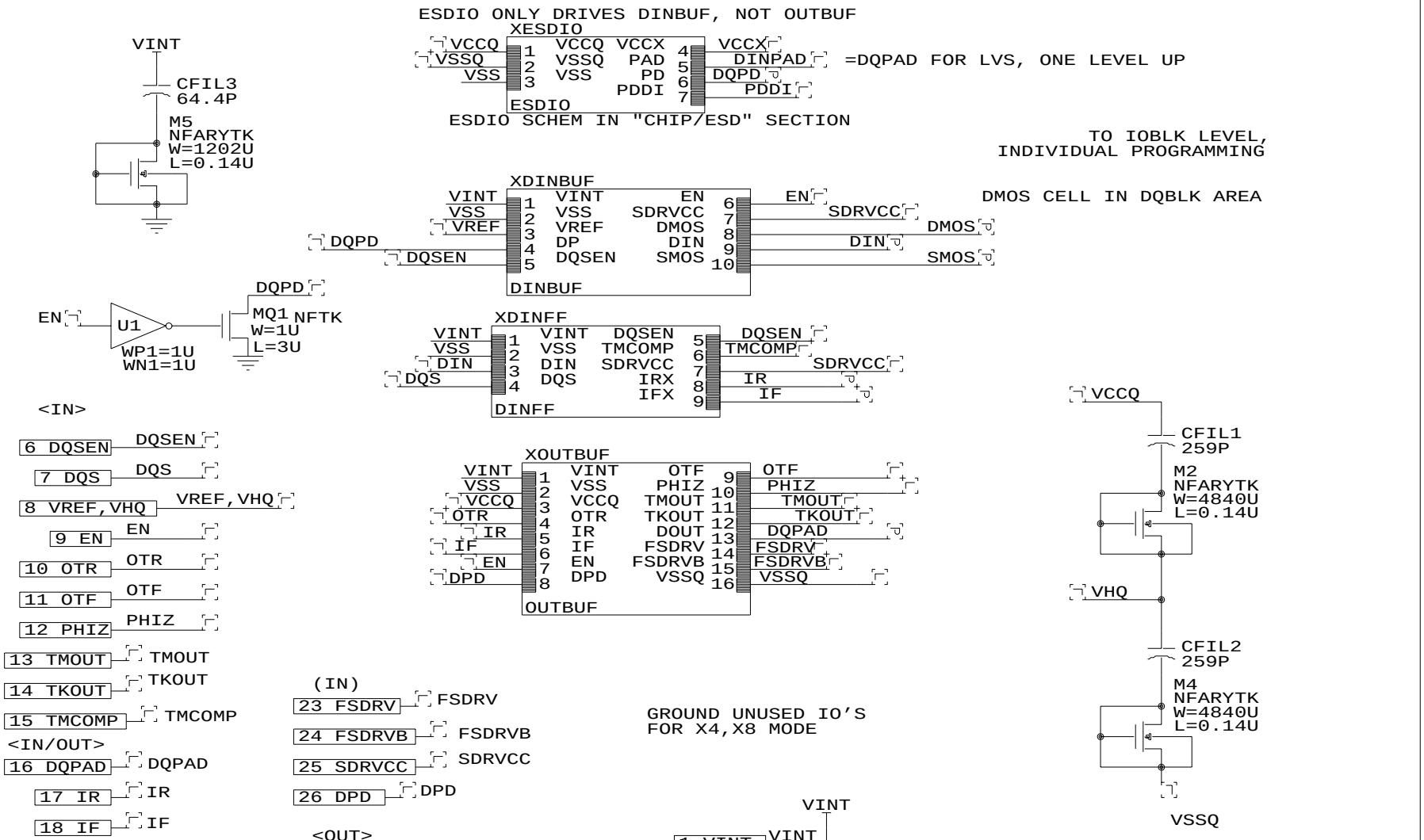
P-CHAN W=5.8U L=1.4U

N-CHAN W=5.8U L=1.4U

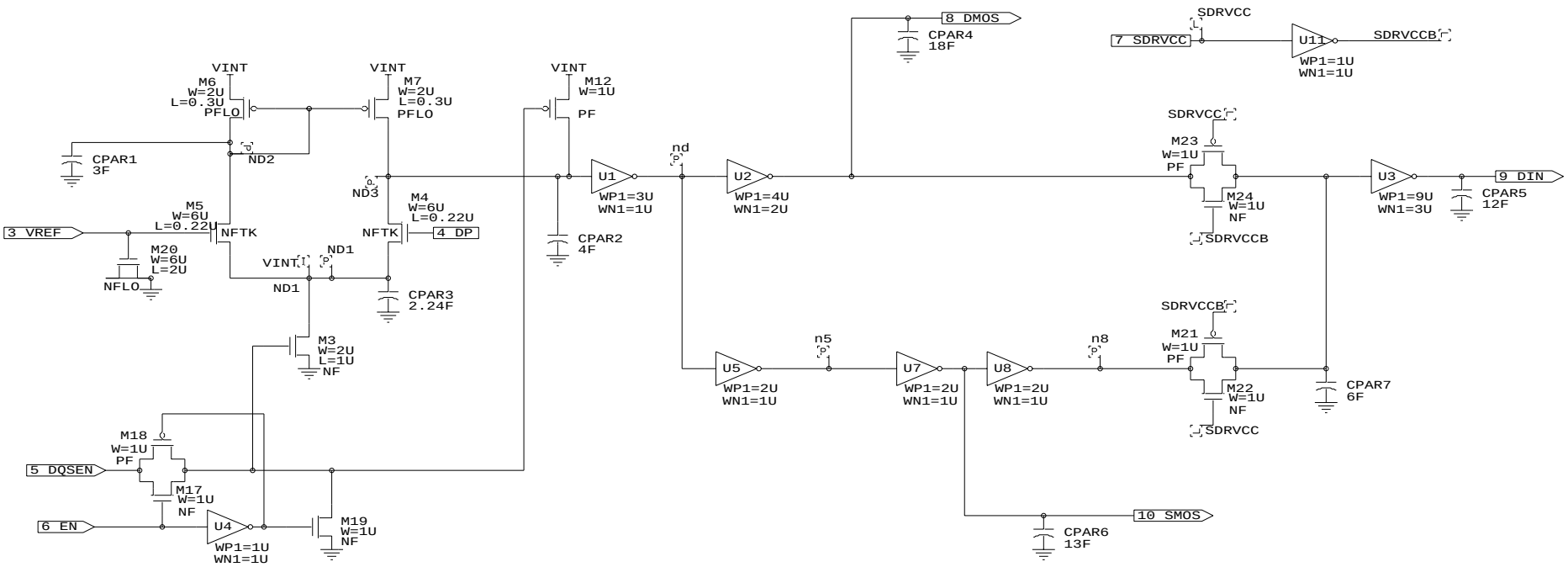


United Memories, Inc.		
PROJECT: 128D14		
Title		
TUNING CIRCUIT FOR DATA/DQS INPUTS		
Size B	Document Number TUNDIN	REV A4
Date: November 7, 2001	Sheet 1 of 1	


VCCQ
M8
PFLOTK
W=0.6U
L=10U
HQ13
M7
PFLOTK
W=2U
L=1U
M6
PFLOTK
W=2U
L=1U
HQP
HQ15
M20
NFTK
W=4U
L=.4U
M21
NFTK
W=4U
L=.4U
M9
NFTK
W=2U
L=1U
M10
NFTK
W=2U
L=1U
VSSQ
M1
PFLOTK
W=.6U
L=20U
M2
PFLOTK
W=.6U
L=20U
M22
NFTK
W=4U
L=.3U
M3
PFLOTK
W=.6U
L=20U
V66VCQ
M5
PFLOTK
W=.6U
L=20U
V33VCQ
M4
PFLOTK
W=.6U
L=20U
M24
NFTK
W=4U
L=.3U
M11
PFLOTK
W=10U
L=0.3U
M27
NFTK
W=1U
L=1U
VHQ
M12
NFTK
W=5U
L=0.22U
M26
NFTK
W=1U
L=1U
M31
PFLOTK
W=1U
L=1U
OP1
5 DDRPAD
IN
VCCX LEVEL
M32
NFTK
W=1U
L=1U
OP2
OT
M16
PFLOTK
W=2U
L=1U
M13
PFLOTK
W=2U
L=1U
M30
PFLOTK
W=1U
L=1U
HQ17
HQN
M18
NFTK
W=4U
L=.4U
M19
NFTK
W=4U
L=.4U
M14
NFTK
W=2U
L=1U
M15
NFTK
W=2U
L=1U
HQ18
M17
NFTK
W=.6U
L=20U
M23
PFLOTK
W=1U
L=1U
M34
PFLOTK
W=1U
L=1U
6 LPSDR
VCCX LEVEL
M25
NFTK
W=1U
L=1U
M33
NFTK
W=1U
L=1U
LPSDRB
M28
PFLOTK
W=1U
L=1U
M29
NFTK
W=1U
L=1U
LPSDR2
STANDBY ~ 5uA
KEEPS .8<VHQ<2.0
OK FOR I<1mA
FORCED FAILURE OF VHQ YIELDS I~3mA
PLACED IN IOBLK
DISABLED FOR SDR-LPSDR PARTS TO SAVE POWER
(VCCQ=1.8V, SO VHQ NOT NEEDED)
(CAN'T SHUT OFF FOR DDR PARTS VDDQ=2.5,IF
ENABLED IN FUTURE DDR SPECS.)
1 VCCQ
2 VSSQ
3 VSS
4 VHQ
VSS
VHQ=VCCQ IN LPSDR,
SHUTS OFF M1
LPSDR DOUBLED INVERTED TO LPSDR2
TO REJECT NOISE GLITCHES IN
VSS/VSSQ DIFFERENTIAL.
M18/19=LPSDRB TO PREVENT SNEAK
FROM M30-19-15-14-18-26
UNITED MEMORIES INC.
PROJECT: 128D14
Title
HALF VCCQ FCAP BIAS
Size
B
Document Number
VHQBIAS
REV
A
Date: November 21, 2001
Sheet 1 of 1



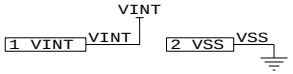
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	BLK AROUND I/O PAD	
Size A	Document Number QBLK	REV A
Date: December 4, 2001	Sheet 1 of 1	



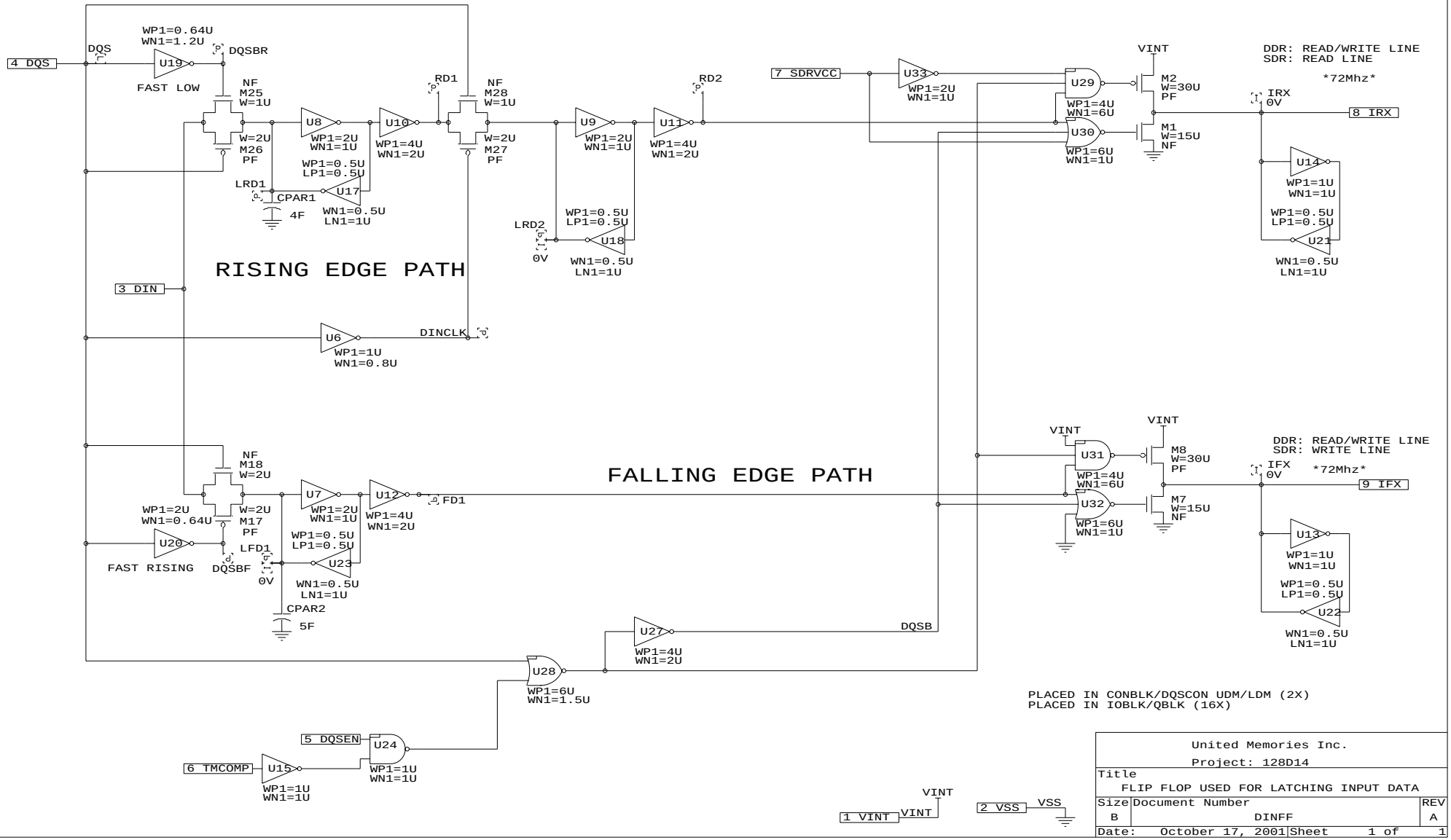
SIZED:1.5X
(0.5 OF CPBUF)

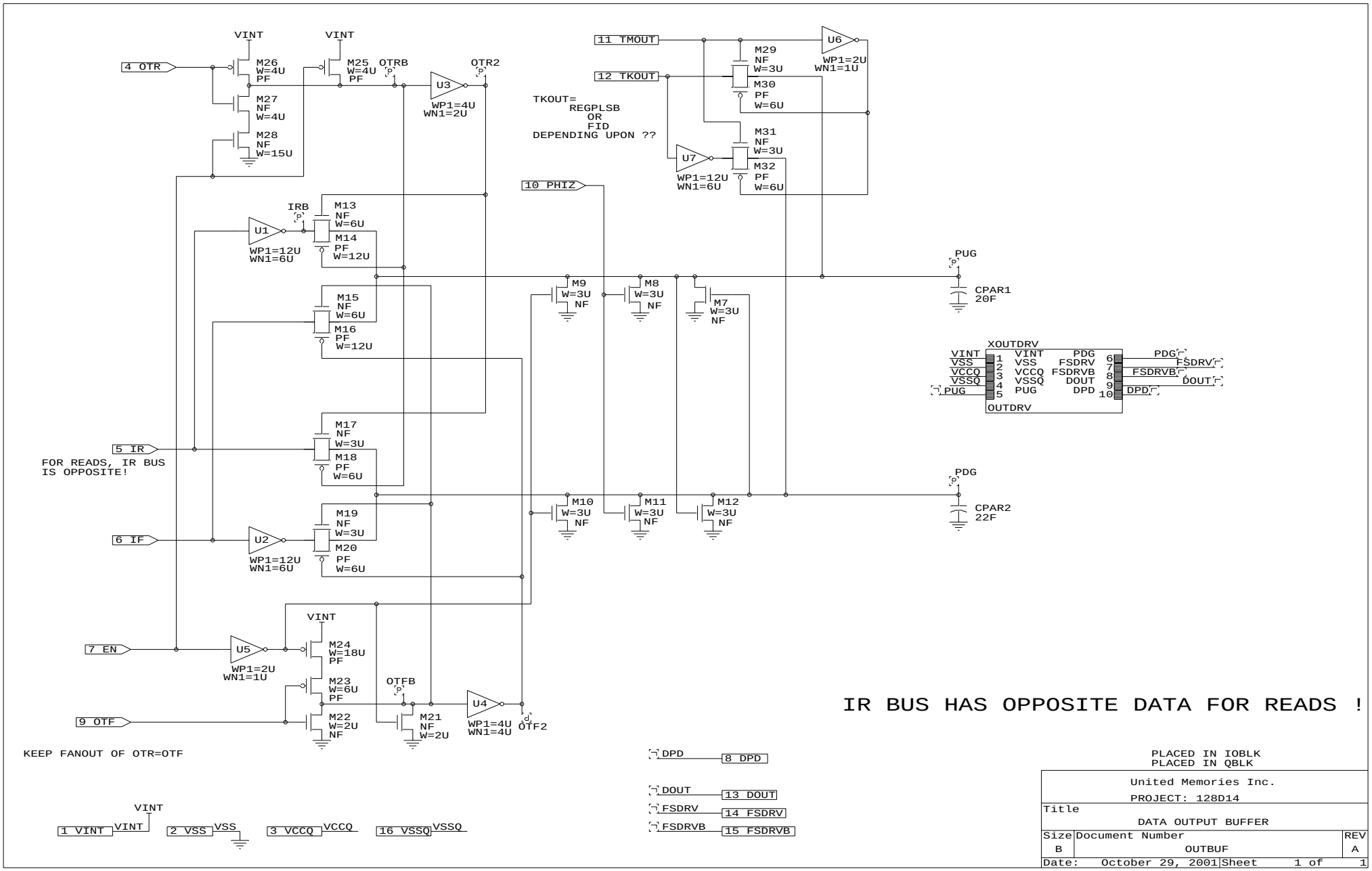
TAIL CURRENT = ????
2.4V,-15,VIH=1.7V,VIL=1.0V

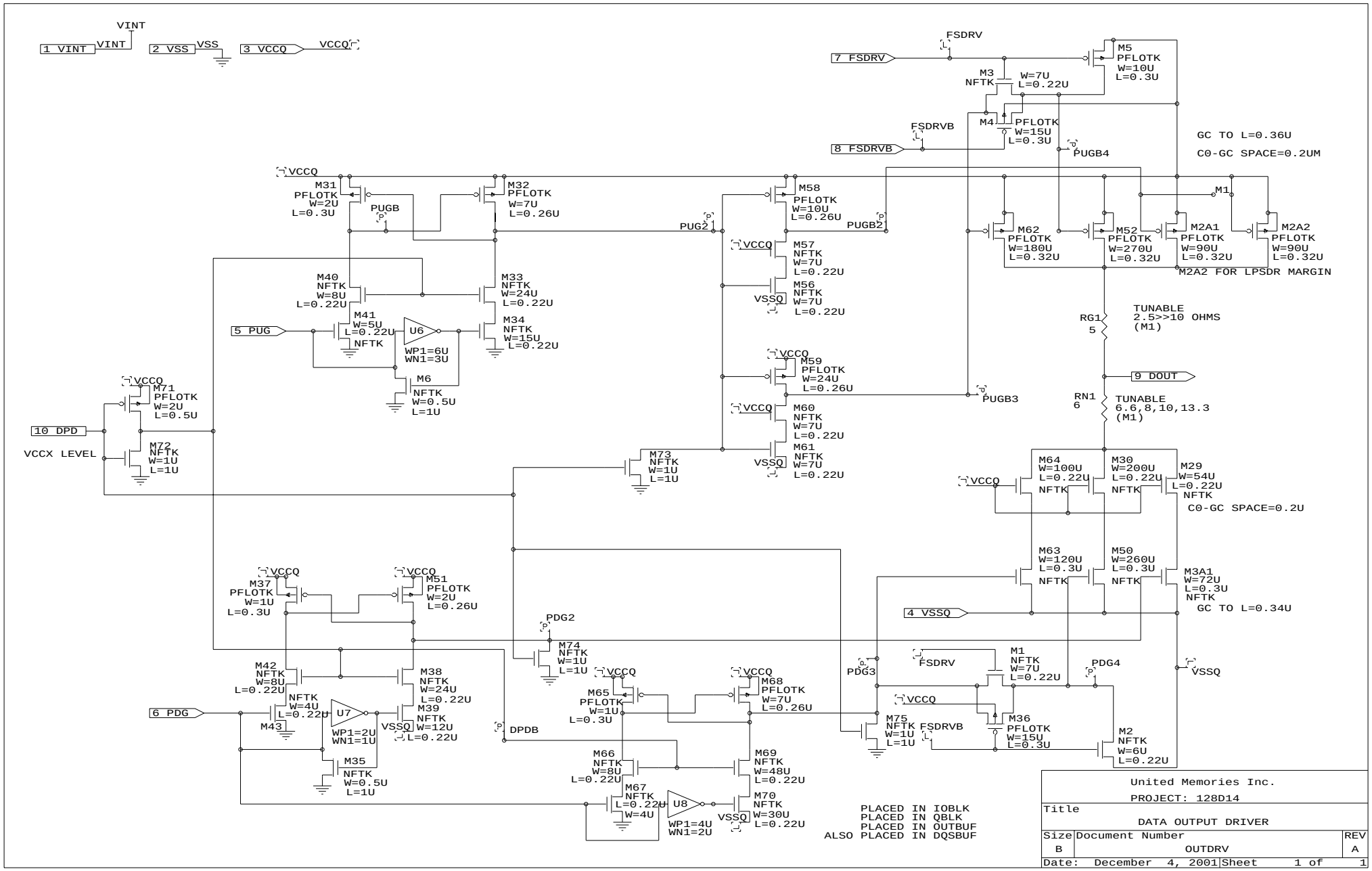
PLACED IN DQSCON -LDM/UDM
PLACED IN QBLK-DQ<0:15> SIGNALS

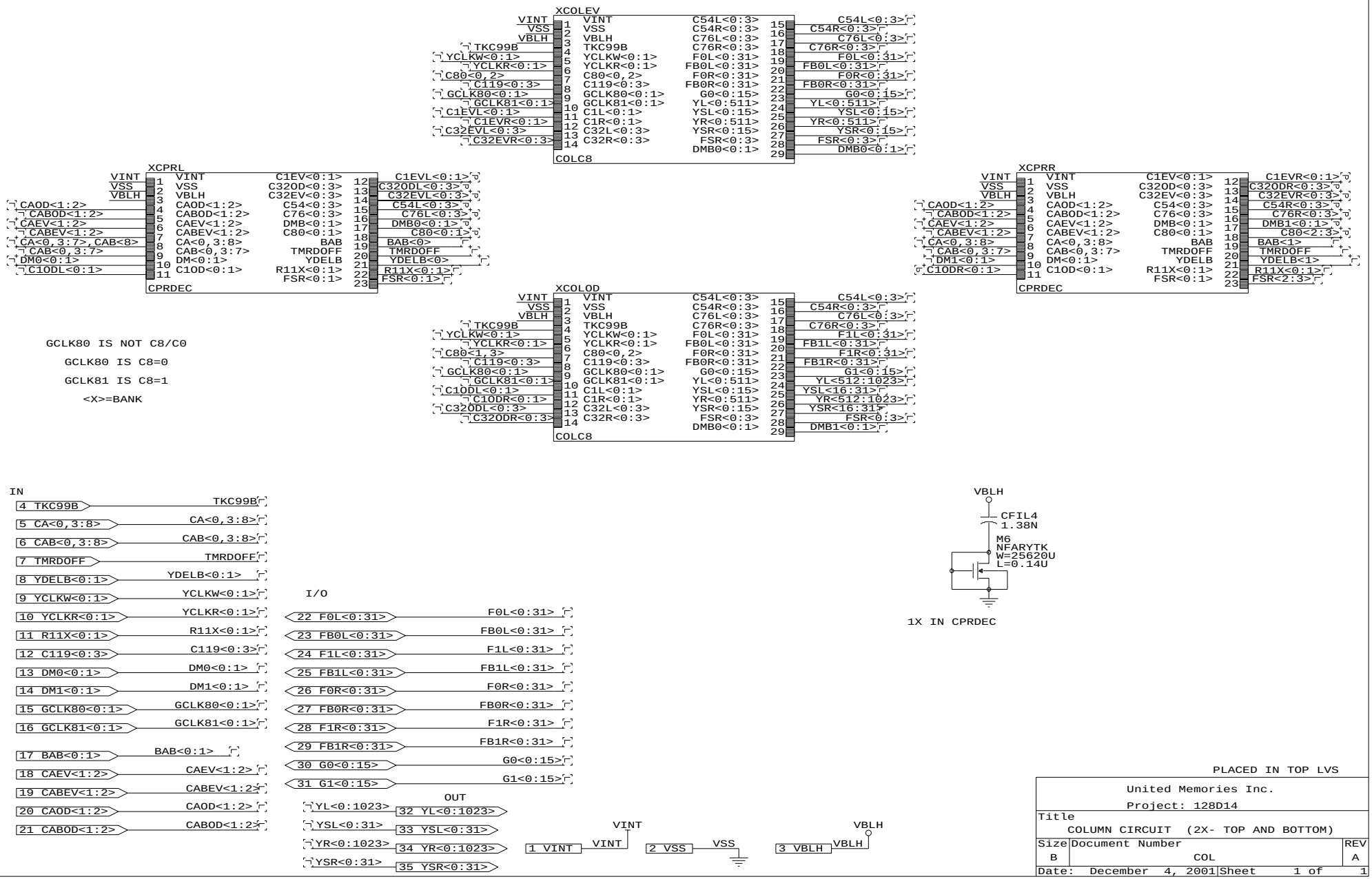


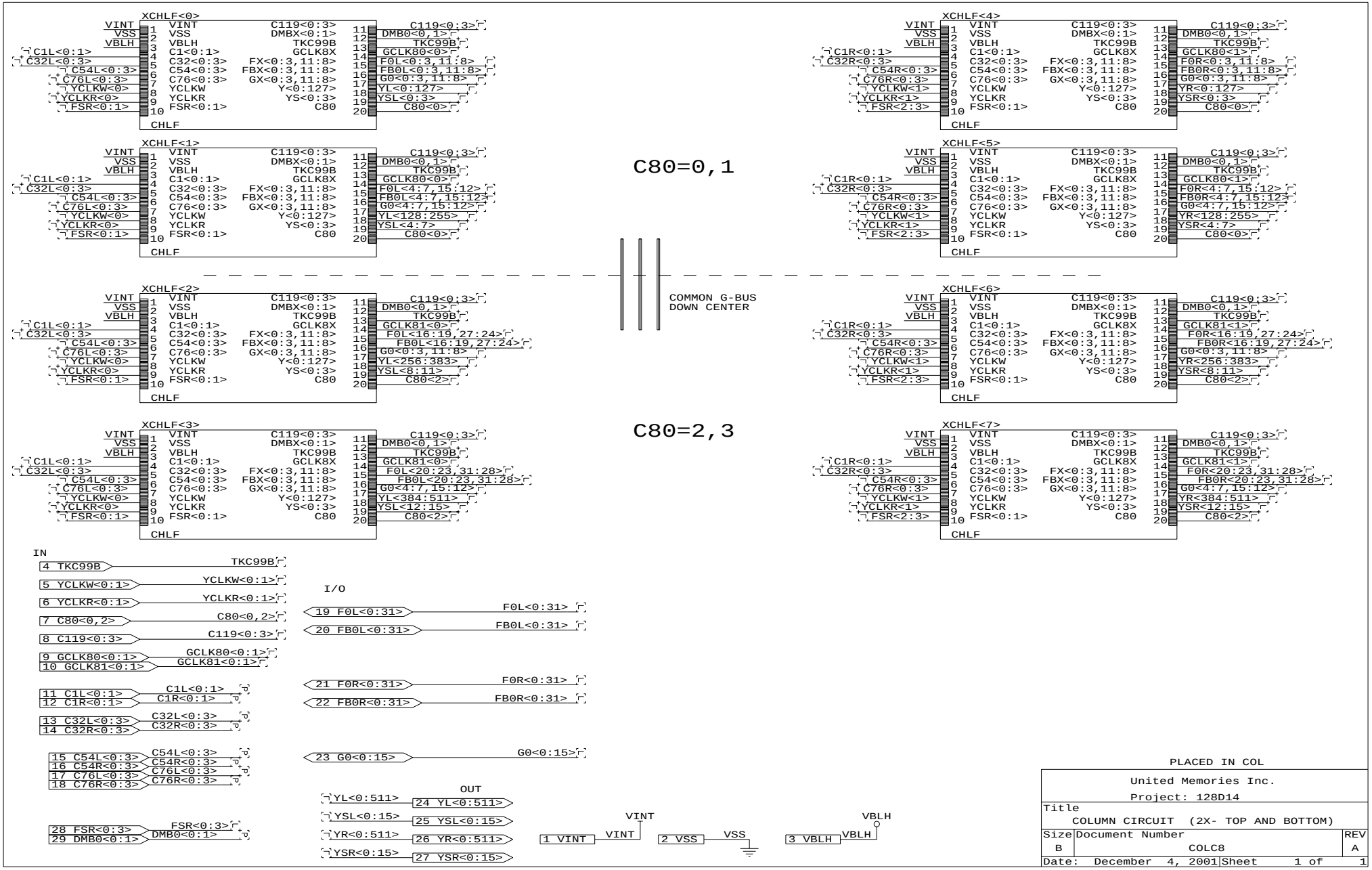
United Memories Inc.		
PROJECT: 128D14		
Title	DATA INPUT BUFFER - SSTL	
Size B	Document Number DINBUF	REV A
Date: October 17, 2001	Sheet 1 of 1	

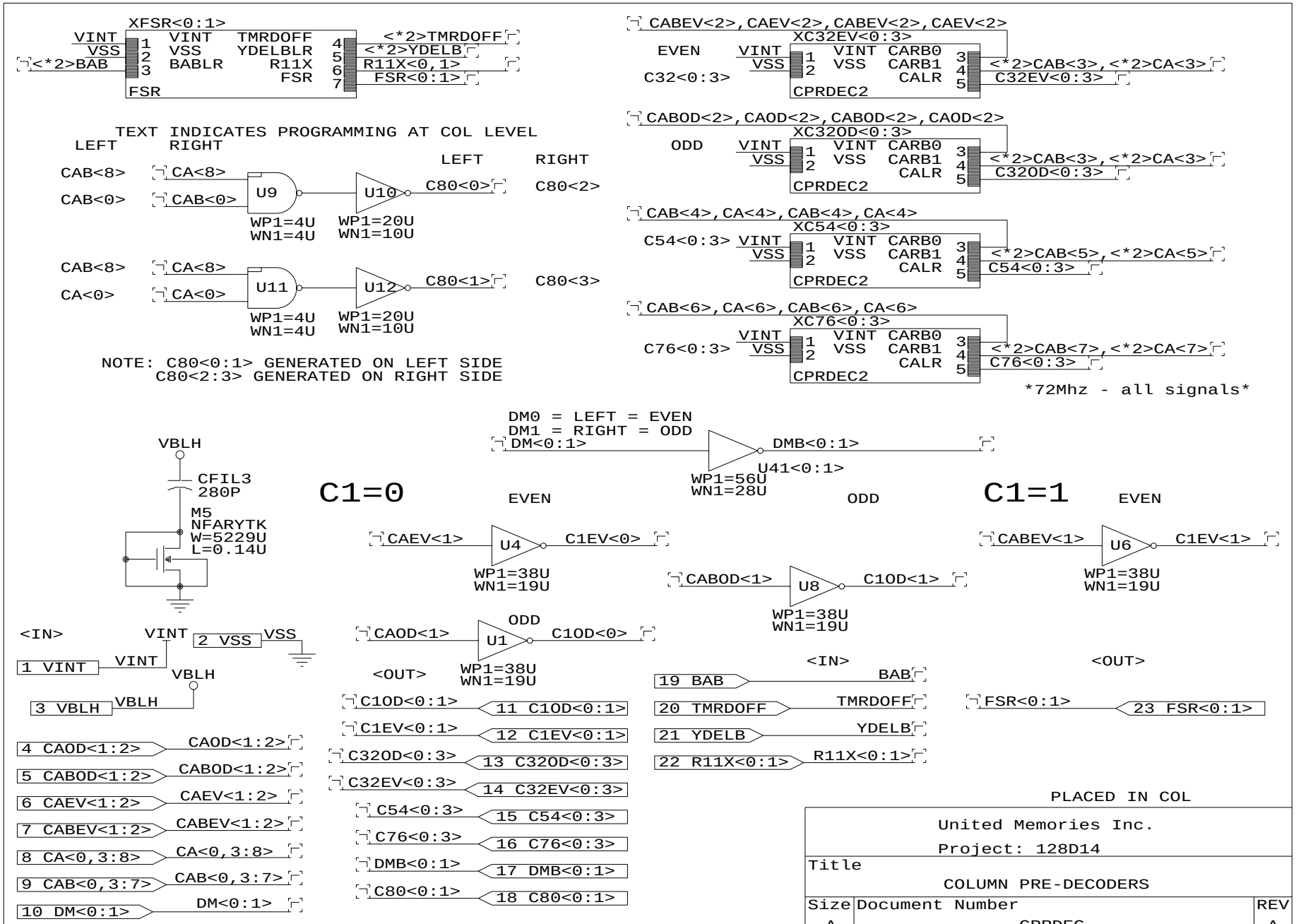

4 DQS
DQS
WP1=0.64U
WN1=1.2U
U19
DQSBR
FAST LOW
NF
M25
W=1U
W=2U
M26
PF
U8
WP1=2U
WN1=1U
U10
WP1=4U
WN1=2U
RD1
NF
M28
W=1U
W=2U
M27
PF
WP1=0.5U
LP1=0.5U
U17
WN1=0.5U
LN1=1U
LRD1
CPAR1
4F
RISING EDGE PATH
3 DIN
U6
WP1=1U
WN1=0.8U
DINCLK
U9
WP1=2U
WN1=1U
U11
WP1=4U
WN1=2U
RD2
LRD2
0V
WP1=0.5U
LP1=0.5U
U18
WN1=0.5U
LN1=1U
7 SDRVCC
U33
WP1=2U
WN1=1U
U29
WP1=4U
WN1=6U
U30
WP1=6U
WN1=1U
VINT
M2
W=30U
PF
M1
W=15U
NF
DDR: READ/WRITE LINE
SDR: READ LINE
72Mhz
IRX
0V
8 IRX
U14
WP1=1U
WN1=1U
WP1=0.5U
LP1=0.5U
U21
WN1=0.5U
LN1=1U
NF
M18
W=2U
W=2U
M17
PF
WP1=2U
WN1=0.64U
U20
FAST RISING
DQSBF
LFD1
0V
U7
WP1=2U
WN1=1U
U12
WP1=4U
WN1=2U
FD1
WP1=0.5U
LP1=0.5U
U23
WN1=0.5U
LN1=1U
CPAR2
5F
FALLING EDGE PATH
U27
WP1=4U
WN1=2U
DQSB
U28
WP1=6U
WN1=1.5U
5 DQSEN
U24
WP1=1U
WN1=1U
6 TMCOMP
U15
WP1=1U
WN1=1U
VINT
U31
WP1=4U
WN1=6U
U32
WP1=6U
WN1=1U
M8
W=30U
PF
M7
W=15U
NF
DDR: READ/WRITE LINE
SDR: WRITE LINE
IFX
0V
72Mhz
9 IFX
U13
WP1=1U
WN1=1U
WP1=0.5U
LP1=0.5U
U22
WN1=0.5U
LN1=1U
PLACED IN CONBLK/DQSCON UDM/LDM (2X)
PLACED IN IOBLK/QBLK (16X)
1 VINT
VINT
2 VSS
VSS
United Memories Inc.
Project: 128D14
Title
FLIP FLOP USED FOR LATCHING INPUT DATA
Size
B
Document Number
DINFF
REV
A
Date: October 17, 2001
Sheet 1 of 1

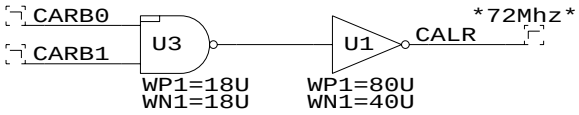

VINT
VINT
4 OTR
M26
W=4U
PF
M25
W=4U
PF
OTRB
OTR2
U3
WP1=4U
WN1=2U
M27
NF
W=4U
M28
NF
W=15U
11 TMOUT
12 TKOUT
M29
NF
W=3U
U6
WP1=2U
WN1=1U
M30
PF
W=6U
TKOUT=
REGPLSB
OR
FID
DEPENDING UPON ??
M31
NF
W=3U
U7
WP1=12U
WN1=6U
M32
PF
W=6U
10 PHIZ
IRB
M13
NF
W=6U
U1
WP1=12U
WN1=6U
M14
PF
W=12U
PUG
M9
W=3U
NF
M8
W=3U
NF
M7
W=3U
NF
CPAR1
20F
M15
NF
W=6U
M16
PF
W=12U
XOUTDRV
VINT
VSS
VCCQ
VSSQ
PUG
1
2
3
4
5
VINT
VSS
VCCQ
VSSQ
PUG
PDG
FSDRV
FSDRVB
DOUT
DPD
6
7
8
9
10
PDG
FSDRV
FSDRVB
DOUT
DPD
OUTDRV
M17
NF
W=3U
5 IR
FOR READS, IR BUS
IS OPPOSITE!
M18
PF
W=6U
PDG
M10
W=3U
NF
M11
W=3U
NF
M12
W=3U
NF
CPAR2
22F
M19
NF
W=3U
6 IF
U2
WP1=12U
WN1=6U
M20
PF
W=6U
VINT
7 EN
U5
WP1=2U
WN1=1U
M24
W=18U
PF
M23
W=6U
PF
OTFB
U4
WP1=4U
WN1=4U
OTF2
9 OTF
M22
W=2U
NF
M21
NF
W=2U
IR BUS HAS OPPOSITE DATA FOR READS !
KEEP FANOUT OF OTR=OTF
DPD
8 DPD
DOUT
13 DOUT
FSDRV
14 FSDRV
FSDRVB
15 FSDRVB
VINT
1 VINT
VINT
2 VSS
VSS
3 VCCQ
VCCQ
16 VSSQ
VSSQ
PLACED IN IOBLK
PLACED IN QBLK
United Memories Inc.
PROJECT: 128D14
Title
DATA OUTPUT BUFFER
Size
B
Document Number
OUTBUF
REV
A
Date: October 29, 2001
Sheet 1 of 1


1 VINT
VINT
2 VSS
VSS
3 VCCQ
VCCQ
7 FSDRV
FSDRV
M5
PFLOTK
W=10U
L=0.3U
M3
NFTK
W=7U
L=0.22U
M4
PFLOTK
W=15U
L=0.3U
FSDRVB
8 FSDRVB
PUGB4
GC TO L=0.36U
C0-GC SPACE=0.2UM
M31
PFLOTK
W=2U
L=0.3U
PUGB
M32
PFLOTK
W=7U
L=0.26U
PUG2
M58
PFLOTK
W=10U
L=0.26U
PUGB2
M1
M62
PFLOTK
W=180U
L=0.32U
M52
PFLOTK
W=270U
L=0.32U
M2A1
PFLOTK
W=90U
L=0.32U
M2A2
PFLOTK
W=90U
L=0.32U
M2A2 FOR LPSDR MARGIN
M57
NFTK
W=7U
L=0.22U
M56
NFTK
W=7U
L=0.22U
VSSQ
M40
NFTK
W=8U
L=0.22U
M33
NFTK
W=24U
L=0.22U
M41
W=5U
L=0.22U
NFTK
U6
WP1=6U
WN1=3U
M34
NFTK
W=15U
L=0.22U
5 PUG
M6
NFTK
W=0.5U
L=1U
RG1
5
TUNABLE
2.5>>10 OHMS
(M1)
M59
PFLOTK
W=24U
L=0.26U
PUGB3
9 DOUT
RN1
6
TUNABLE
6.6,8,10,13.3
(M1)
M60
NFTK
W=7U
L=0.22U
M61
NFTK
W=7U
L=0.22U
M71
PFLOTK
W=2U
L=0.5U
10 DPD
VCCX LEVEL
M72
NFTK
W=1U
L=1U
M73
NFTK
W=1U
L=1U
M64
W=100U
L=0.22U
NFTK
M30
W=200U
L=0.22U
NFTK
M29
W=54U
L=0.22U
NFTK
C0-GC SPACE=0.2U
M63
W=120U
L=0.3U
NFTK
M50
W=260U
L=0.3U
NFTK
M3A1
W=72U
L=0.3U
NFTK
GC TO L=0.34U
4 VSSQ
M37
PFLOTK
W=1U
L=0.3U
M51
PFLOTK
W=2U
L=0.26U
PDG2
M74
NFTK
W=1U
L=1U
M42
NFTK
W=8U
L=0.22U
M38
NFTK
W=24U
L=0.22U
M39
NFTK
W=12U
L=0.22U
6 PDG
NFTK
W=4U
L=0.22U
M43
U7
WP1=2U
WN1=1U
M35
NFTK
W=0.5U
L=1U
DPDB
M65
PFLOTK
W=1U
L=0.3U
M68
PFLOTK
W=7U
L=0.26U
M66
NFTK
W=8U
L=0.22U
M69
NFTK
W=48U
L=0.22U
M67
NFTK
L=0.22U
W=4U
U8
WP1=4U
WN1=2U
M70
NFTK
W=30U
L=0.22U
PDG3
M75
NFTK
W=1U
L=1U
M1
NFTK
W=7U
L=0.22U
PDG4
M36
PFLOTK
W=15U
L=0.3U
M2
NFTK
W=6U
L=0.22U
PLACED IN IOBLK
PLACED IN QBLK
PLACED IN OUTBUF
ALSO PLACED IN DQSBUF
United Memories Inc.
PROJECT: 128D14
Title
DATA OUTPUT DRIVER
Size B
Document Number
OUTDRV
REV A
Date: December 4, 2001
Sheet 1 of 1

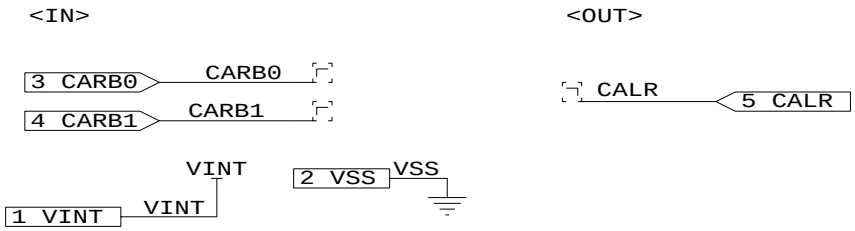

XCOLEV
COLC8
XCPRL
CPRDEC
XCPRR
CPRDEC
XCOLOD
COLC8
GCLK80 IS NOT C8/C0
GCLK80 IS C8=0
GCLK81 IS C8=1
<X>=BANK
IN
I/O
OUT
VBLH
CFIL4
1.38N
M6
NFARYTK
W=25620U
L=0.14U
1X IN CPRDEC
VINT
VSS
VBLH
PLACED IN TOP LVS
United Memories Inc.
Project: 128D14
Title
COLUMN CIRCUIT (2X- TOP AND BOTTOM)
Size B
Document Number
COL
REV A
Date: December 4, 2001
Sheet 1 of 1


XCHLF<0>
XCHLF<1>
XCHLF<2>
XCHLF<3>
XCHLF<4>
XCHLF<5>
XCHLF<6>
XCHLF<7>
CHLF
VINT
VSS
VBLH
C1L<0:1>
C32L<0:3>
C54L<0:3>
C76L<0:3>
YCLKW<0>
YCLKR<0>
FSR<0:1>
C1<0:1>
C32<0:3>
C54<0:3>
C76<0:3>
YCLKW
YCLKR
FSR<0:1>
C119<0:3>
DMBX<0:1>
TKC99B
GCLK8X
FX<0:3,11:8>
FBX<0:3,11:8>
GX<0:3,11:8>
Y<0:127>
YS<0:3>
C80
DMB0<0,1>
GCLK80<0>
F0L<0:3,11:8>
FB0L<0:3,11:8>
G0<0:3,11:8>
YL<0:127>
YSL<0:3>
C80<0>
F0L<4:7,15:12>
FB0L<4:7,15:12>
G0<4:7,15:12>
YL<128:255>
YSL<4:7>
GCLK81<0>
F0L<16:19,27:24>
FB0L<16:19,27:24>
YL<256:383>
YSL<8:11>
C80<2>
F0L<20:23,31:28>
FB0L<20:23,31:28>
YL<384:511>
YSL<12:15>
C1R<0:1>
C32R<0:3>
C54R<0:3>
C76R<0:3>
YCLKW<1>
YCLKR<1>
FSR<2:3>
GCLK80<1>
F0R<0:3,11:8>
FB0R<0:3,11:8>
G0<0:3,11:8>
YR<0:127>
YSR<0:3>
F0R<4:7,15:12>
FB0R<4:7,15:12>
G0<4:7,15:12>
YR<128:255>
YSR<4:7>
GCLK81<1>
F0R<16:19,27:24>
FB0R<16:19,27:24>
YR<256:383>
YSR<8:11>
F0R<20:23,31:28>
FB0R<20:23,31:28>
YR<384:511>
YSR<12:15>
C80=0,1
C80=2,3
COMMON G-BUS
DOWN CENTER
IN
4 TKC99B
5 YCLKW<0:1>
6 YCLKR<0:1>
7 C80<0,2>
8 C119<0:3>
9 GCLK80<0:1>
10 GCLK81<0:1>
11 C1L<0:1>
12 C1R<0:1>
13 C32L<0:3>
14 C32R<0:3>
15 C54L<0:3>
16 C54R<0:3>
17 C76L<0:3>
18 C76R<0:3>
28 FSR<0:3>
29 DMB0<0:1>
I/O
19 F0L<0:31>
20 FB0L<0:31>
21 F0R<0:31>
22 FB0R<0:31>
23 G0<0:15>
OUT
24 YL<0:511>
25 YSL<0:15>
26 YR<0:511>
27 YSR<0:15>
1 VINT
2 VSS
3 VBLH
PLACED IN COL
United Memories Inc.
Project: 128D14
Title
COLUMN CIRCUIT (2X- TOP AND BOTTOM)
Size B
Document Number
COLC8
REV A
Date: December 4, 2001
Sheet 1 of 1


XFSR<0:1>
VINT
VSS
<*2>BAB
FSR
VINT
VSS
BABLR
TMRDOFF
YDELBLR
R11X
FSR
<*2>TMRDOFF
<*2>YDELB
R11X<0,1>
FSR<0:1>
TEXT INDICATES PROGRAMMING AT COL LEVEL
LEFT RIGHT
CAB<8>
CAB<0>
CA<8>
CAB<0>
U9
U10
WP1=4U
WN1=4U
WP1=20U
WN1=10U
LEFT RIGHT
C80<0>
C80<2>
CAB<8>
CA<0>
CA<8>
CA<0>
U11
U12
WP1=4U
WN1=4U
WP1=20U
WN1=10U
C80<1>
C80<3>
NOTE: C80<0:1> GENERATED ON LEFT SIDE
C80<2:3> GENERATED ON RIGHT SIDE
CABEV<2>,CAEV<2>,CABEV<2>,CAEV<2>
XC32EV<0:3>
EVEN
C32<0:3>
VINT
VSS
CARB0
CARB1
CALR
CPRDEC2
<*2>CAB<3>,<*2>CA<3>
C32EV<0:3>
CABOD<2>,CAOD<2>,CABOD<2>,CAOD<2>
XC32OD<0:3>
ODD
C32OD<0:3>
CAB<4>,CA<4>,CAB<4>,CA<4>
XC54<0:3>
C54<0:3>
<*2>CAB<5>,<*2>CA<5>
C54<0:3>
CAB<6>,CA<6>,CAB<6>,CA<6>
XC76<0:3>
C76<0:3>
<*2>CAB<7>,<*2>CA<7>
C76<0:3>
72Mhz - all signals
DM0 = LEFT = EVEN
DM1 = RIGHT = ODD
DM<0:1>
DMB<0:1>
U41<0:1>
WP1=56U
WN1=28U
VBLH
CFIL3
280P
M5
NFARYTK
W=5229U
L=0.14U
C1=0
EVEN
CAEV<1>
U4
C1EV<0>
WP1=38U
WN1=19U
ODD
CAOD<1>
U1
C1OD<0>
WP1=38U
WN1=19U
C1=1
EVEN
CABEV<1>
U6
C1EV<1>
WP1=38U
WN1=19U
CABOD<1>
U8
C1OD<1>
WP1=38U
WN1=19U
<IN>
VINT
2 VSS
VSS
1 VINT
VINT
VBLH
3 VBLH
VBLH
4 CAOD<1:2>
CAOD<1:2>
5 CABOD<1:2>
CABOD<1:2>
6 CAEV<1:2>
CAEV<1:2>
7 CABEV<1:2>
CABEV<1:2>
8 CA<0,3:8>
CA<0,3:8>
9 CAB<0,3:7>
CAB<0,3:7>
10 DM<0:1>
DM<0:1>
<OUT>
C1OD<0:1>
11 C1OD<0:1>
C1EV<0:1>
12 C1EV<0:1>
C32OD<0:3>
13 C32OD<0:3>
C32EV<0:3>
14 C32EV<0:3>
C54<0:3>
15 C54<0:3>
C76<0:3>
16 C76<0:3>
DMB<0:1>
17 DMB<0:1>
C80<0:1>
18 C80<0:1>
<IN>
19 BAB
BAB
20 TMRDOFF
TMRDOFF
21 YDELB
YDELB
22 R11X<0:1>
R11X<0:1>
<OUT>
FSR<0:1>
23 FSR<0:1>
PLACED IN COL
United Memories Inc.
Project: 128D14
Title
COLUMN PRE-DECODERS
Size
A
Document Number
CPRDEC
REV
A
Date: November 21, 2001
Sheet 1 of 1



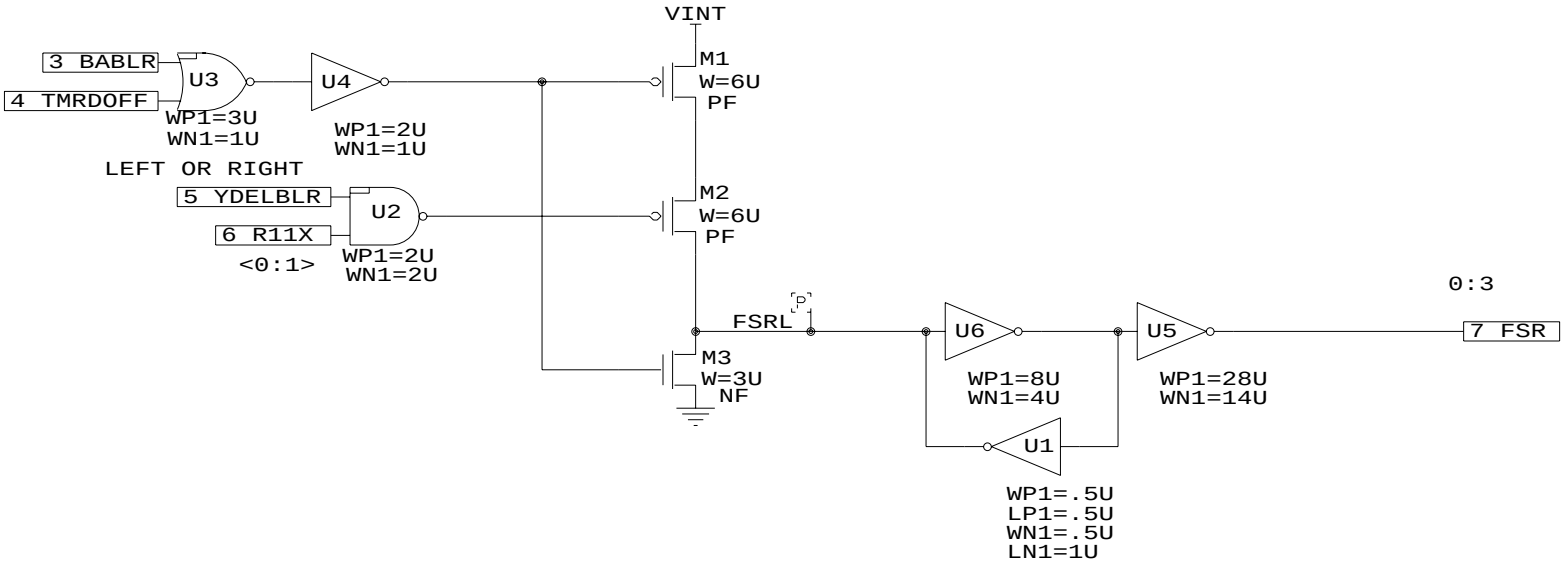
CARB - Column Address or Bar
CAL - Column Address Left OR RIGHT

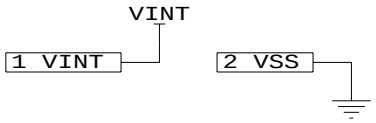


PLACED IN COL
PLACED IN CPRDEC

United Memories Inc. Project: 128D14		
Title COLUMN PRE-DECODER LOGIC		
Size A	Document Number CPRDEC2	REV A
Date: August 24, 2001	Sheet 1 of 1	

	BAB	YDELB	R11	FSR
LEFT BANK (0 OR 2)	0	0	0	0
	0	0	1	1
RIGHT BANK (1 OR 3)	1	1	0	2
	1	1	1	3





UNITED MEMORIES INC.

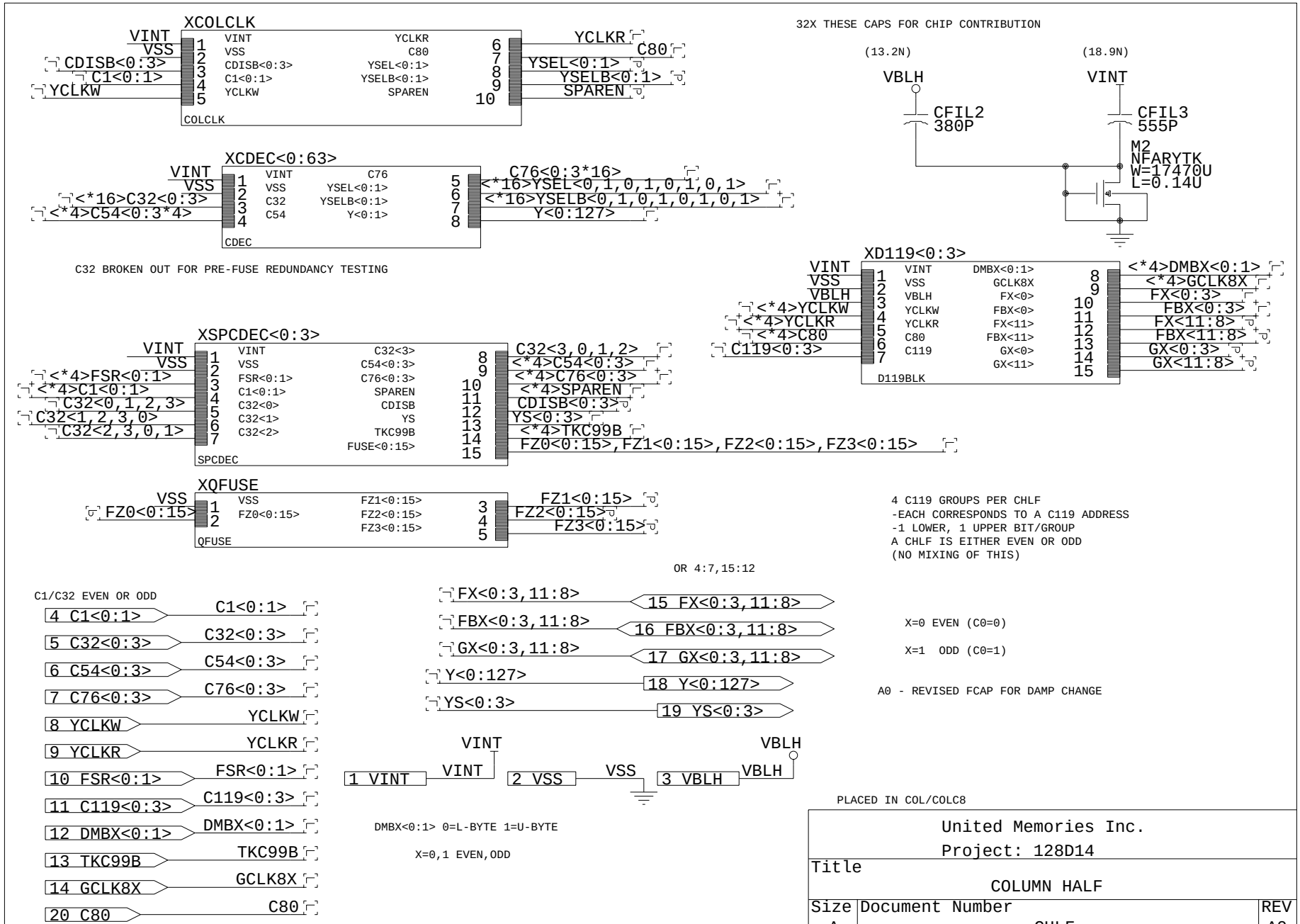
PROJECT: 128D14

Title

R11 FUSE SELECT FOR COLUMNS

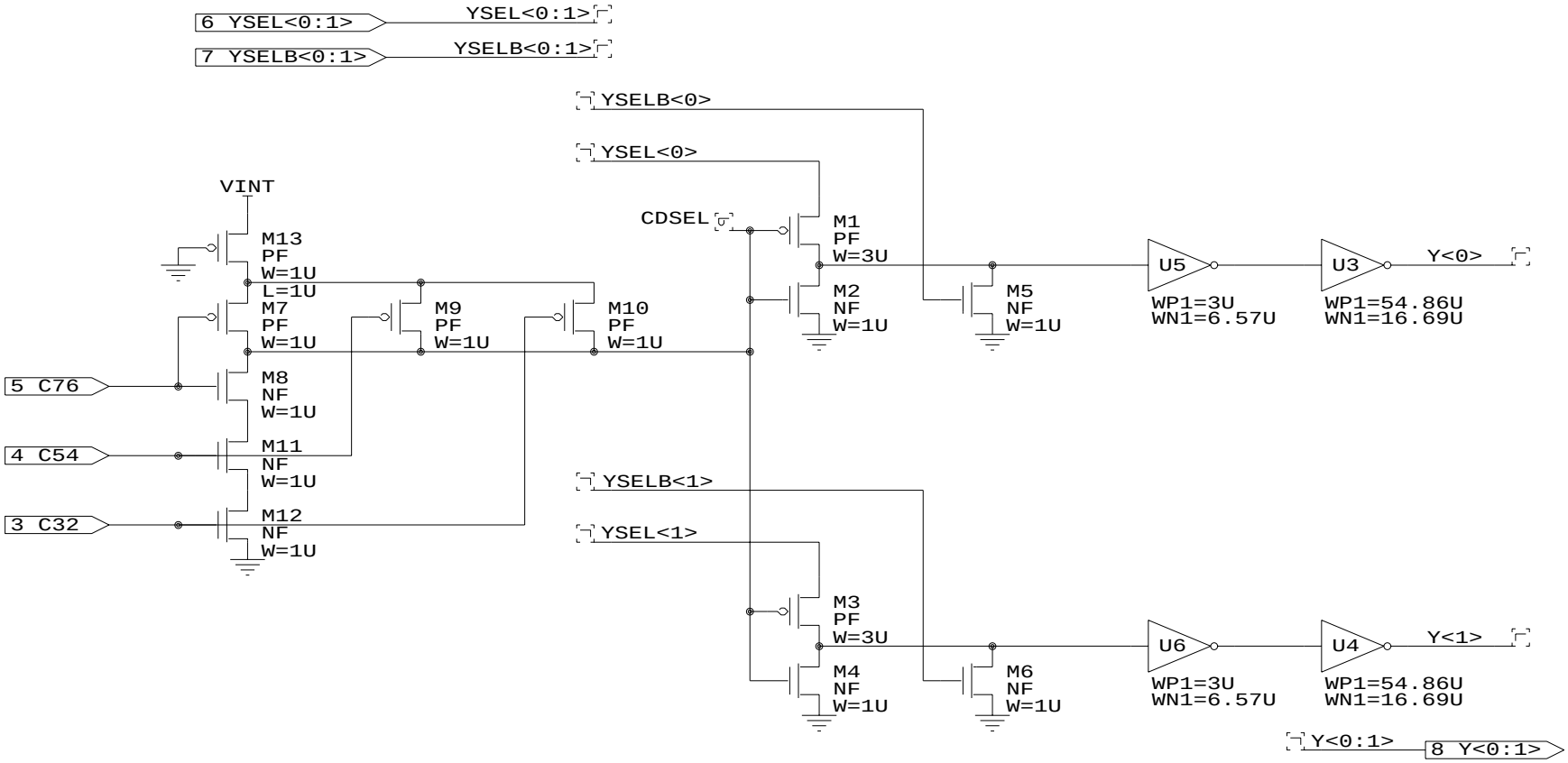
Size	Document Number	REV
A	FSR	A

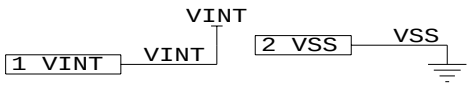
Date: March 24, 2001 Sheet 1 of 1



United Memories Inc.
Project: 128D14

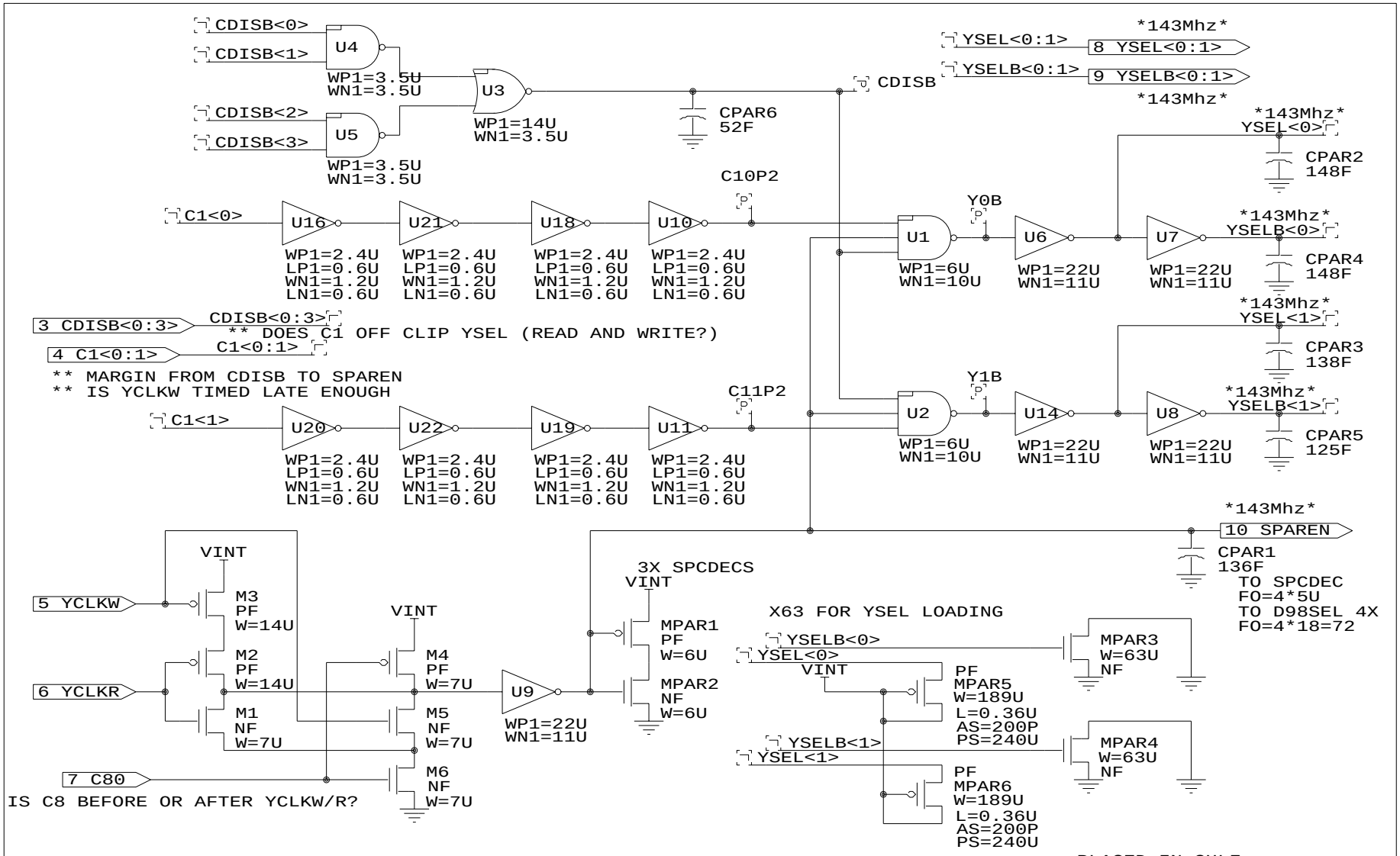
Title		
	COLUMN HALF	
Size A	Document Number CHLF	REV A0
Date: February 4, 2002	Sheet 1 of 1	



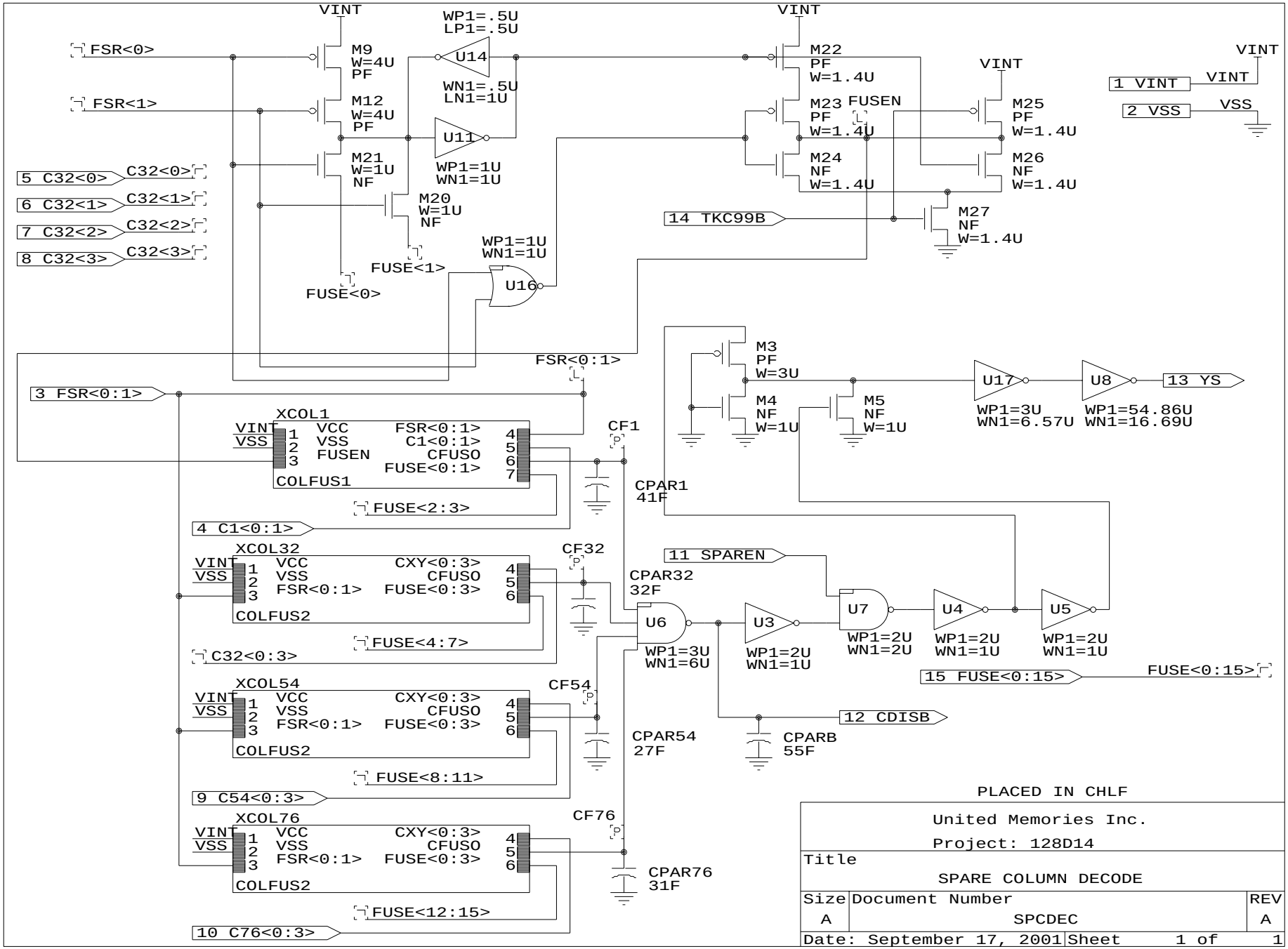


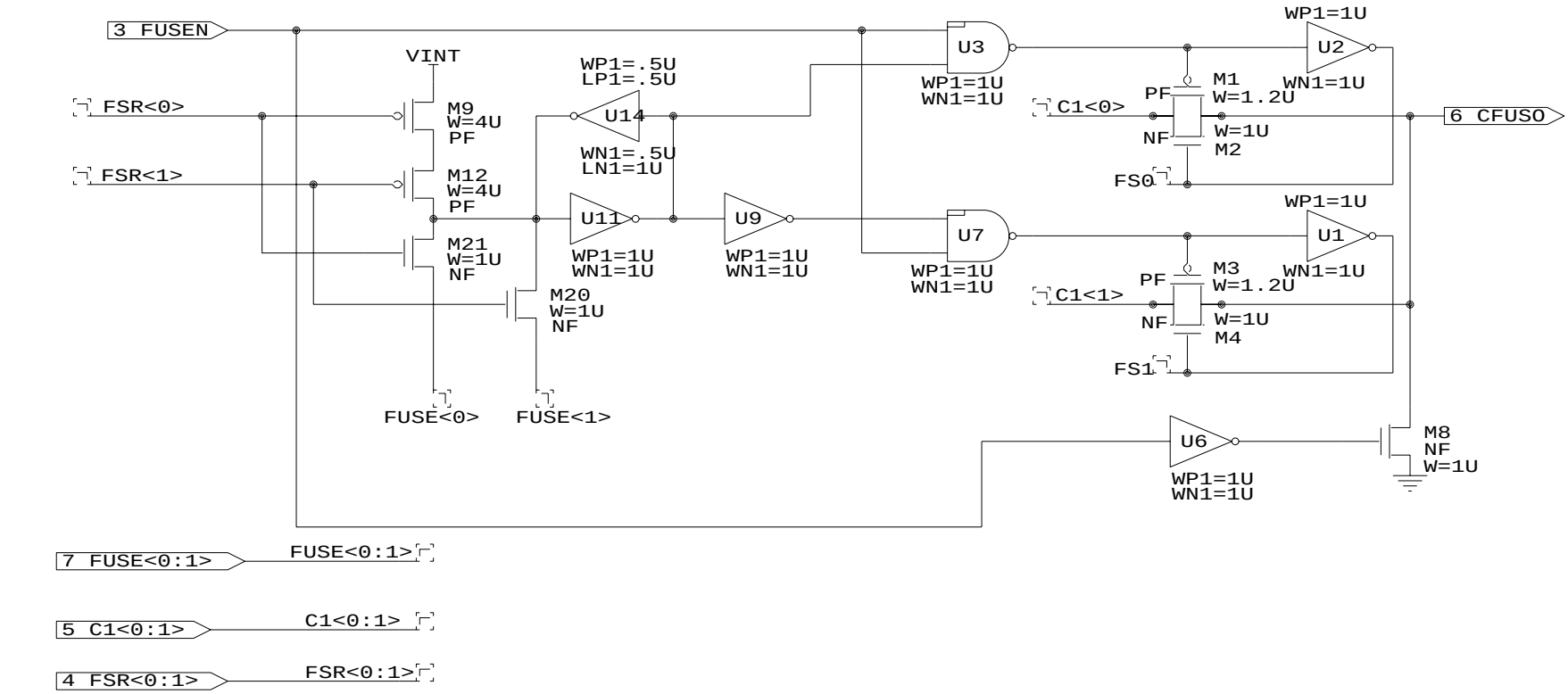
PLACED IN CHLF

United Memories Inc. Project: 128D14		
Title COLUMN DECODE		
Size A	Document Number CDEC	REV A
Date: September 17, 2001	Sheet 1 of 1	

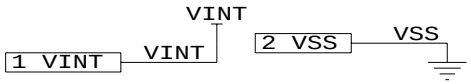


United Memories Inc.		
Project: 128D14		
Title	COLUMN CLOCK CIRCUIT	
Size A	Document Number COLCLK	REV A
Date: September 17, 2001	Sheet 1 of 1	

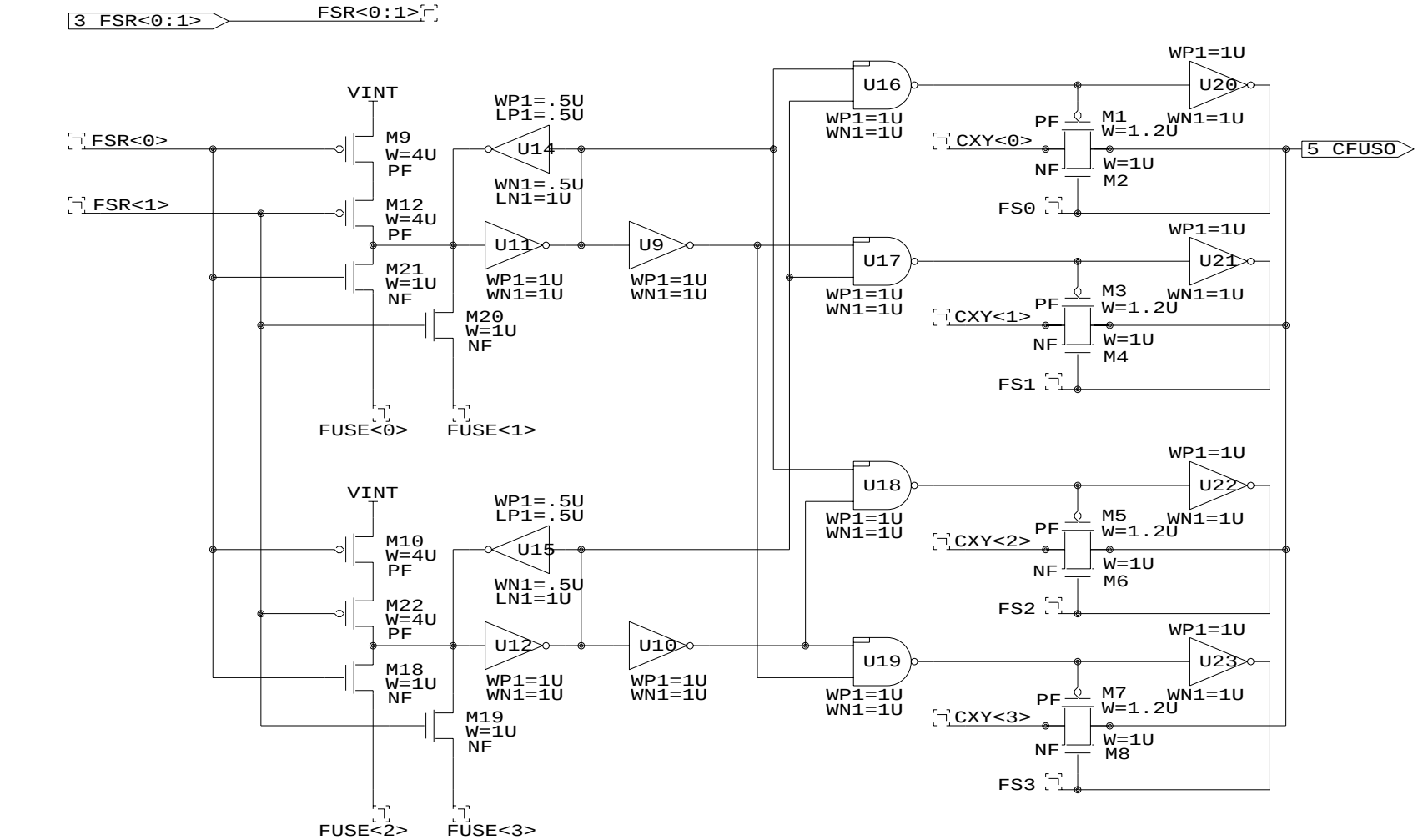

VINT
FSR<0>
FSR<1>
M9
W=4U
PF
M12
W=4U
PF
M21
W=1U
NF
M20
W=1U
NF
WP1=.5U
LP1=.5U
U14
WN1=.5U
LN1=1U
U11
WP1=1U
WN1=1U
5 C32<0>
C32<0>
6 C32<1>
C32<1>
7 C32<2>
C32<2>
8 C32<3>
C32<3>
FUSE<1>
FUSE<0>
WP1=1U
WN1=1U
U16
M22
PF
W=1.4U
M23
PF
W=1.4U
FUSEN
M24
NF
W=1.4U
M25
PF
W=1.4U
M26
NF
W=1.4U
14 TKC99B
M27
NF
W=1.4U
1 VINT
2 VSS
VSS
FSR<0:1>
3 FSR<0:1>
M3
PF
W=3U
M4
NF
W=1U
M5
NF
W=1U
U17
WP1=3U
WN1=6.57U
U8
WP1=54.86U
WN1=16.69U
13 YS
XCOL1
VCC
VSS
FUSEN
FSR<0:1>
C1<0:1>
CFUSO
FUSE<0:1>
COLFUS1
FUSE<2:3>
4 C1<0:1>
CF1
CPAR1
41F
XCOL32
CXY<0:3>
CFUSO
FSR<0:1>
FUSE<0:3>
COLFUS2
FUSE<4:7>
C32<0:3>
CF32
CPAR32
32F
11 SPAREN
U6
WP1=3U
WN1=6U
U3
WP1=2U
WN1=1U
U7
WP1=2U
WN1=2U
U4
WP1=2U
WN1=1U
U5
WP1=2U
WN1=1U
15 FUSE<0:15>
FUSE<0:15>
XCOL54
CF54
CPAR54
27F
12 CDISB
CPARB
55F
FUSE<8:11>
9 C54<0:3>
XCOL76
CF76
CPAR76
31F
FUSE<12:15>
10 C76<0:3>
PLACED IN CHLF
United Memories Inc.
Project: 128D14
Title
SPARE COLUMN DECODE
Size
A
Document Number
SPCDEC
REV
A
Date: September 17, 2001
Sheet 1 of 1



PLACED IN COL
PLACED IN CHLF
PLACED IN SPCDEC



United Memories Inc. Project: 128D14		
Title COLUMN REDUNDANCY FUSE - 1 FUSE		
Size A	Document Number COLFUS1	REV A
Date: March 21, 2001	Sheet 1 of 1	



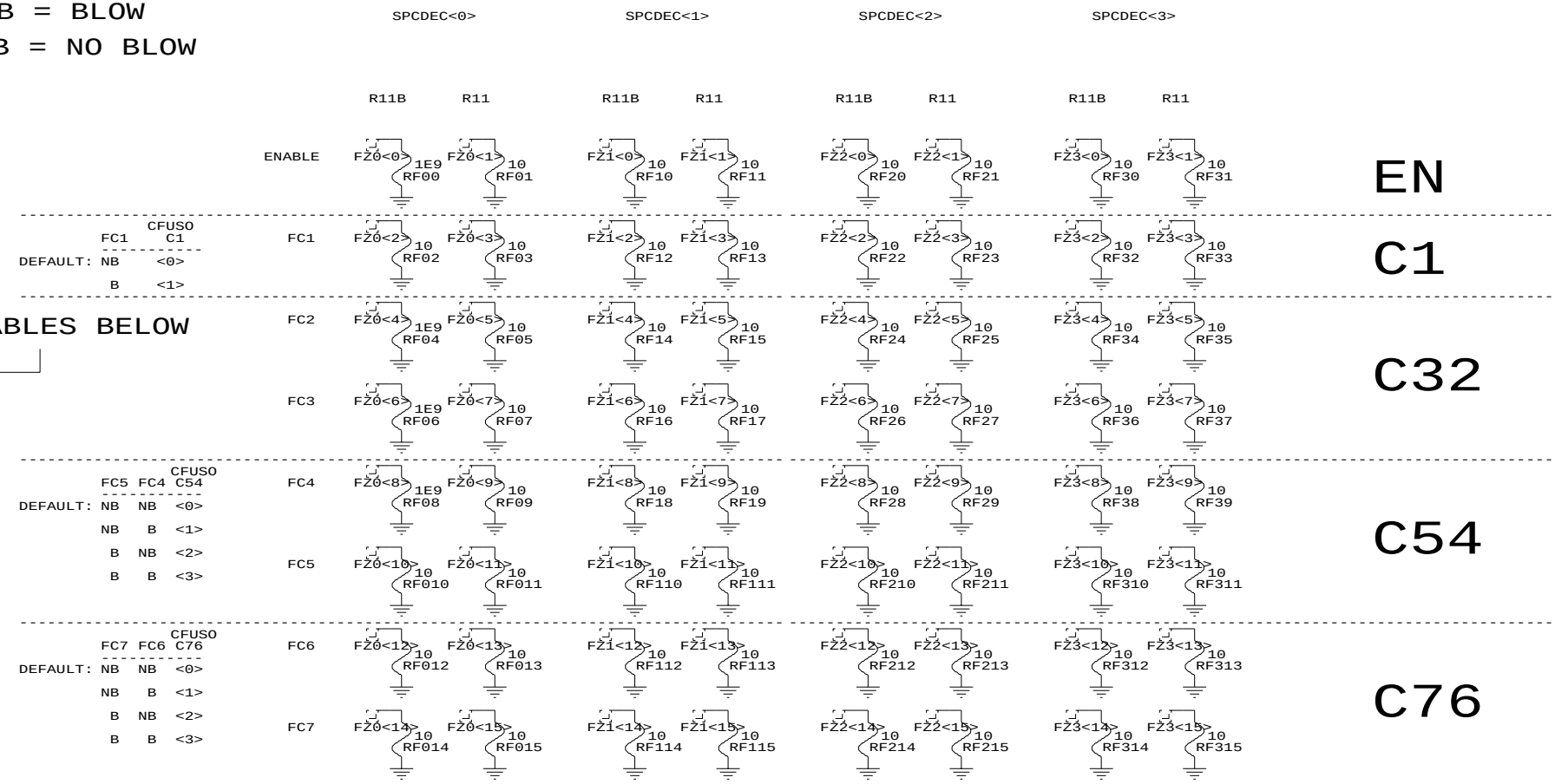
PLACED IN COL
PLACED IN CHLF
PLACED IN SPCDEC

United Memories Inc. Project: 128D14		
Title COLUMN REDUNDANCY FUSE - 2 FUSES		
Size A	Document Number COLFUS2	REV A
Date: March 21, 2001	Sheet 1 of 1	

B = BLOW

NB = NO BLOW

SEE TABLES BELOW



CFUSO

	FC1	C1
DEFAULT:	NB	<0>
	B	<1>

CFUSO

	FC5	FC4	C54
DEFAULT:	NB	NB	<0>
	NB	B	<1>
	B	NB	<2>
	B	B	<3>

CFUSO

	FC7	FC6	C76
DEFAULT:	NB	NB	<0>
	NB	B	<1>
	B	NB	<2>
	B	B	<3>

DEFAULT:C32<0>

CFUSO

FC3	FC2	C32
NB	NB	<0>
NB	B	<1>
B	NB	<2>
B	B	<3>

DEFAULT:C32<1>

CFUSO

FC3	FC2	C32
NB	NB	<1>
NB	B	<2>
B	NB	<3>
B	B	<0>

DEFAULT:C32<2>

CFUSO

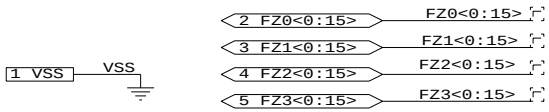
FC3	FC2	C32
NB	NB	<2>
NB	B	<3>
B	NB	<0>
B	B	<1>

DEFAULT:C32<3>

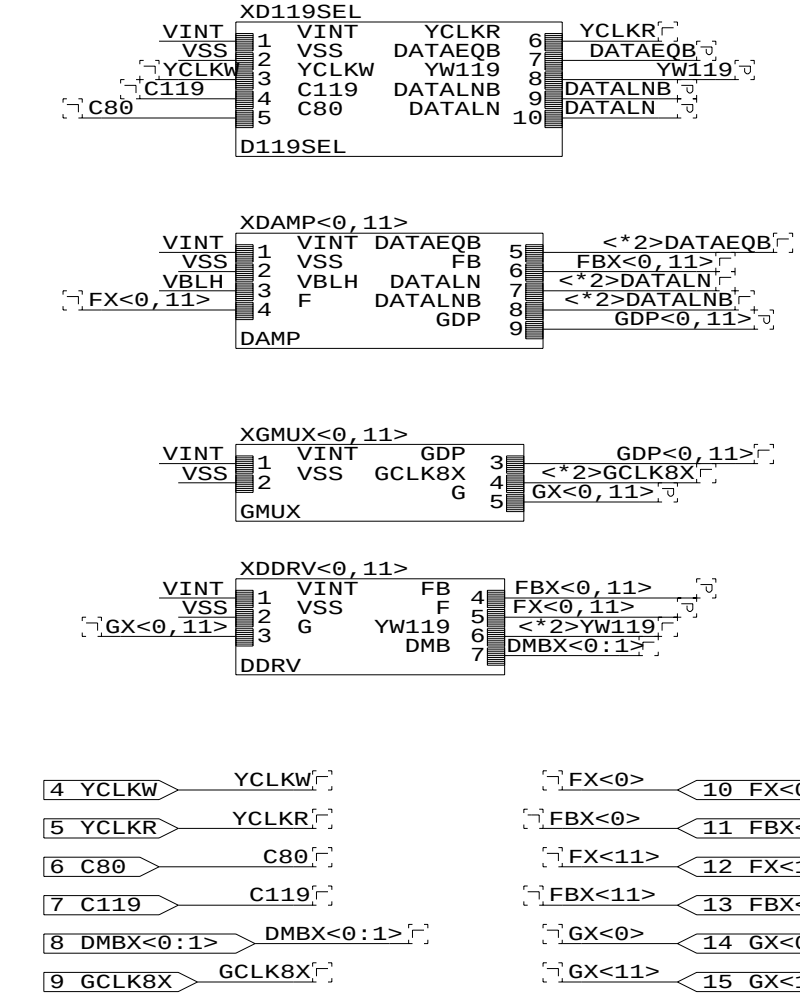
CFUSO

FC3	FC2	C32
NB	NB	<3>
NB	B	<0>
B	NB	<1>
B	B	<2>

PLACED IN CHLF



United Memories Inc.		
Project: 128D14		
Title	COLUMN FUSES PER HQUAD	
Size B	Document Number QFUSE	REV A2
Date: December 4, 2001	Sheet 1 of 1	



TEXTED FOR F0,11 C98=0

OTHER CASES ARE:

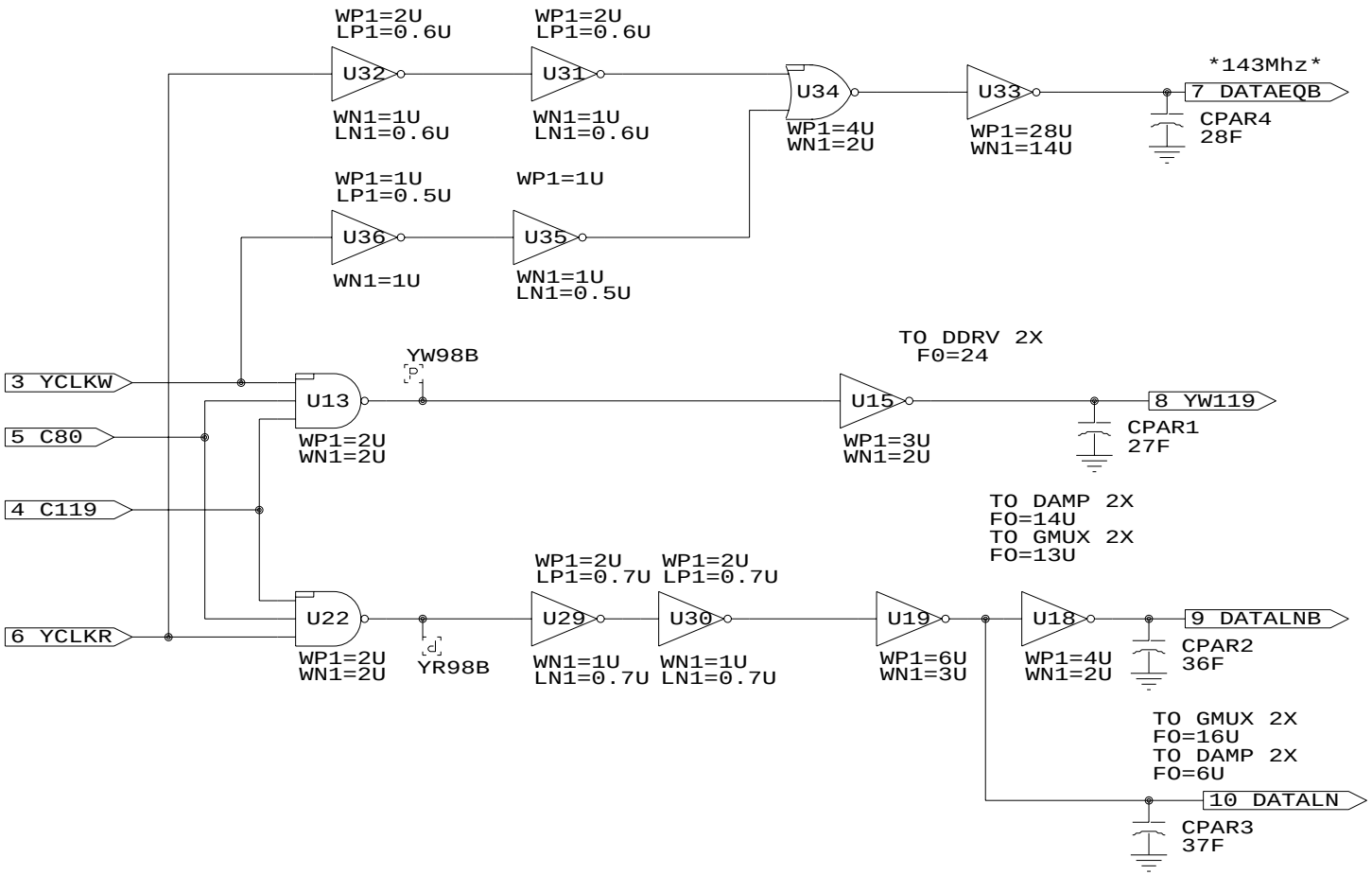
C119	0	1	2	3
F'S	0,11	1,10	2,9	3,8
F'S	4,15	5,14	6,13	7,12

EVERYTHING IS DUPLICATED FOR EVEN/ODD AS WELL

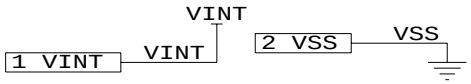
X=0 EVEN (C0=0)
X=1 ODD (C0=1)

PLACED IN COL
PLACED IN CHLF

United Memories Inc. Project: 128D14		
Title DATA PAIR FOR C119		
Size A	Document Number D119BLK	REV A
Date: December 4, 2001	Sheet 1 of 1	

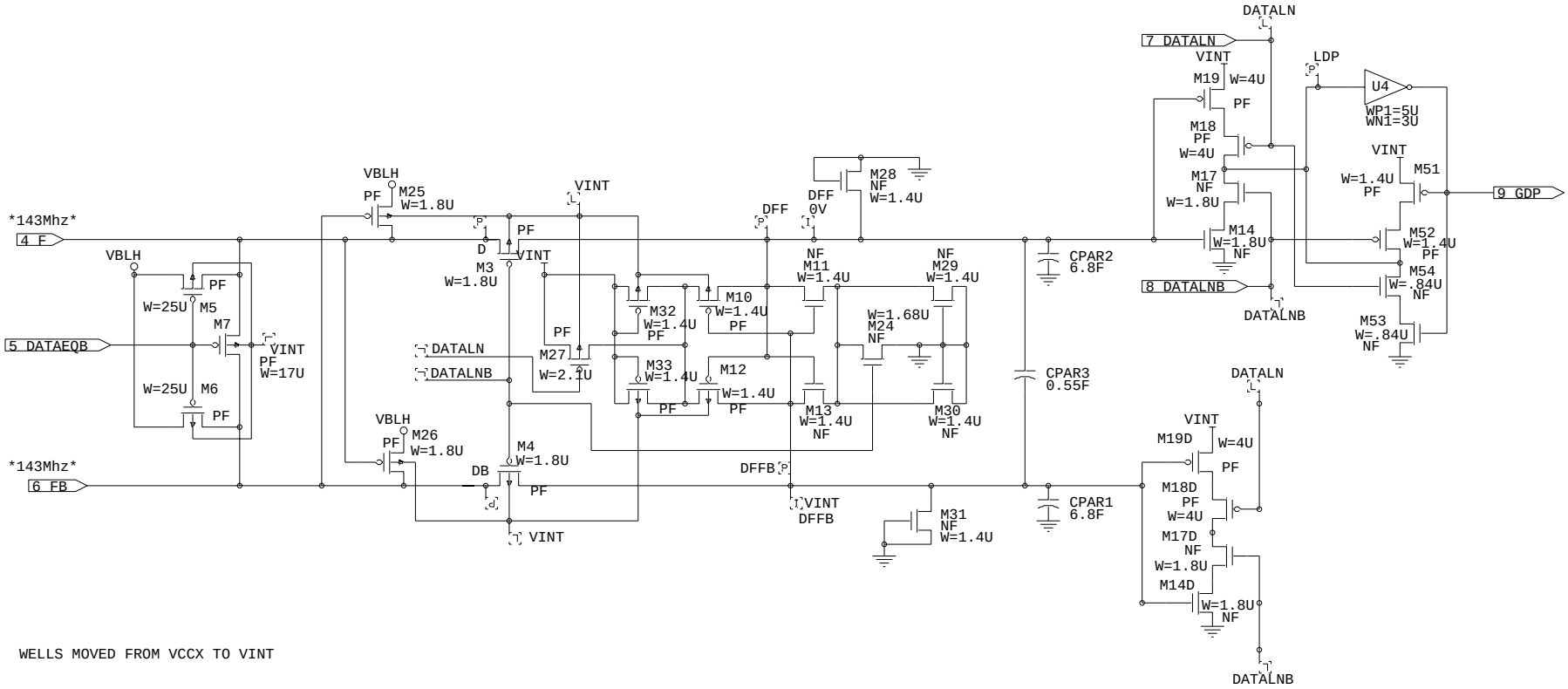


PLACED IN CHLF/D119BLK



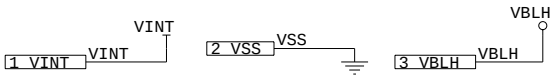
United Memories Inc.		
Project: 128D14		
Title		
DATA PAIR SELECT FOR C119 ADDRESS		
Size	Document Number	REV
A	D119SEL	A
Date: September 17, 2001	Sheet 1 of 1	

TRANSISTORS M28,M31 ARE FOR LAYOUT BALANCING PURPOSES



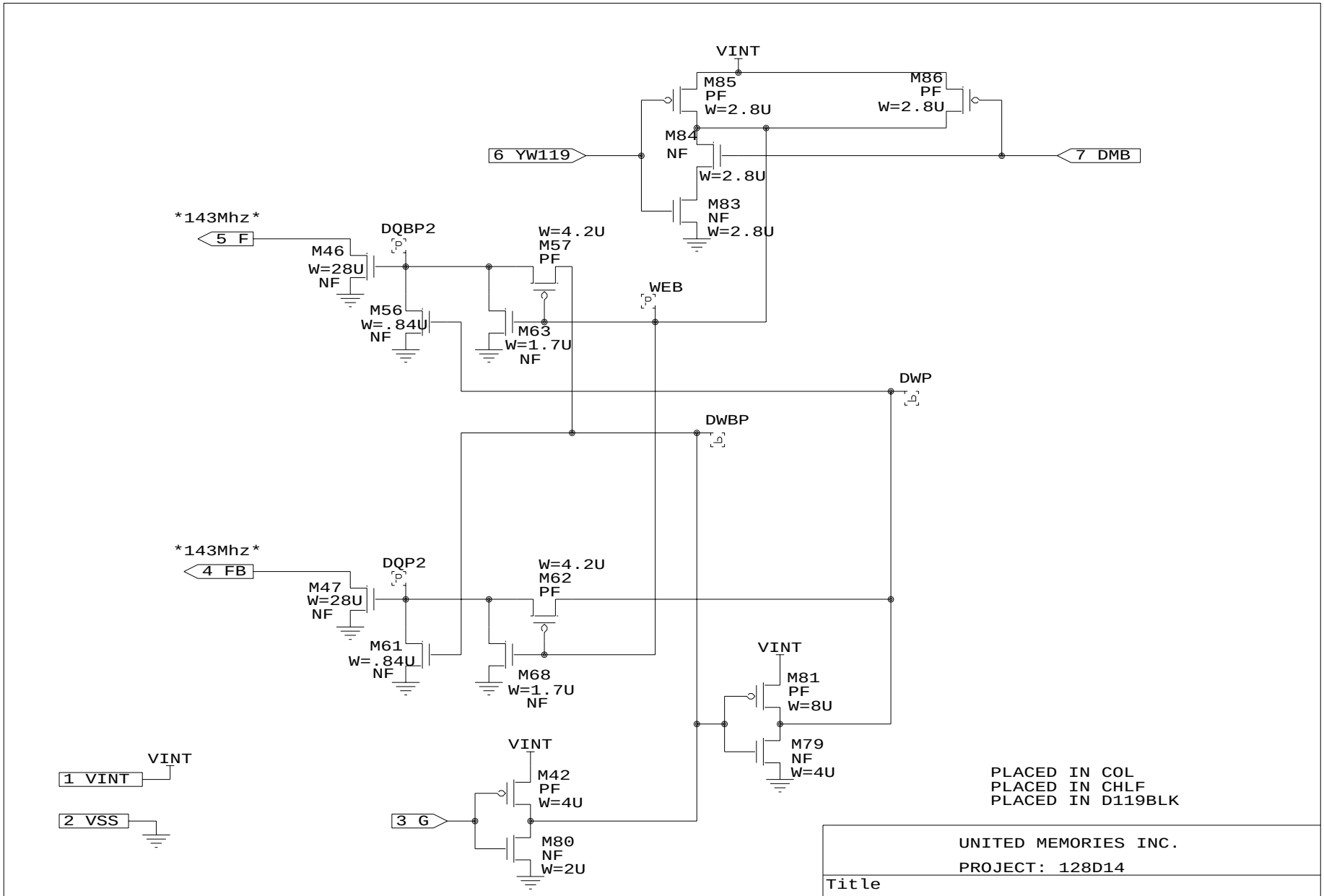
WELLS MOVED FROM VCCX TO VINT

PLACED IN COL
PLACED IN CHLF
PLACE IN D119BLK

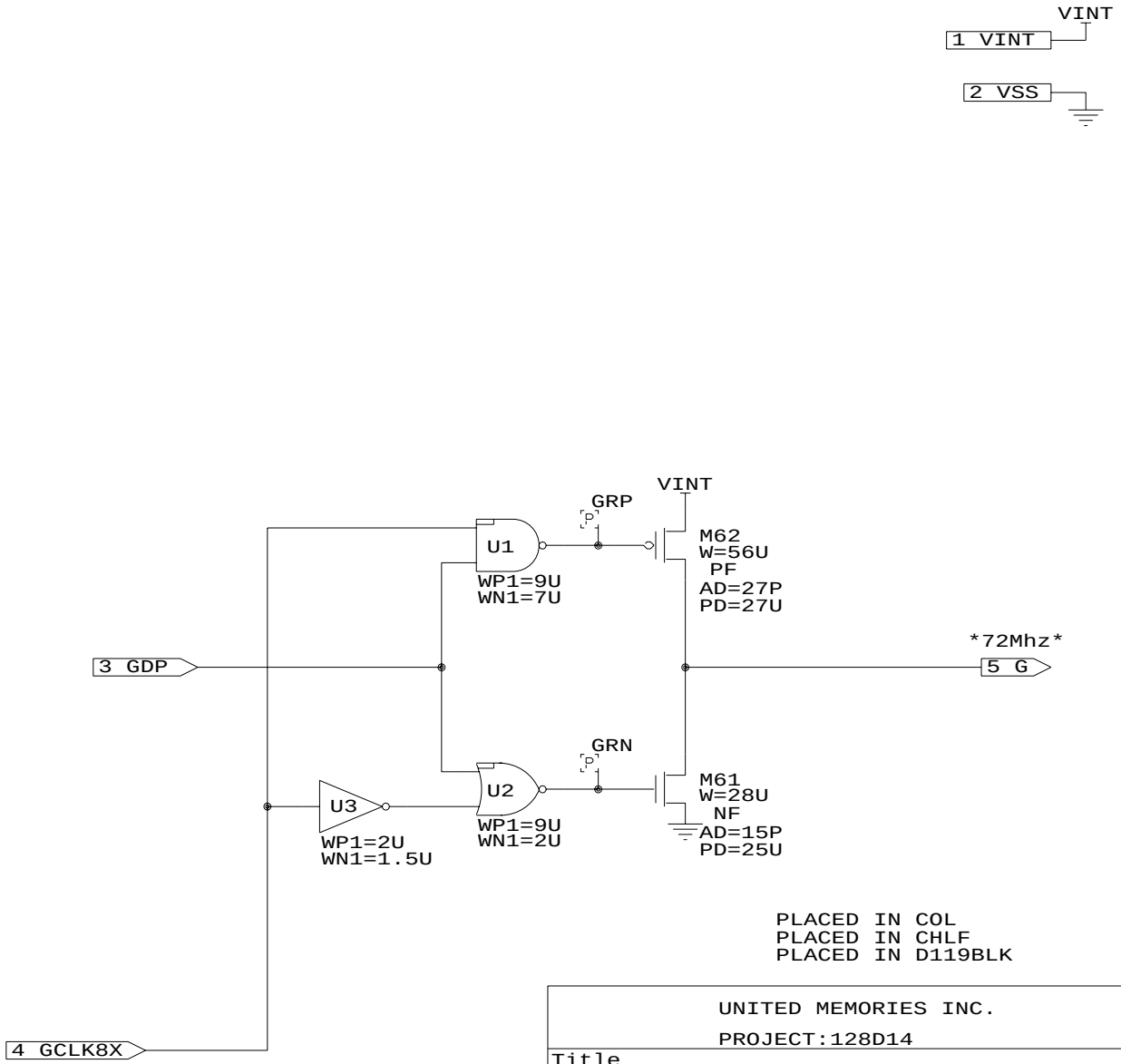


A0 - BETTER BALANCED

UNITED MEMORIES INC.		
PROJECT:128D14		
Title	DATA SENSE AMP	
Size B	Document Number DAMP	REV A0
Date: February 4, 2002	Sheet 1 of 1	

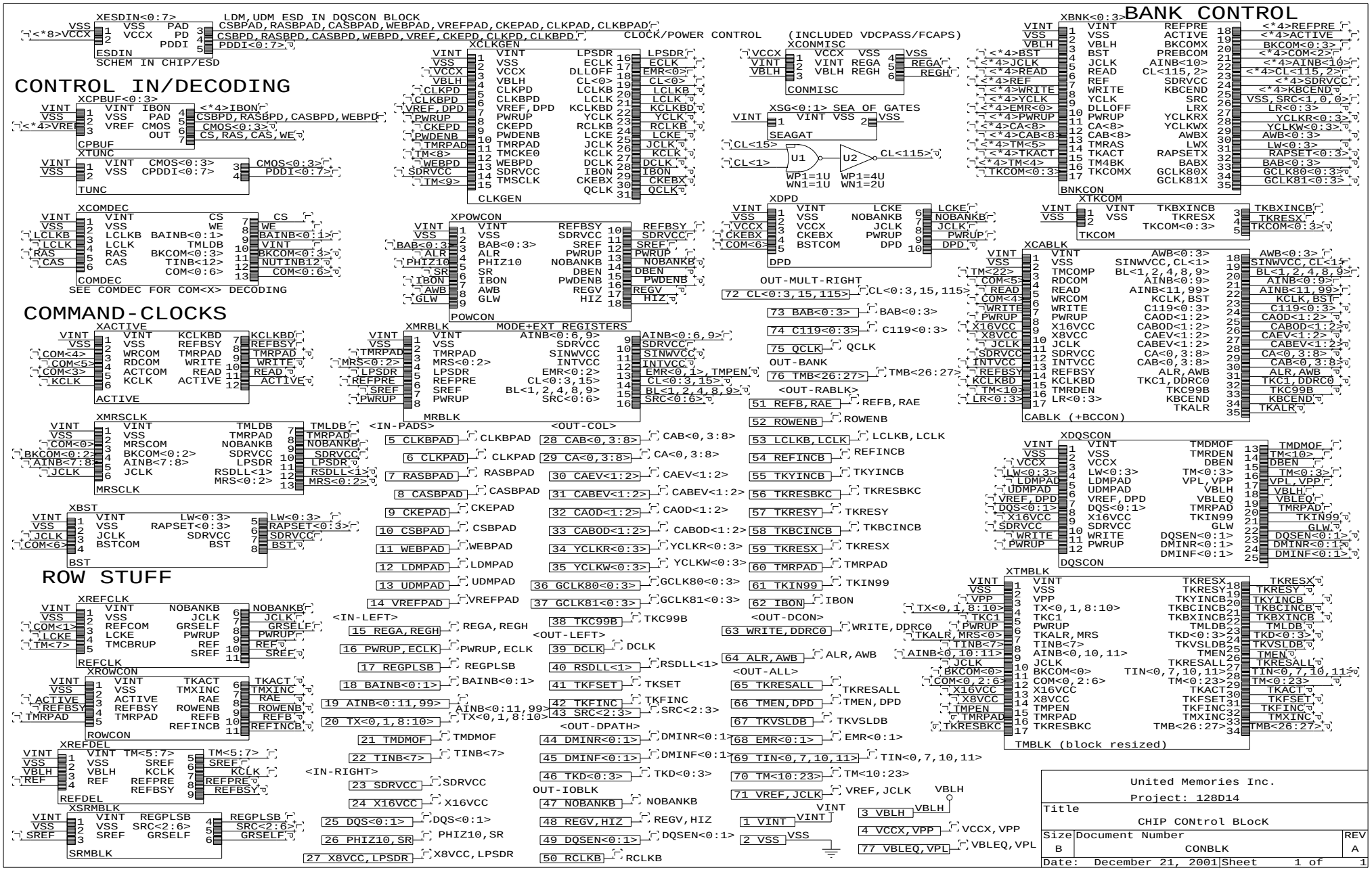


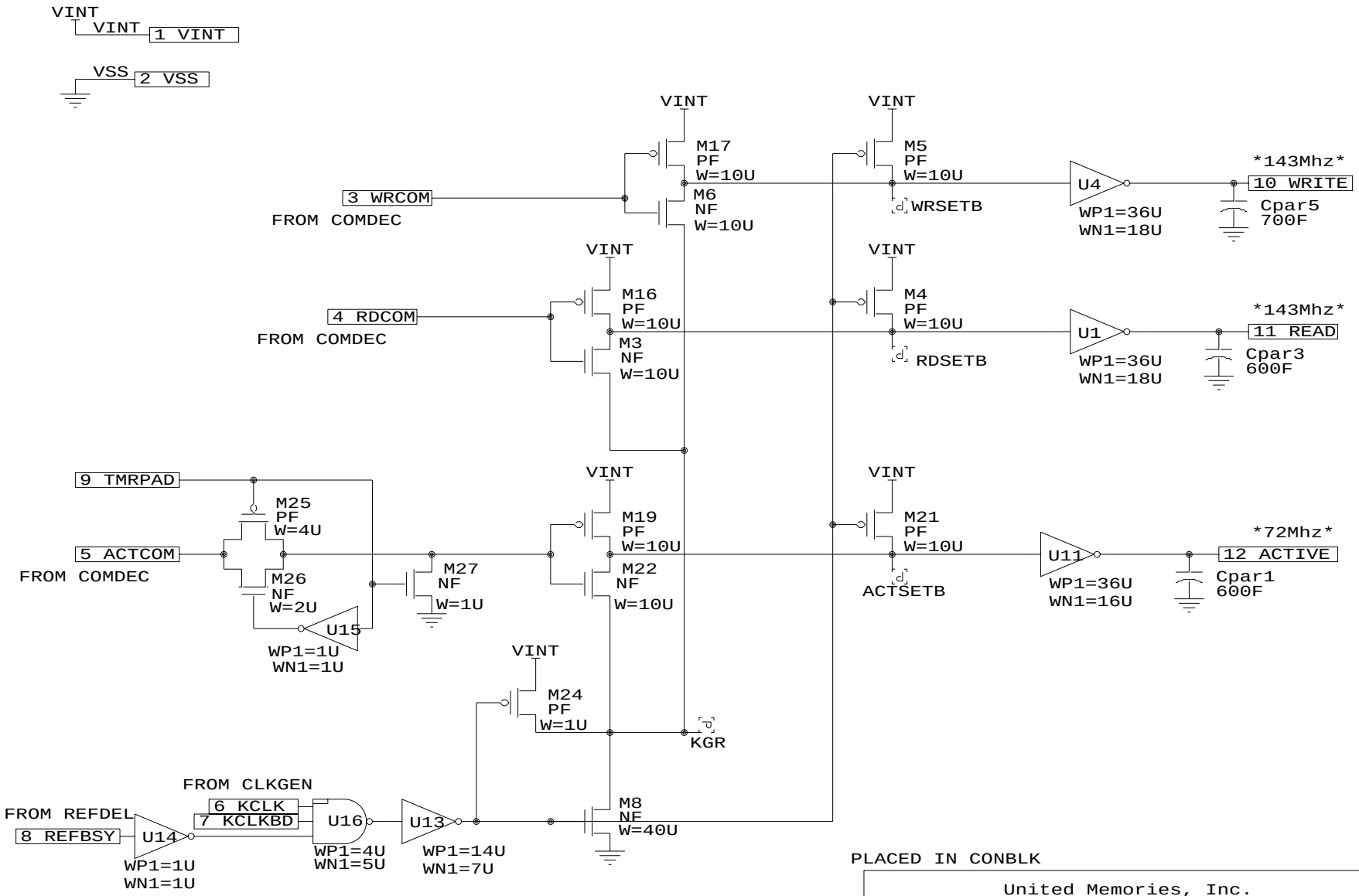
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
INPUT DATA DRIVE		
Size A	Document Number DDRV	REV A
Date: December 4, 2001	Sheet 1 of 1	



PLACED IN COL
PLACED IN CHLF
PLACED IN D119BLK

UNITED MEMORIES INC. PROJECT:128D14		
Title DATA SLAVE AND OUTPUT MUX		
Size A	Document Number GMUX	REV A
Date: October 24, 2001	Sheet 1 of 1	

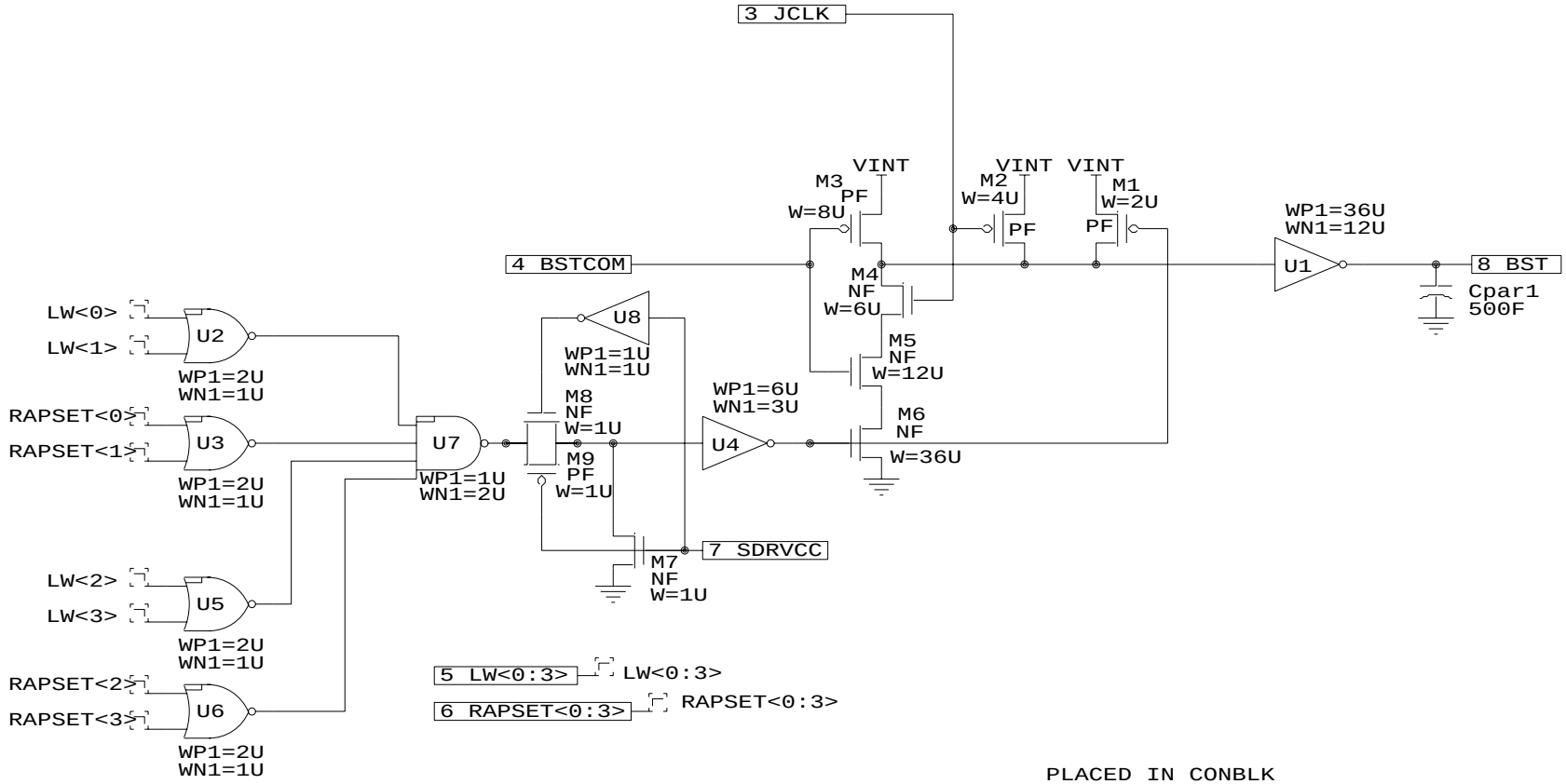

BANK CONTROL
CONTROL IN/DECODING
COMMAND-CLOCKS
ROW STUFF
XESDIN<0:7>
LDM,UDM ESD IN DQSCON BLOCK
CSBPAD,RASBPAD,CASBPAD,WEBPAD,VREFPAD,CKEPAD,CLKPAD,CLKBPAD
CSBPD,RASBPD,CASBPD,WEBPD,VREF,CKEPD,CLKPD,CLKBPD
PDDI<0:7>
ESDIN
SCHEM IN CHIP/ESD
CLOCK/POWER CONTROL
(INCLUDED VDCPASS/FCAPS)
XCLKGEN
XCONMISC
CONMISC
XSG<0:1> SEA OF GATES
SEAGAT
U1
U2
WP1=1U WN1=1U
WP1=4U WN1=2U
XBNK<0:3>
BNKCON
XCPBUF<0:3>
CPBUF
XTUNC
TUNC
XCOMDEC
COMDEC
SEE COMDEC FOR COM<X> DECODING
XPOWCON
POWCON
XDPD
DPD
XTKCOM
TKCOM
XCABLK
CABLK (+BCCON)
XACTIVE
ACTIVE
XMRBLK
MODE+EXT REGISTERS
MRBLK
OUT-MULT-RIGHT
OUT-BANK
OUT-RABLK
OUT-COL
OUT-DCON
OUT-ALL
OUT-LEFT
OUT-DPATH
OUT-IOBLK
IN-PADS
IN-LEFT
IN-RIGHT
XMRSCLK
MRSCLK
XDQSCON
DQSCON
XBST
BST
XREFCLK
REFCLK
XROWCON
ROWCON
XREFDEL
REFDEL
XSRMBLK
SRMBLK
XTMBLK
TMBLK (block resized)
United Memories Inc.
Project: 128D14
Title
CHIP CONtrol BLocK
Size B
Document Number
CONBLK
REV A
Date: December 21, 2001
Sheet 1 of 1



PLACED IN CONBLK

LOCKOUT THESE COMMANDS DURING REFRESH CYCLES

United Memories, Inc. PROJECT: 128D14		
Title ACTIVE / READ / WRITE GENERATION		
Size A	Document Number ACTIVE	REV A
Date: October 12, 2001	Sheet 1 of 1	

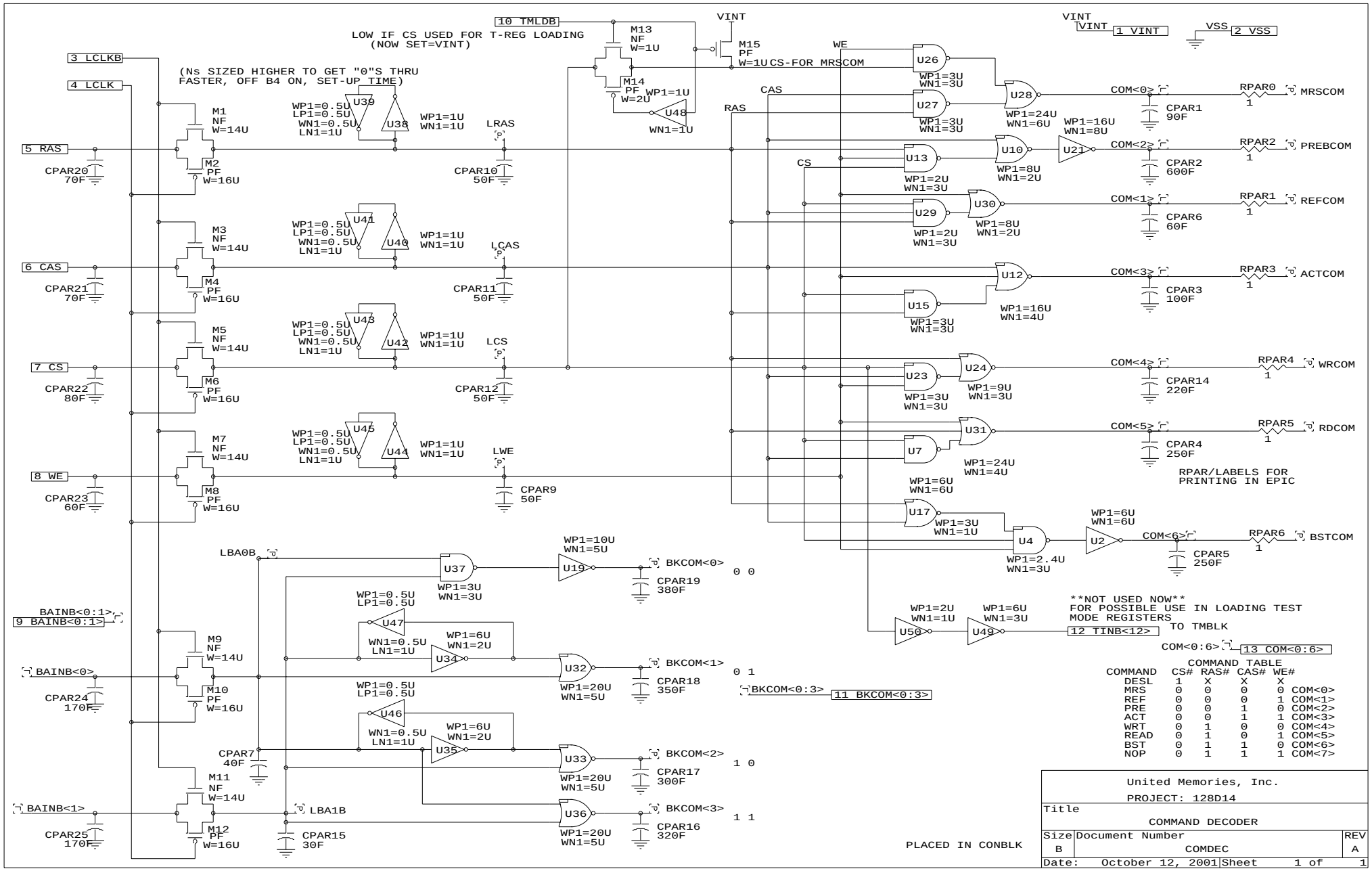


PLACED IN CONBLK

VINT
VINT 1 VINT
VSS 2 VSS

INHIBIT BST IF ANY READ AUTO-PRECHARGE IS SET,
OR THE PART IS BURST-WRITING
(DON'T NEED WRITE AUTO PRECHARGE SINCE LWX=1 ANYWAY!)

United Memories, Inc. PROJECT: 128D14		
Title BURST STOP DETECT		
Size A	Document Number BST	REV A
Date: October 6, 2001	Sheet 1 of 1	



COMMAND TABLE

COMMAND	CS#	RAS#	CAS#	WE#	
DESL	1	X	X	X	
MRS	0	0	0	0	COM<0>
REF	0	0	0	1	COM<1>
PRE	0	0	1	0	COM<2>
ACT	0	0	1	1	COM<3>
WRT	0	1	0	0	COM<4>
READ	0	1	0	1	COM<5>
BST	0	1	1	0	COM<6>
NOP	0	1	1	1	COM<7>

United Memories, Inc.

PROJECT: 128D14

Title: COMMAND DECODER

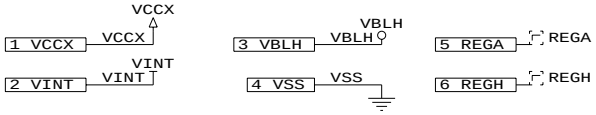
Size	Document Number	REV
B	COMDEC	A

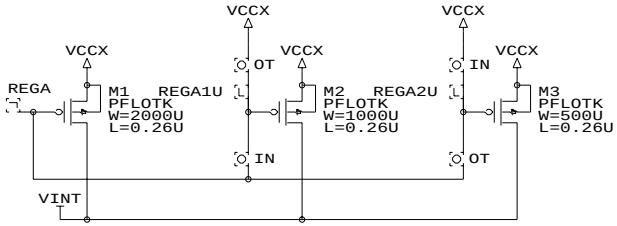
Date: October 12, 2001 | Sheet 1 of 1

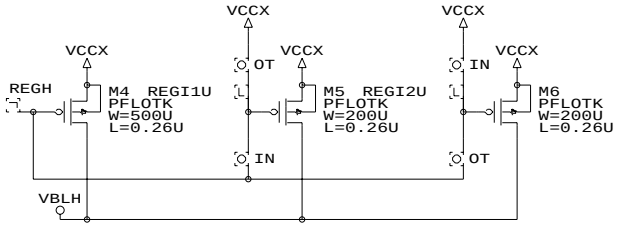
VINT
FOR 100mA:
33mA/VDCPASS = 33mA/3000U
1mA/91U
(.33mA/30U) x 100 legs
VBLH
FOR 100mA:
33mA/VDCPASS = 33mA/2000U

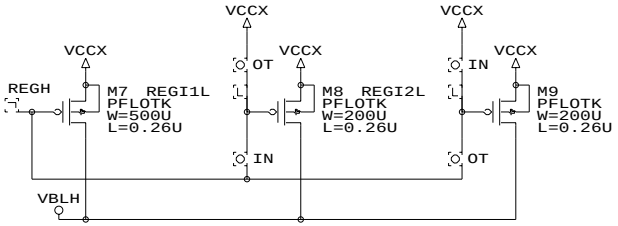
(.33mA/20U) x 100 legs

M1=.73U
C1=18/leg
C2=5/leg
M2=.2U

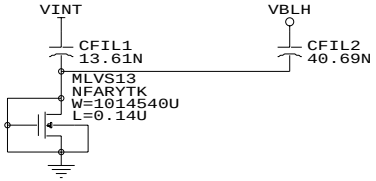






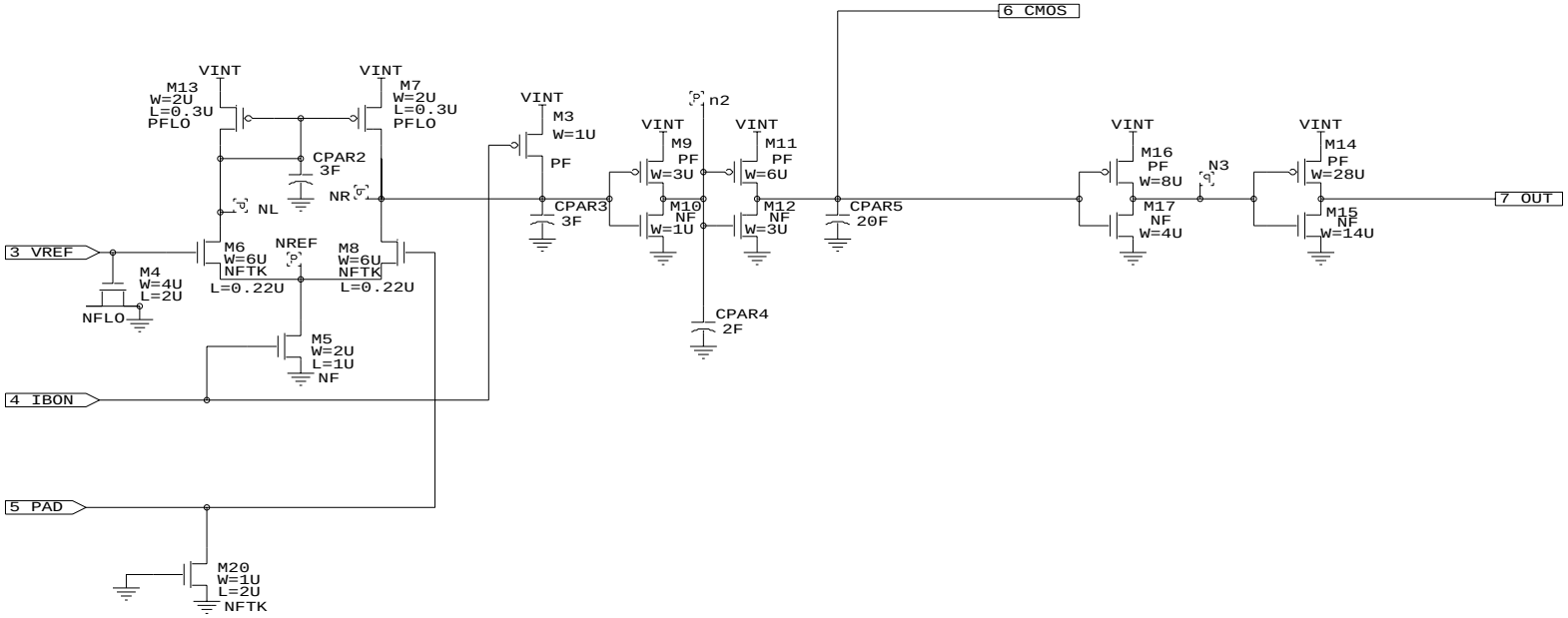


NOT SIZED



PLACED IN CONBLK

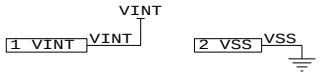
United Memories Inc.		Confidential
Project: 128DDR		
Title		
Voltage Down Converter PASS -CENTER CASE		
Size	Document Number	REV
B	CONMISC	A
Date: December 10, 2001	Sheet 1 of 1	



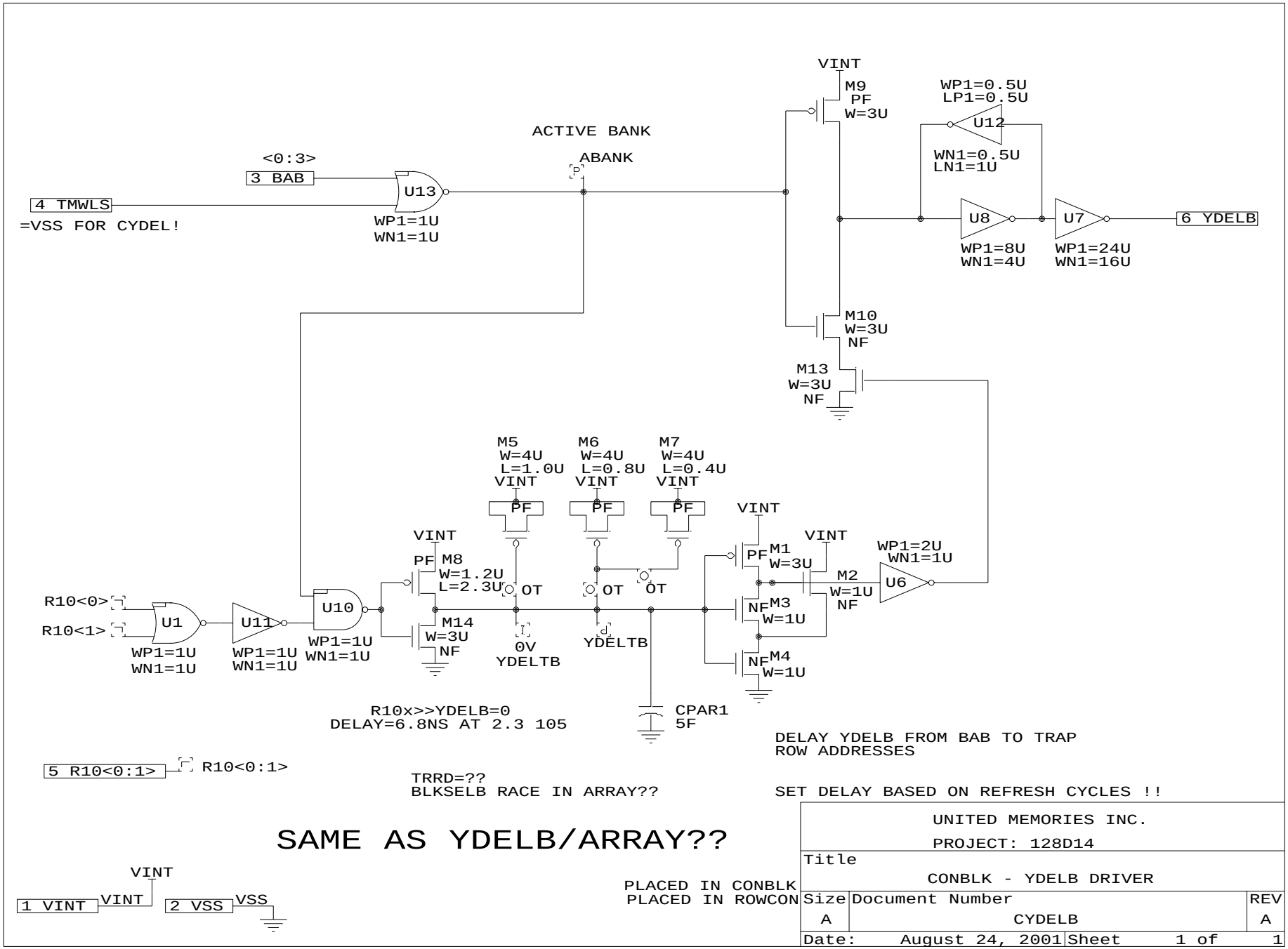
TAIL CURRENT = 320 uA
(VINT=2.2,-15,VREF=1.4)
(VINT=2.0,55,VREF=1.25)

PLACED IN CONBLK

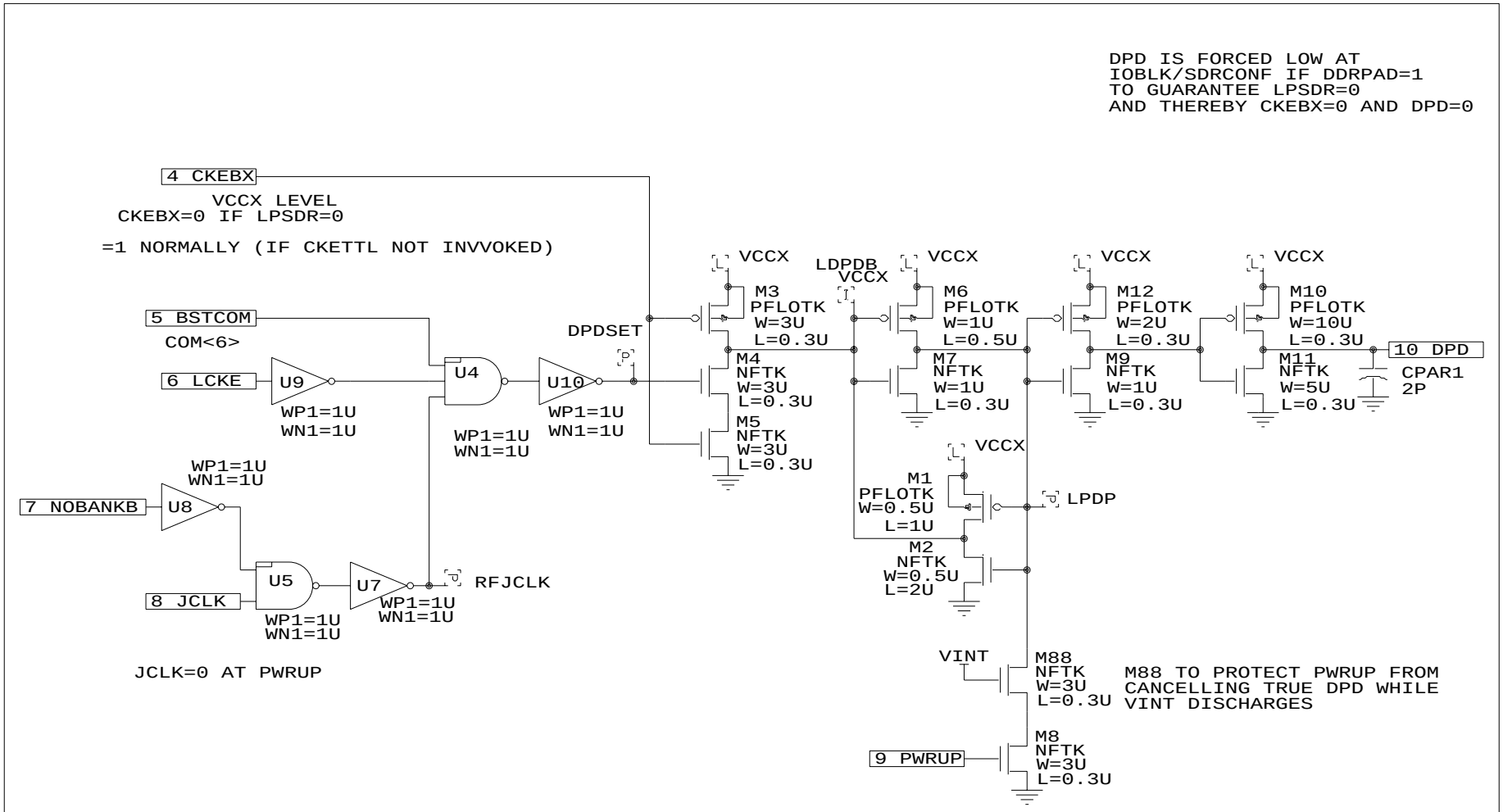
* USED FOR RAS/CAS/WE/CS



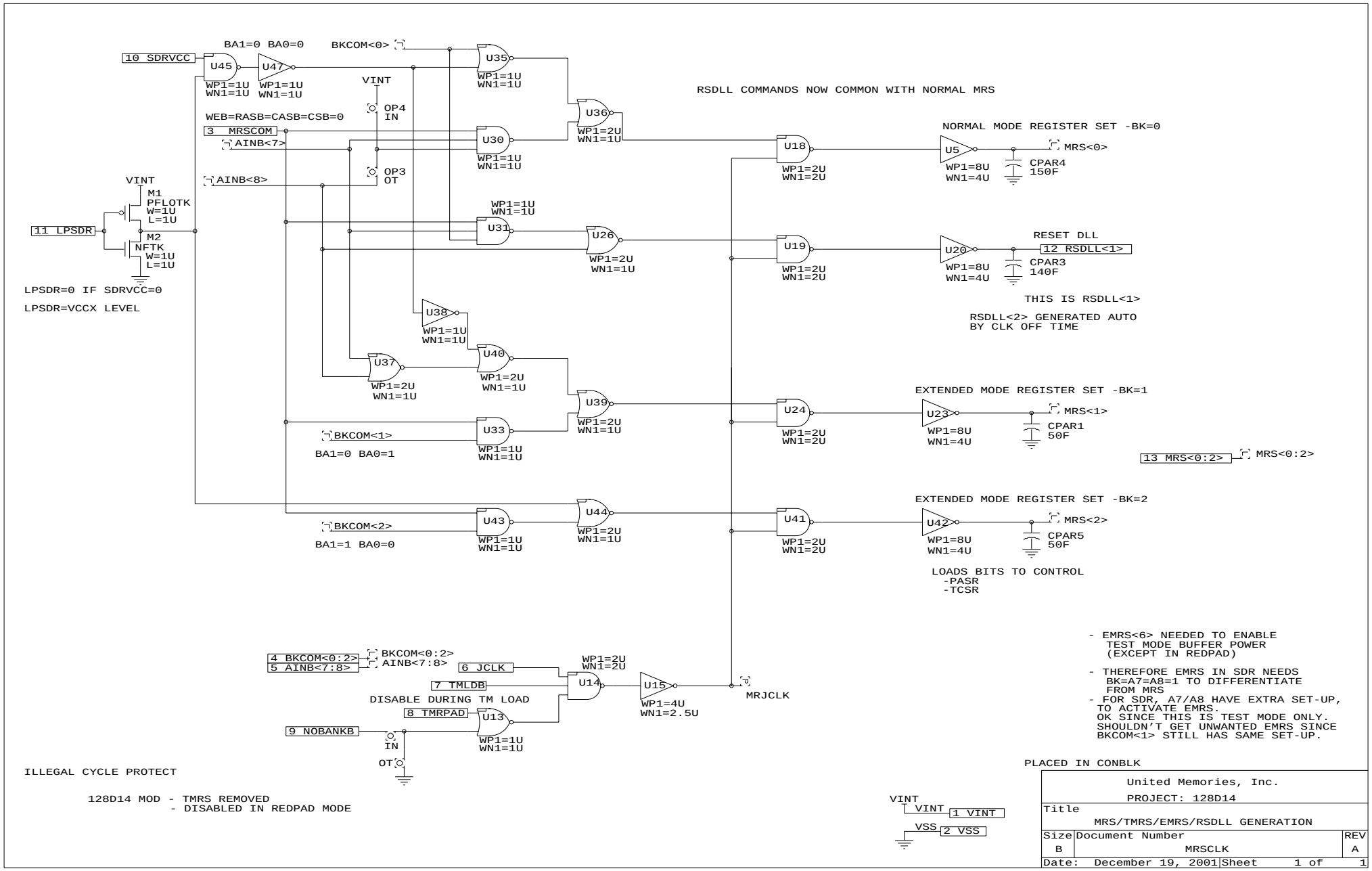
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
CONTROL INPUT BUFFER		
Size B	Document Number CPBUF	REV A
Date: October 19, 2001	Sheet 1 of 1	

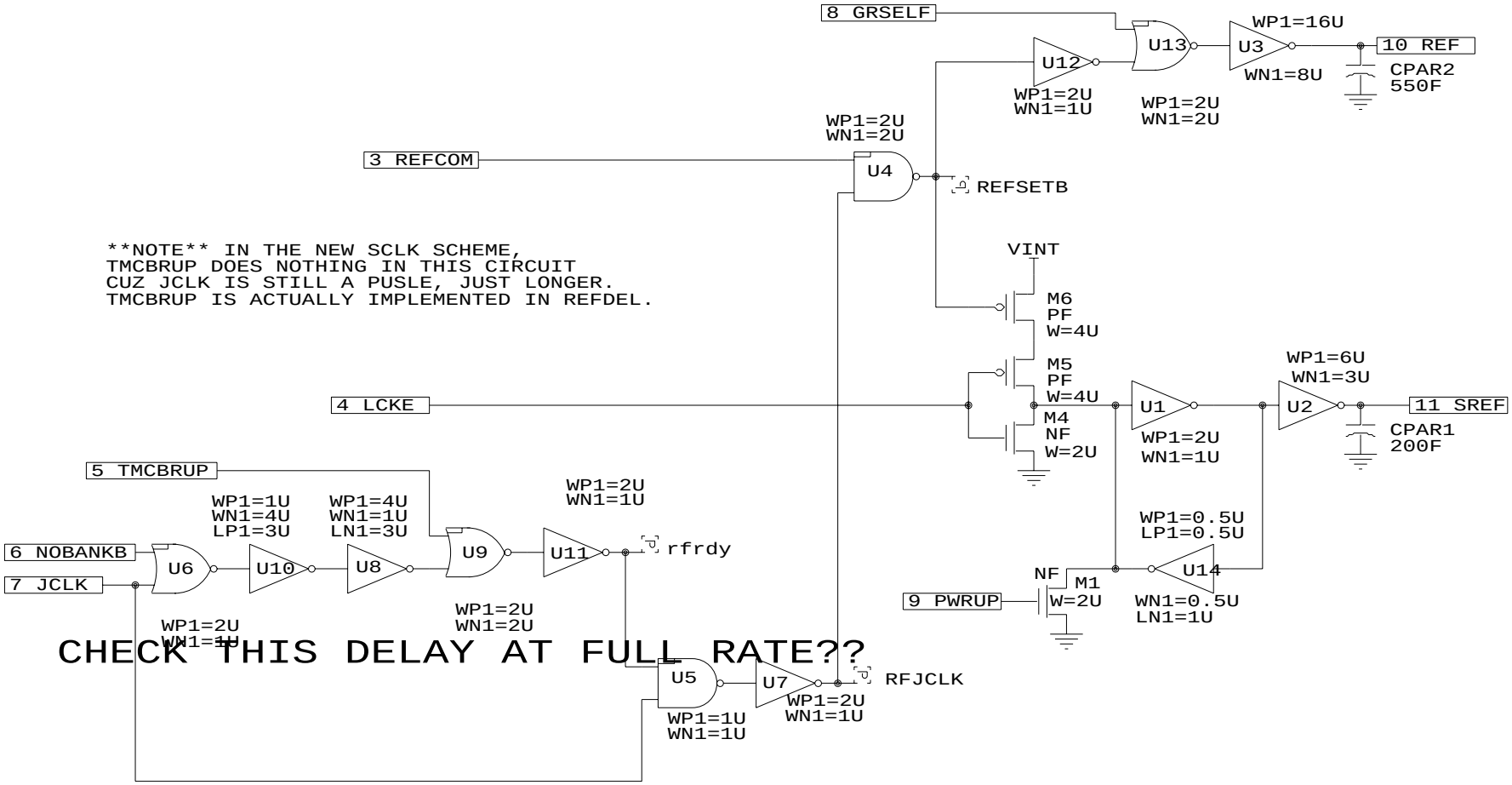


UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
CONBLK - YDELB DRIVER		
Size	Document Number	REV
A	CYDELB	A
Date: August 24, 2001	Sheet 1 of 1	



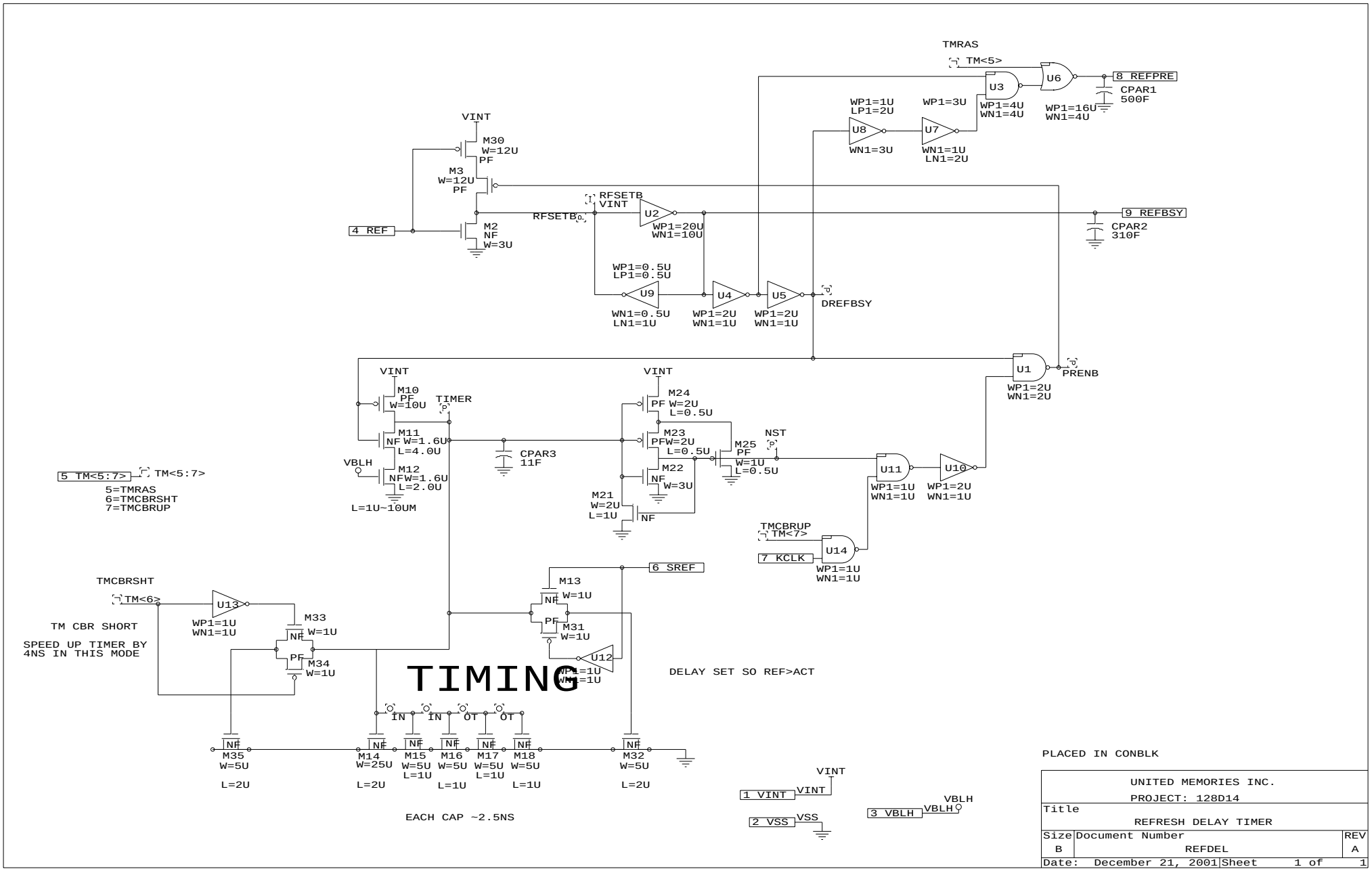
United Memories, Inc. PROJECT: 128D14		
Title DEEP POWER DOWN (DPD) GENERATION		
Size A	Document Number DPD	REV A
Date: October 30, 2001	Sheet 1 of 1	

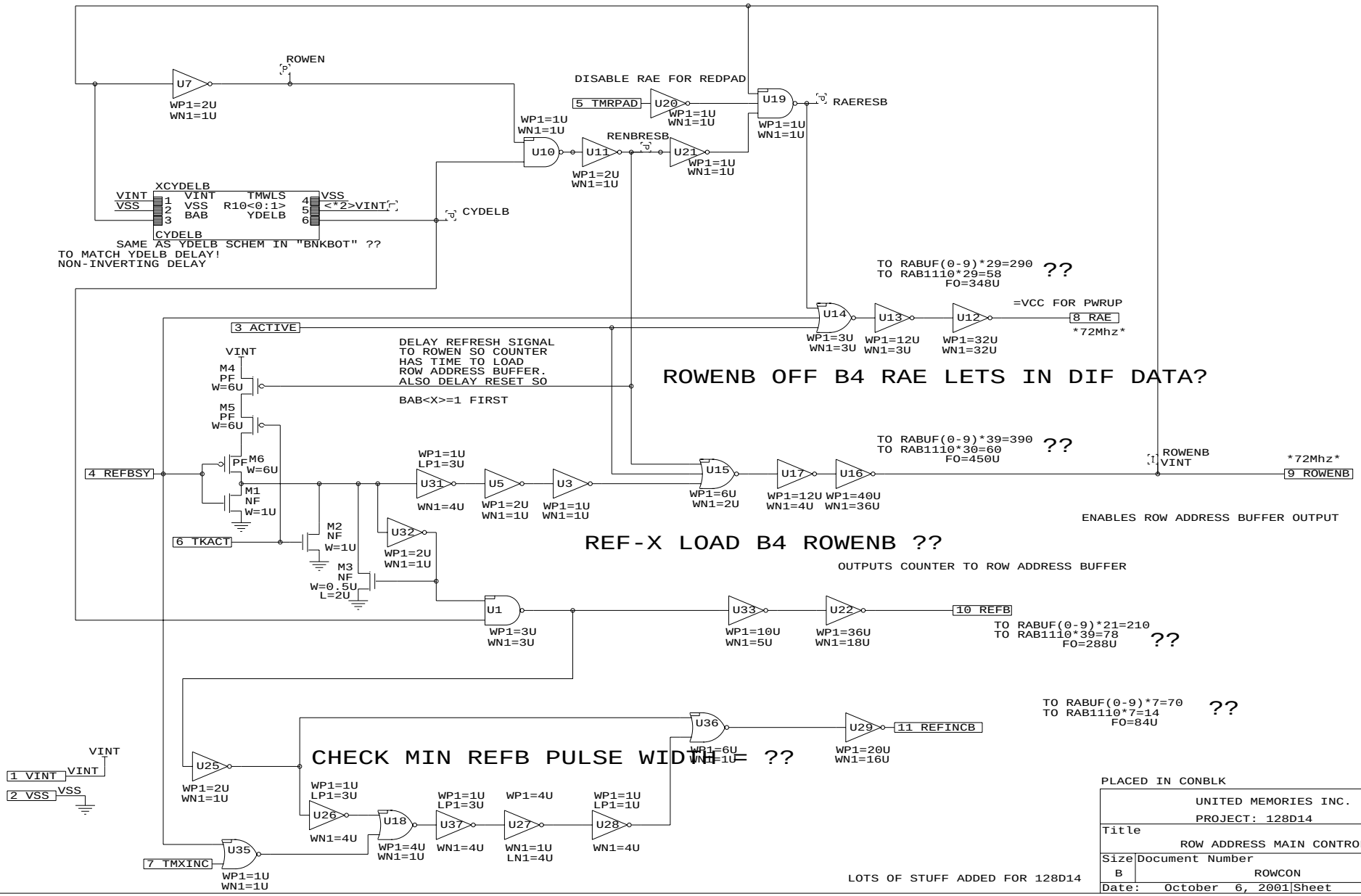

10 SDRVCC
U45
U47
WP1=1U
WN1=1U
BA1=0 BA0=0
BKCOM<0>
U35
VINT
OP4
IN
WEB=RASB=CASB=CSB=0
3 MRSCOM
AINB<7>
U30
OP3
OT
AINB<8>
U36
WP1=2U
WN1=1U
RSDLL COMMANDS NOW COMMON WITH NORMAL MRS
U18
WP1=2U
WN1=2U
NORMAL MODE REGISTER SET -BK=0
U5
WP1=8U
WN1=4U
MRS<0>
CPAR4
150F
VINT
M1
PFLOTK
W=1U
L=1U
11 LPSDR
M2
NFTK
W=1U
L=1U
LPSDR=0 IF SDRVCC=0
LPSDR=VCCX LEVEL
U31
U26
U19
U20
RESET DLL
12 RSDLL<1>
CPAR3
140F
THIS IS RSDLL<1>
RSDLL<2> GENERATED AUTO
BY CLK OFF TIME
U38
U37
U40
U39
U33
BKCOM<1>
BA1=0 BA0=1
U24
U23
EXTENDED MODE REGISTER SET -BK=1
MRS<1>
CPAR1
50F
13 MRS<0:2>
MRS<0:2>
U43
U44
U41
U42
BKCOM<2>
BA1=1 BA0=0
EXTENDED MODE REGISTER SET -BK=2
MRS<2>
CPAR5
50F
LOADS BITS TO CONTROL
-PASR
-TCSR
4 BKCOM<0:2>
5 AINB<7:8>
BKCOM<0:2>
AINB<7:8>
6 JCLK
7 TMLDB
DISABLE DURING TM LOAD
8 TMRPAD
9 NOBANKB
U14
U15
WP1=4U
WN1=2.5U
MRJCLK
U13
IN
OT
- EMRS<6> NEEDED TO ENABLE
TEST MODE BUFFER POWER
(EXCEPT IN REDPAD)
- THEREFORE EMRS IN SDR NEEDS
BK=A7=A8=1 TO DIFFERENTIATE
FROM MRS
- FOR SDR, A7/A8 HAVE EXTRA SET-UP,
TO ACTIVATE EMRS.
OK SINCE THIS IS TEST MODE ONLY.
SHOULDN'T GET UNWANTED EMRS SINCE
BKCOM<1> STILL HAS SAME SET-UP.
PLACED IN CONBLK
ILLEGAL CYCLE PROTECT
128D14 MOD - TMRS REMOVED
- DISABLED IN REDPAD MODE
VINT
1 VINT
VSS
2 VSS
United Memories, Inc.
PROJECT: 128D14
Title
MRS/TMRS/EMRS/RSDLL GENERATION
Size
B
Document Number
MRSCLK
REV
A
Date: December 19, 2001
Sheet 1 of 1

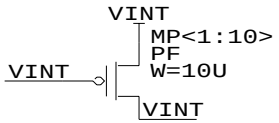


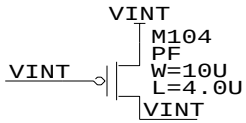
PLACED IN CONBLK

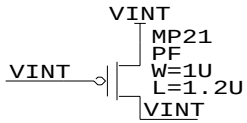
United Memories, Inc. PROJECT: 128D14		
Title REF/SELF GENERATION		
Size A	Document Number REFCLK	REV A
Date: December 21, 2001	Sheet 1 of 1	

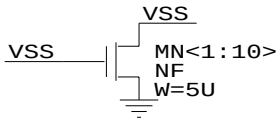

TMRAS
TM<5>
U6
8 REFPRE
CPAR1
500F
U3
WP1=4U
WN1=4U
WP1=16U
WN1=4U
WP1=1U
LP1=2U
WP1=3U
U8
WN1=3U
U7
WN1=1U
LN1=2U
VINT
M30
W=12U
PF
M3
W=12U
PF
RFSETB
VINT
RFSETB
U2
WP1=20U
WN1=10U
9 REFBSY
CPAR2
310F
4 REF
M2
NF
W=3U
WP1=0.5U
LP1=0.5U
U9
WN1=0.5U
LN1=1U
U4
WP1=2U
WN1=1U
U5
WP1=2U
WN1=1U
DREFBSY
U1
PRENB
WP1=2U
WN1=2U
VINT
M10
PF
W=10U
TIMER
M11
NF
W=1.6U
L=4.0U
VBLH
M12
NF
W=1.6U
L=2.0U
L=1U~10UM
CPAR3
11F
VINT
M24
PF
W=2U
L=0.5U
M23
PF
W=2U
L=0.5U
M25
PF
W=1U
L=0.5U
NST
M22
NF
W=3U
M21
W=2U
L=1U
NF
U11
WP1=1U
WN1=1U
U10
WP1=2U
WN1=1U
5 TM<5:7>
TM<5:7>
5=TMRAS
6=TMCBRSHT
7=TMCBRUP
TMCBRUP
TM<7>
7 KCLK
U14
WP1=1U
WN1=1U
6 SREF
TMCBRSHT
TM<6>
U13
WP1=1U
WN1=1U
TM CBR SHORT
SPEED UP TIMER BY
4NS IN THIS MODE
M33
NF
W=1U
PF
M34
W=1U
M13
NF
W=1U
PF
M31
W=1U
U12
WP1=1U
WN1=1U
TIMING
DELAY SET SO REF>ACT
IN
IN
OT
OT
NF
M35
W=5U
L=2U
M14
W=25U
L=2U
M15
W=5U
L=1U
M16
W=5U
L=1U
M17
W=5U
L=1U
M18
W=5U
L=1U
M32
W=5U
L=2U
EACH CAP ~2.5NS
VINT
1 VINT
VINT
2 VSS
VSS
VBLH
3 VBLH
VBLH
PLACED IN CONBLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
REFRESH DELAY TIMER
Size
B
Document Number
REFDEL
REV
A
Date: December 21, 2001
Sheet 1 of 1

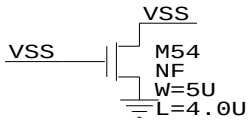

ROWEN
U7
WP1=2U
WN1=1U
DISABLE RAE FOR REDPAD
5 TMRPAD
U20
WP1=1U
WN1=1U
U19
RAERESB
WP1=1U
WN1=1U
WP1=1U
WN1=1U
U10
U11
RENBRESB
U21
WP1=1U
WN1=1U
WP1=2U
WN1=1U
XCYDELB
VINT
VSS
VINT
VSS
BAB
TMWLS
R10<0:1>
YDELB
VSS
<*2>VINT
CYDELB
CYDELB
SAME AS YDELB SCHEM IN "BNKBOT" ??
TO MATCH YDELB DELAY!
NON-INVERTING DELAY
TO RABUF(0-9)*29=290
TO RAB1110*29=58
FO=348U
??
=VCC FOR PWRUP
U14
U13
U12
8 RAE
72Mhz
WP1=3U
WN1=3U
WP1=12U
WN1=3U
WP1=32U
WN1=32U
3 ACTIVE
DELAY REFRESH SIGNAL
TO ROWEN SO COUNTER
HAS TIME TO LOAD
ROW ADDRESS BUFFER.
ALSO DELAY RESET SO
BAB<X>=1 FIRST
ROWENB OFF B4 RAE LETS IN DIF DATA?
VINT
M4
PF
W=6U
M5
PF
W=6U
PF
M6
W=6U
M1
NF
W=1U
4 REFBSY
6 TKACT
M2
NF
W=1U
M3
NF
W=0.5U
L=2U
WP1=1U
LP1=3U
U31
WN1=4U
U5
WP1=2U
WN1=1U
U3
WP1=1U
WN1=1U
U32
WP1=2U
WN1=1U
TO RABUF(0-9)*39=390
TO RAB1110*30=60
FO=450U
??
U15
WP1=6U
WN1=2U
U17
WP1=12U
WN1=4U
U16
WP1=40U
WN1=36U
ROWENB
VINT
72Mhz
9 ROWENB
ENABLES ROW ADDRESS BUFFER OUTPUT
REF-X LOAD B4 ROWENB ??
OUTPUTS COUNTER TO ROW ADDRESS BUFFER
U1
WP1=3U
WN1=3U
U33
WP1=10U
WN1=5U
U22
WP1=36U
WN1=18U
10 REFB
TO RABUF(0-9)*21=210
TO RAB1110*39=78
FO=288U
??
TO RABUF(0-9)*7=70
TO RAB1110*7=14
FO=84U
??
U36
WP1=6U
WN1=1U
U29
WP1=20U
WN1=16U
11 REFINCB
CHECK MIN REFB PULSE WIDTH = ??
VINT
1 VINT
VINT
2 VSS
VSS
U25
WP1=2U
WN1=1U
WP1=1U
LP1=3U
U26
WN1=4U
U18
WP1=4U
WN1=1U
WP1=1U
LP1=3U
U37
WN1=4U
WP1=4U
U27
WN1=1U
LN1=4U
WP1=1U
LP1=1U
U28
WN1=4U
U35
7 TMXINC
WP1=1U
WN1=1U
LOTS OF STUFF ADDED FOR 128D14
PLACED IN CONBLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
ROW ADDRESS MAIN CONTROL
Size
B
Document Number
ROWCON
REV
A
Date: October 6, 2001
Sheet 1 of 1

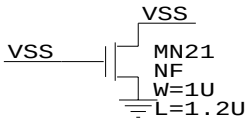


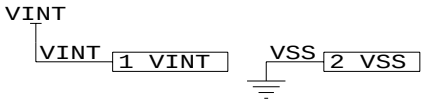






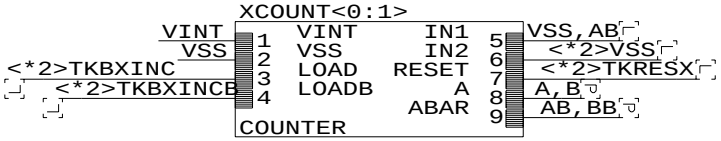


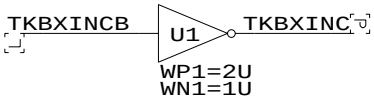




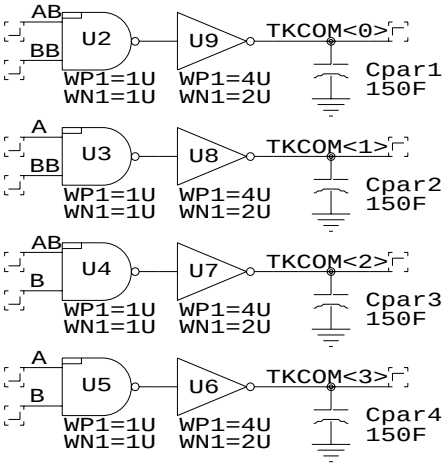
PLACED IN CONBLK

UNITED MEMORIES INC. PROJECT: 128D14		
Title EXTRA TRANSISTORS (SEA OF GATES)		
Size A	Document Number SEAGAT	REV A
Date: August 24, 2001	Sheet 1 of 1	





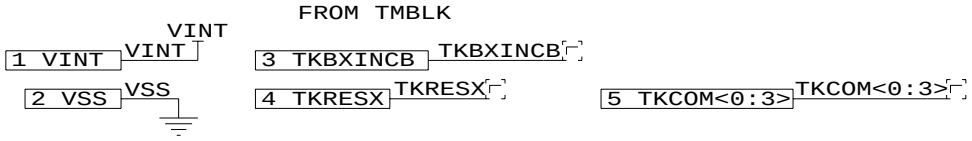
TO BNKCON<0:3>\BAB



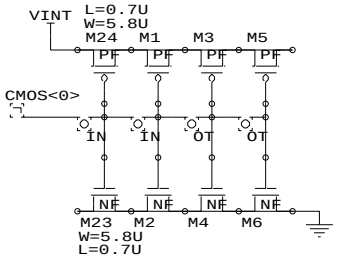
TKCOM IS THE BANK ADDRESS
FOR ROWS IN REDPAD MODE

PLACED IN CONBLK

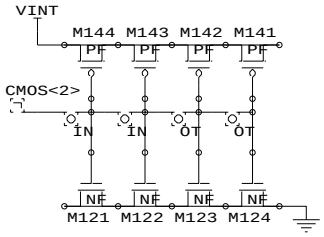
FROM TMBLK



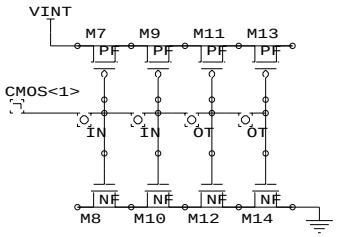
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
TKCOM		
Size A	Document Number TKCOM	REV A
Date: October 6, 2001	Sheet 1 of 1	



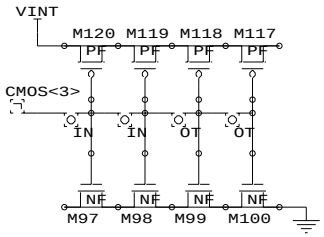
CS



CAS



RAS

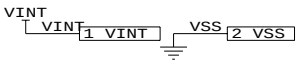


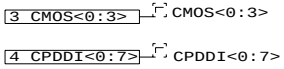
WE

100-200 PS/CAP

P-CHAN W=5.4U L=0.7U

N-CHAN W=5.4U L=0.7U





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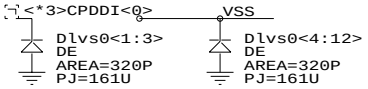

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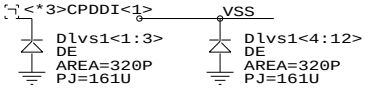

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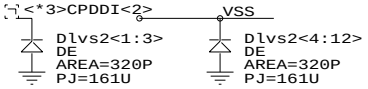
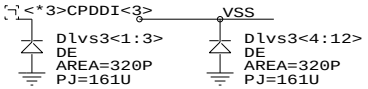
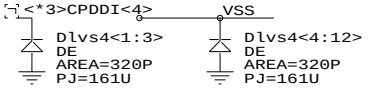


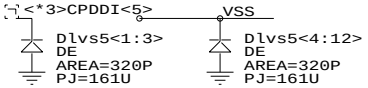
WE



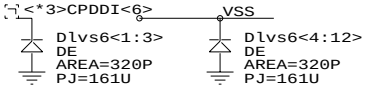
VREF



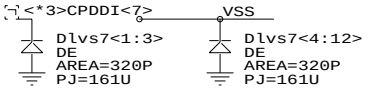
CKE



CLK



CLKB

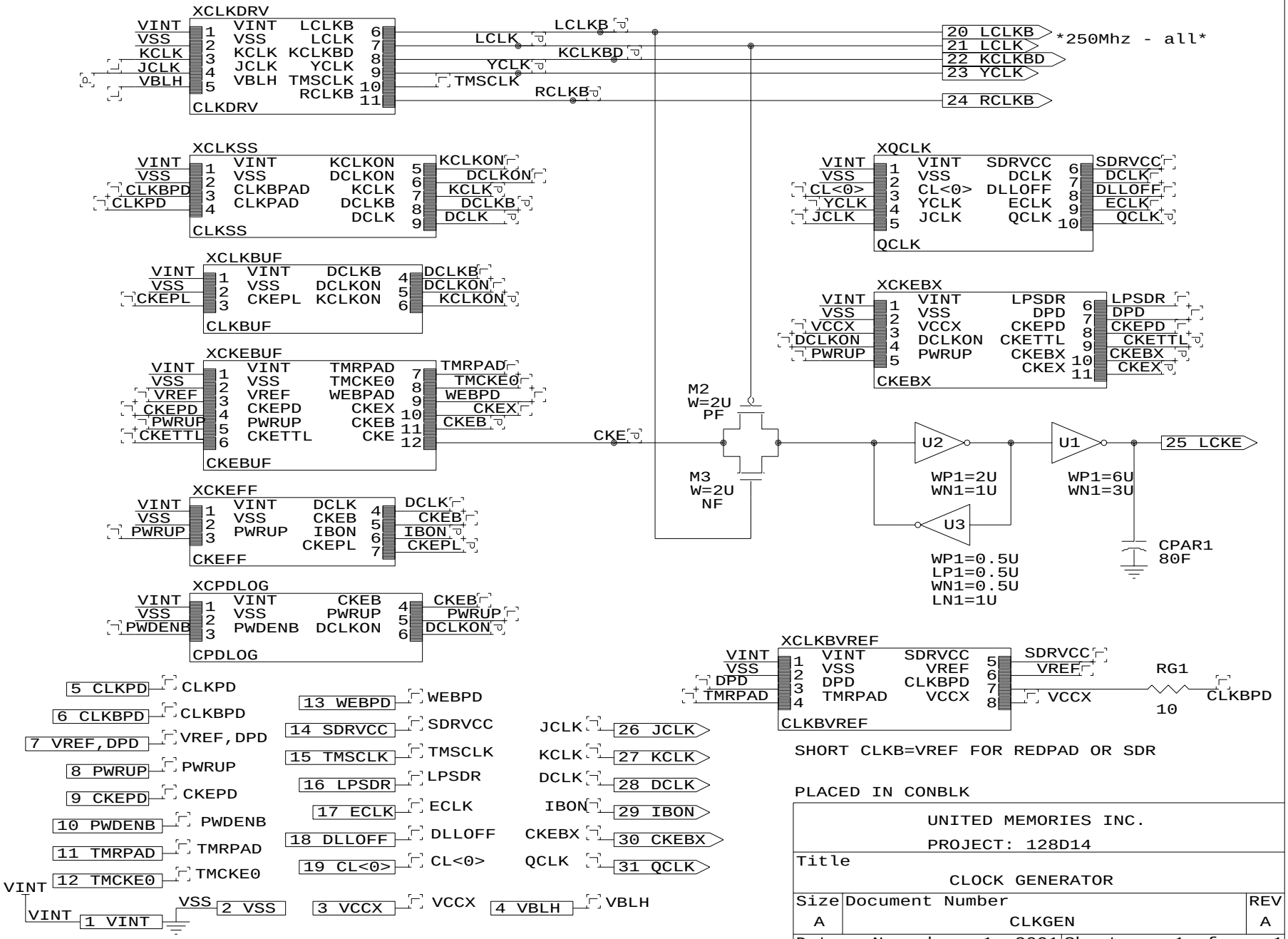


PLACED IN CONBLK

12 WELL DIODES UNDER THE PADS

THESE DIODES ARE TO ADD PAD CAPACITANCE

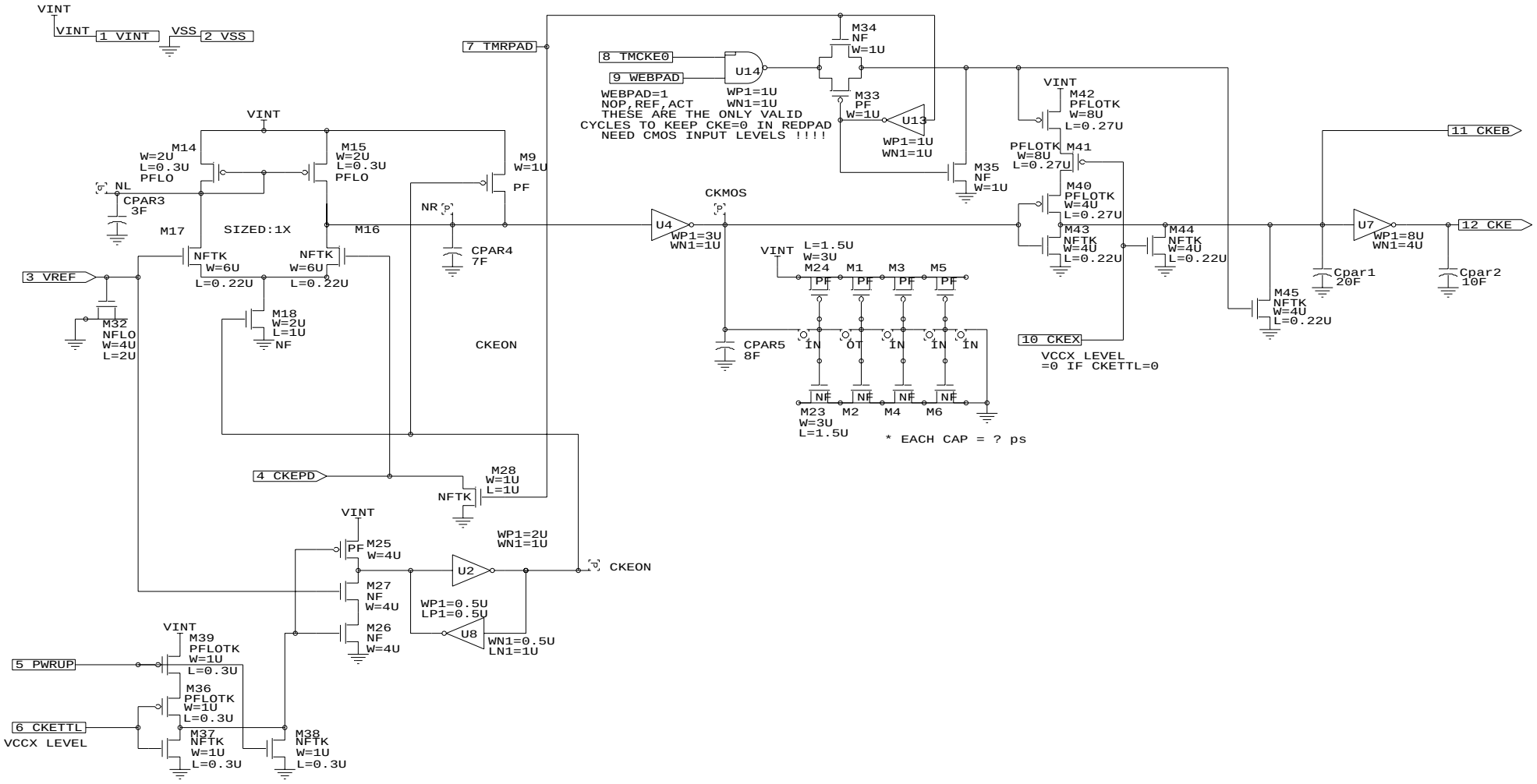
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title TUNNING CIRCUIT FOR CONTROL SIGNALS		
Size B	Document Number TUNC	REV A
Date: October 24, 2001	Sheet 1 of 1	



SHORT CLKB=VREF FOR REDPAD OR SDR

PLACED IN CONBLK

UNITED MEMORIES INC. PROJECT: 128D14		
Title CLOCK GENERATOR		
Size A	Document Number CLKGEN	REV A
Date: November 1, 2001	Sheet 1 of 1	



TURN OFF SSTL CKEBUF AND FORCE CKMOS=0

IF PWRUP=1, AND STAY OFF UNTIL VREF=1
(TEST MODE FOR DDR, LOWEST POWER)

OR

CKETTL=1

(CKETTL=1 IF LPSDR MODE=1, AND CLKON=0)

IF DEEP POWER DOWN IS ENTERED (DPD)
THIS CKEBUF IS NOT NEEDED AND WILL FADE WITH VINT.

FOR TMRPAD=1, CKEPAD=0
IF TMCKE0=1 AND WEBPAD=1, CKE=CKEPAD=0
(i.e. WEBPAD pad must be held high)
ELSE, CKE=1

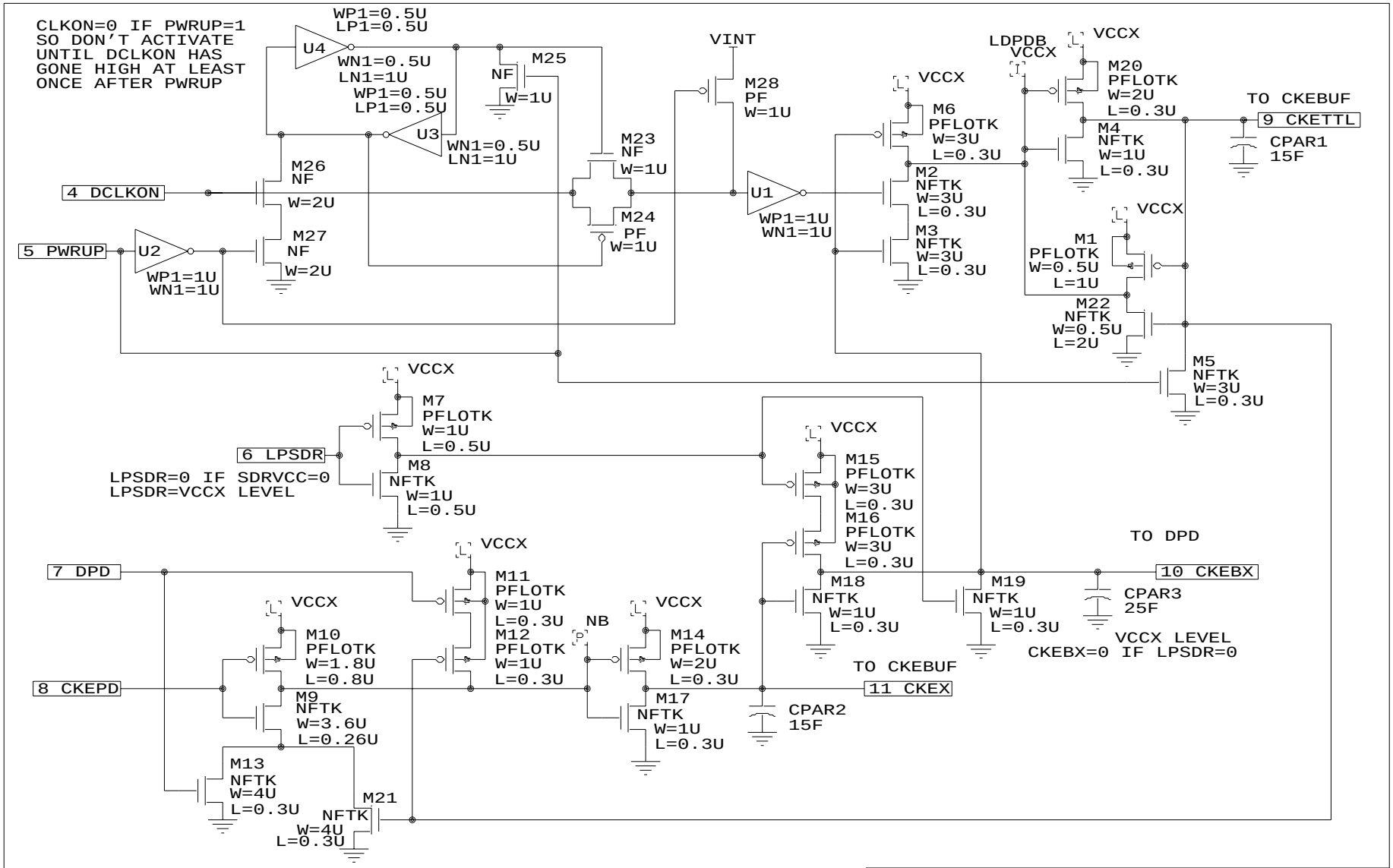
FOR TMRPAD=0, CKE=CKEPAD
EXCEPT FOR CKETTL MODE...

PLACED IN CLKGEN

UNITED MEMORIES INC.

PROJECT: 128D14

Title		
	CKE INPUT BUFFER	
Size	Document Number	REV
B	CKEBUF	A
Date: November 1, 2001	Sheet 1 of 1	

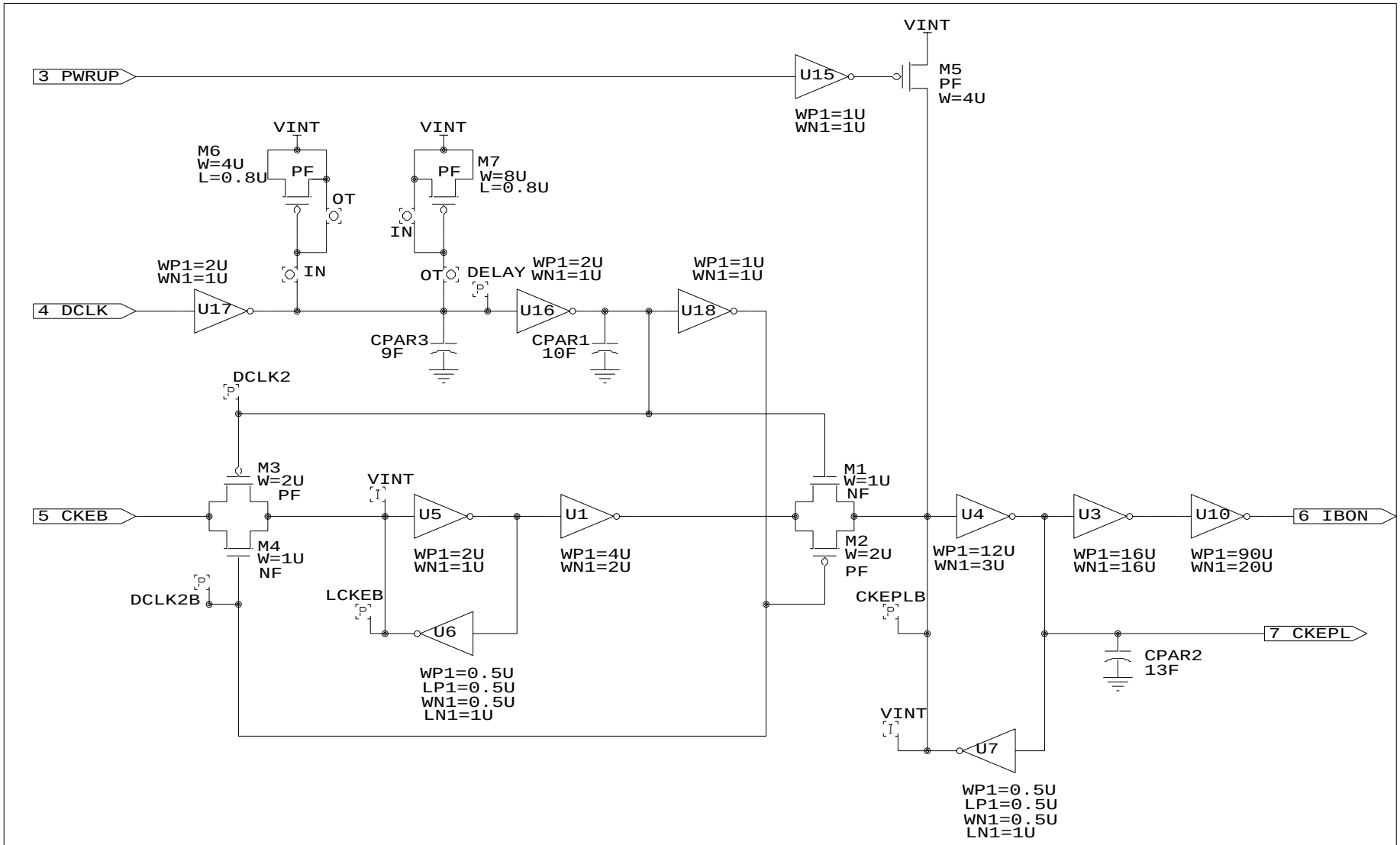


KIND OF A CIRCULAR PATH
WITH CKEBX/CKEBUF/CLKBUF
DOES IT WORK???

VINT
VINT 1 VINT
VSS 2 VSS
3 VCCX VCCX

PLACED IN CONBLK
PLACED IN CLKGEN

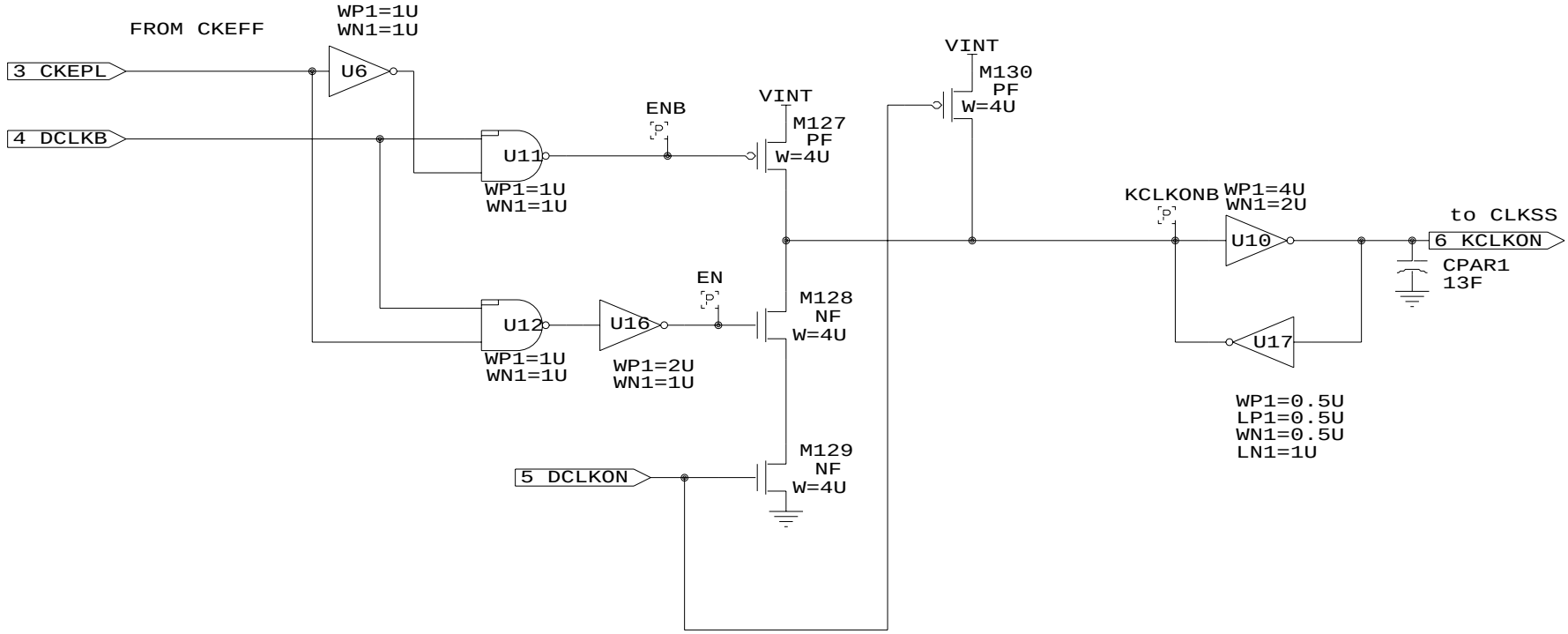
United Memories, Inc.		
PROJECT: 128D14		
Title		
CKEBX/CKEX/CKETTL GENERATION		
Size	Document Number	REV
A	CKEBX	A
Date: December 10, 2001	Sheet 1 of 1	



UNITED MEMORIES INC.

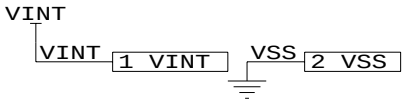
PROJECT: 128D14

Title		
CKE FLIP-FLOP		
Size A	Document Number CKEFF	REV A
Date: October 12, 2001	Sheet 1 of 1	

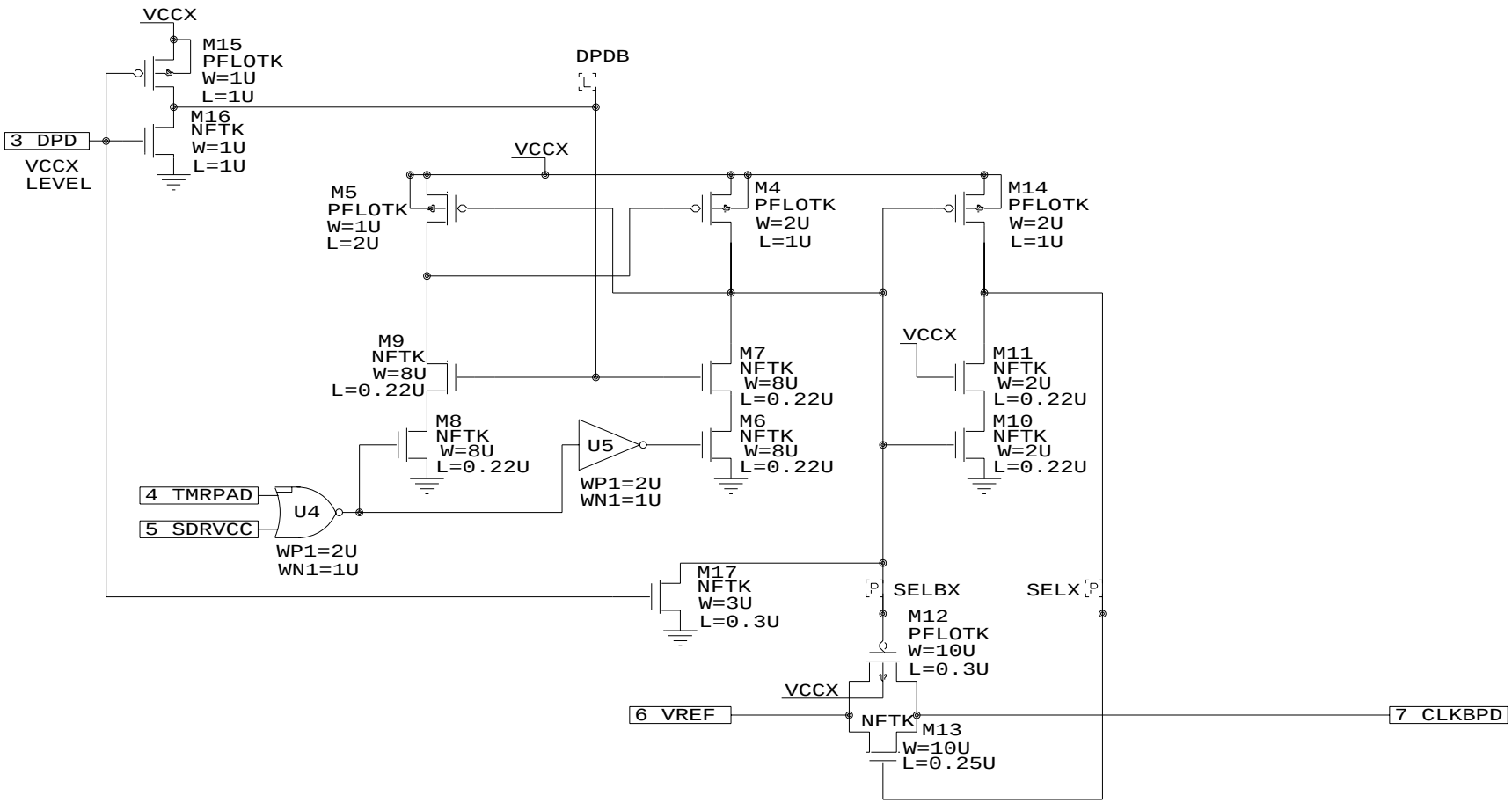


CHECK FOR GLITCHES, SKEWS WERE REMOVED

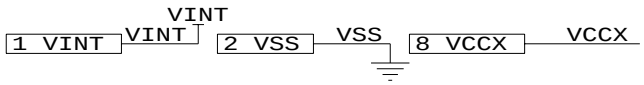
PLACED IN CLKGEN



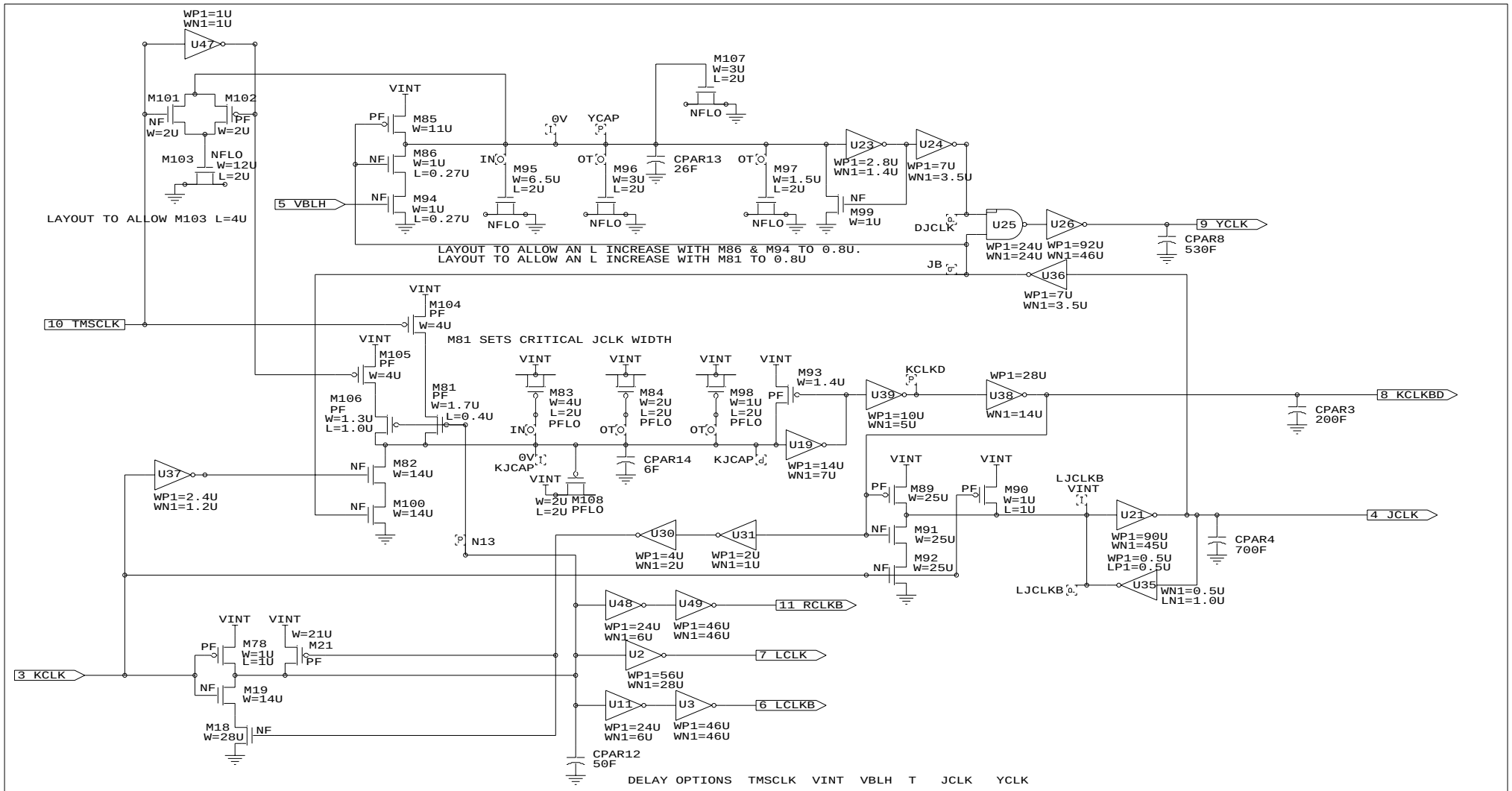
UNITED MEMORIES INC. PROJECT: 128D14		
Title CLK BUFFERING LOGIC		
Size A	Document Number CLKBUF	REV A
Date: October 12, 2001	Sheet 1 of 1	



PLACED IN CLKGEN



United Memories Inc. Project: 128D14		
Title CLKB=VREF FOR SDR AND RPAD MODES		
Size A	Document Number CLKBVREF	REV A
Date: December 7, 2001	Sheet 1 of 1	



DELAY OPTIONS	TMSCLK	VINT	VBLH	T	JCLK	YCLK
000	0	2.0	1.6	45	1.14	0.96
001	0	2.0	1.6	45	1.25	1.14
010	0	2.0	1.6	45	1.35	1.28
O11	0	2.0	1.6	45	1.49	1.43
100	0	2.0	1.6	45	1.59	1.61
101	0	2.0	1.6	45	1.71	1.78
110	0	2.0	1.6	45	1.80	1.93
111	0	2.0	1.6	45	1.92	2.07
110	0	1.8	1.45	105	1.93	2.07
110	0	2.2	1.75	-15	1.31	1.26
110	1	2.0	1.6	45	3.51	2.56
110	1	2.8	2.8	125	2.27	1.77

PLACED IN CLKGEN

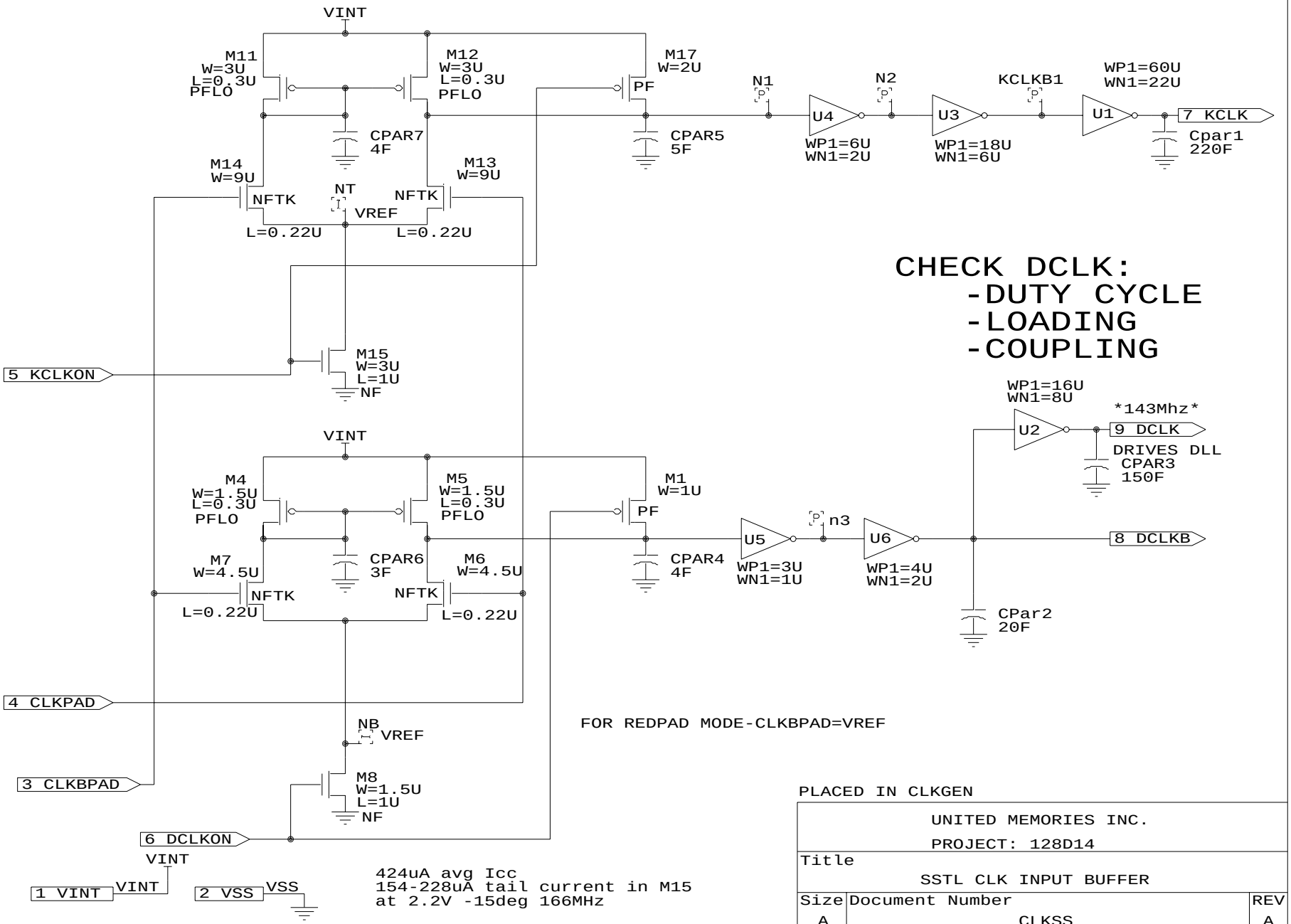
UNITED MEMORIES INC.

PROJECT: 128D14

Title: DRIVER FOR LATCH CLOCKS

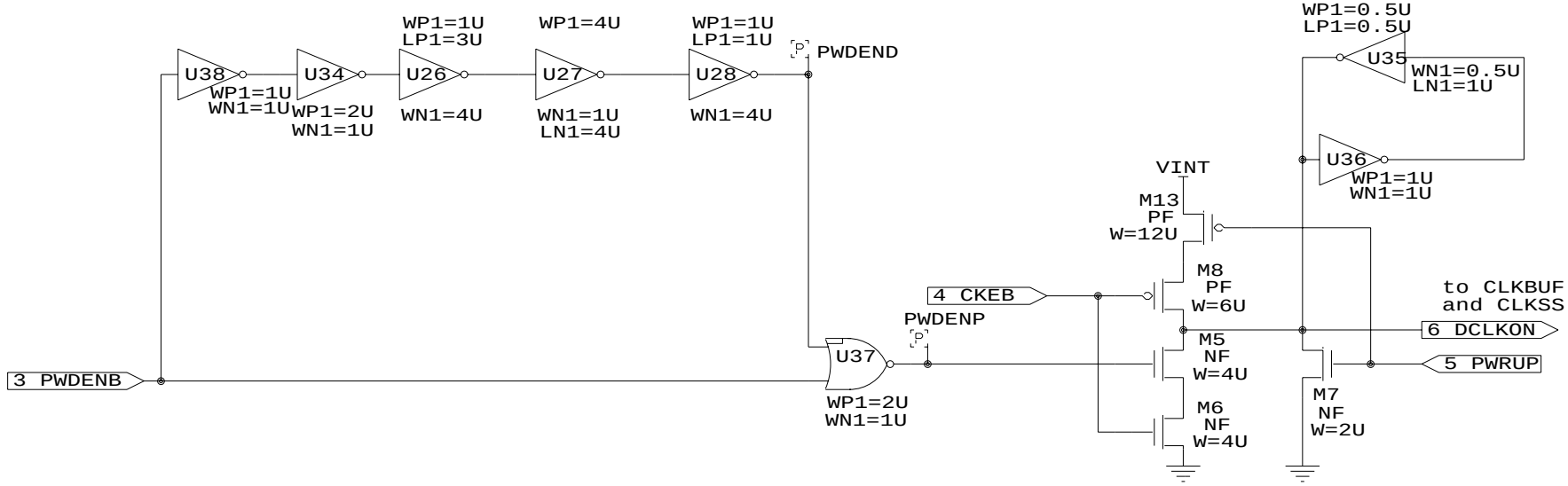
Size	Document Number	REV
B	CLKDRV	A

Date: December 10, 2001 | Sheet 1 of 1

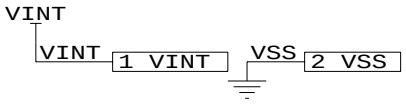


PLACED IN CLKGEN

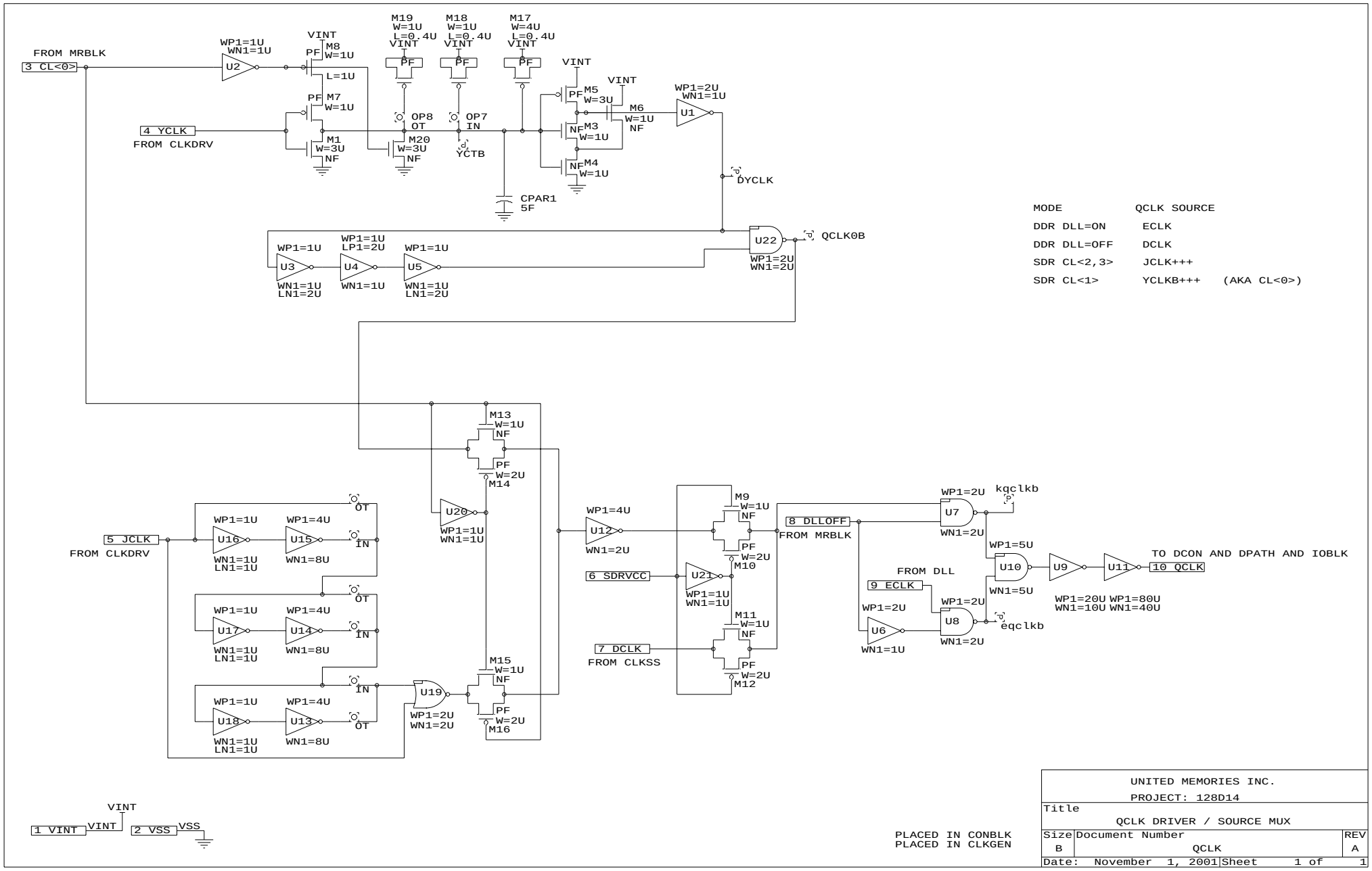
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
SSTL CLK INPUT BUFFER		
Size A	Document Number CLKSS	REV A
Date: October 12, 2001	Sheet 1 of 1	

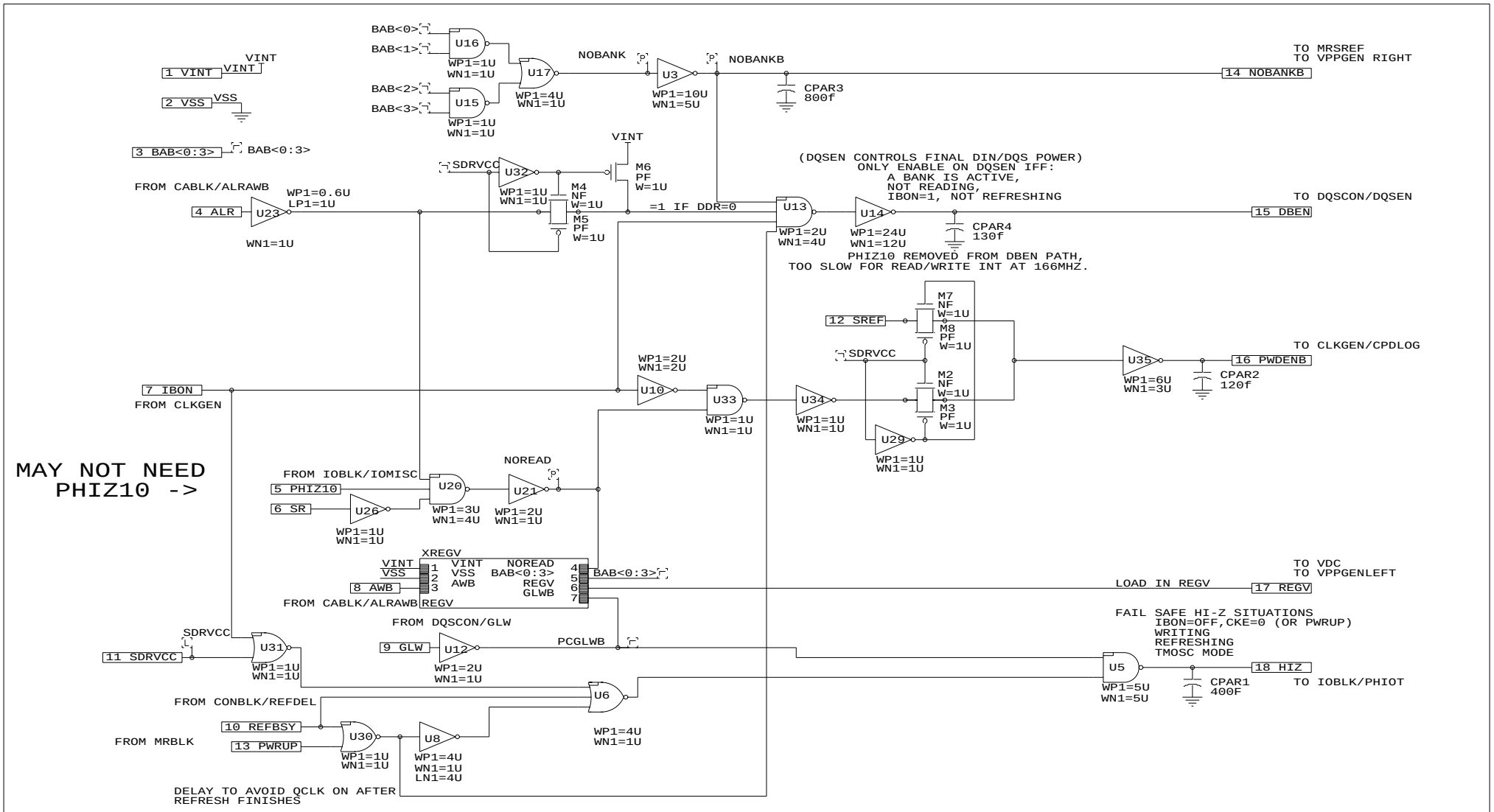


PLACED IN CLKGEN



UNITED MEMORIES INC. PROJECT: 128D14		
Title CLK Power DOWN LOGIC		
Size A	Document Number CPDLOG	REV A
Date: July 9, 2001	Sheet 1 of 1	


FROM MRBLK
3 CL<0>
U2
WP1=1U
WN1=1U
VINT
M8
W=1U
PF
L=1U
PF M7
W=1U
4 YCLK
FROM CLKDRV
M1
W=3U
NF
M19
W=1U
L=0.4U
VINT
PF
M18
W=1U
L=0.4U
VINT
PF
M17
W=4U
L=0.4U
VINT
PF
OP8
OT
M20
W=3U
NF
OP7
IN
YCTB
CPAR1
5F
VINT
PF M5
W=3U
VINT
M6
W=1U
NF
NF M3
W=1U
NF M4
W=1U
WP1=2U
WN1=1U
U1
DYCLK
U22
QCLK0B
WP1=2U
WN1=2U
WP1=1U
U3
WN1=1U
LN1=2U
WP1=1U
LP1=2U
U4
WN1=1U
WP1=1U
U5
WN1=1U
LN1=2U
MODE
QCLK SOURCE
DDR DLL=ON
ECLK
DDR DLL=OFF
DCLK
SDR CL<2,3>
JCLK+++
SDR CL<1>
YCLKB+++
(AKA CL<0>)
M13
W=1U
NF
PF
W=2U
M14
U20
WP1=1U
WN1=1U
5 JCLK
FROM CLKDRV
WP1=1U
U16
WN1=1U
LN1=1U
WP1=4U
U15
WN1=8U
OT
IN
WP1=1U
U17
WN1=1U
LN1=1U
WP1=4U
U14
WN1=8U
OT
IN
WP1=1U
U18
WN1=1U
LN1=1U
WP1=4U
U13
WN1=8U
IN
OT
U19
WP1=2U
WN1=2U
M15
W=1U
NF
PF
W=2U
M16
WP1=4U
U12
WN1=2U
6 SDRVCC
U21
WP1=1U
WN1=1U
7 DCLK
FROM CLKSS
M9
W=1U
NF
PF
W=2U
M10
M11
W=1U
NF
PF
W=2U
M12
8 DLLOFF
FROM MRBLK
WP1=2U
U7
WN1=2U
kqclkb
WP1=5U
U10
WN1=5U
FROM DLL
9 ECLK
WP1=2U
U6
WN1=1U
WP1=2U
U8
WN1=2U
eqclkb
U9
WP1=20U
WN1=10U
U11
WP1=80U
WN1=40U
TO DCON AND DPATH AND IOBLK
10 QCLK
VINT
1 VINT
VINT
2 VSS
VSS
PLACED IN CONBLK
PLACED IN CLKGEN
UNITED MEMORIES INC.
PROJECT: 128D14
Title
QCLK DRIVER / SOURCE MUX
Size
B
Document Number
QCLK
REV
A
Date: November 1, 2001
Sheet 1 of 1



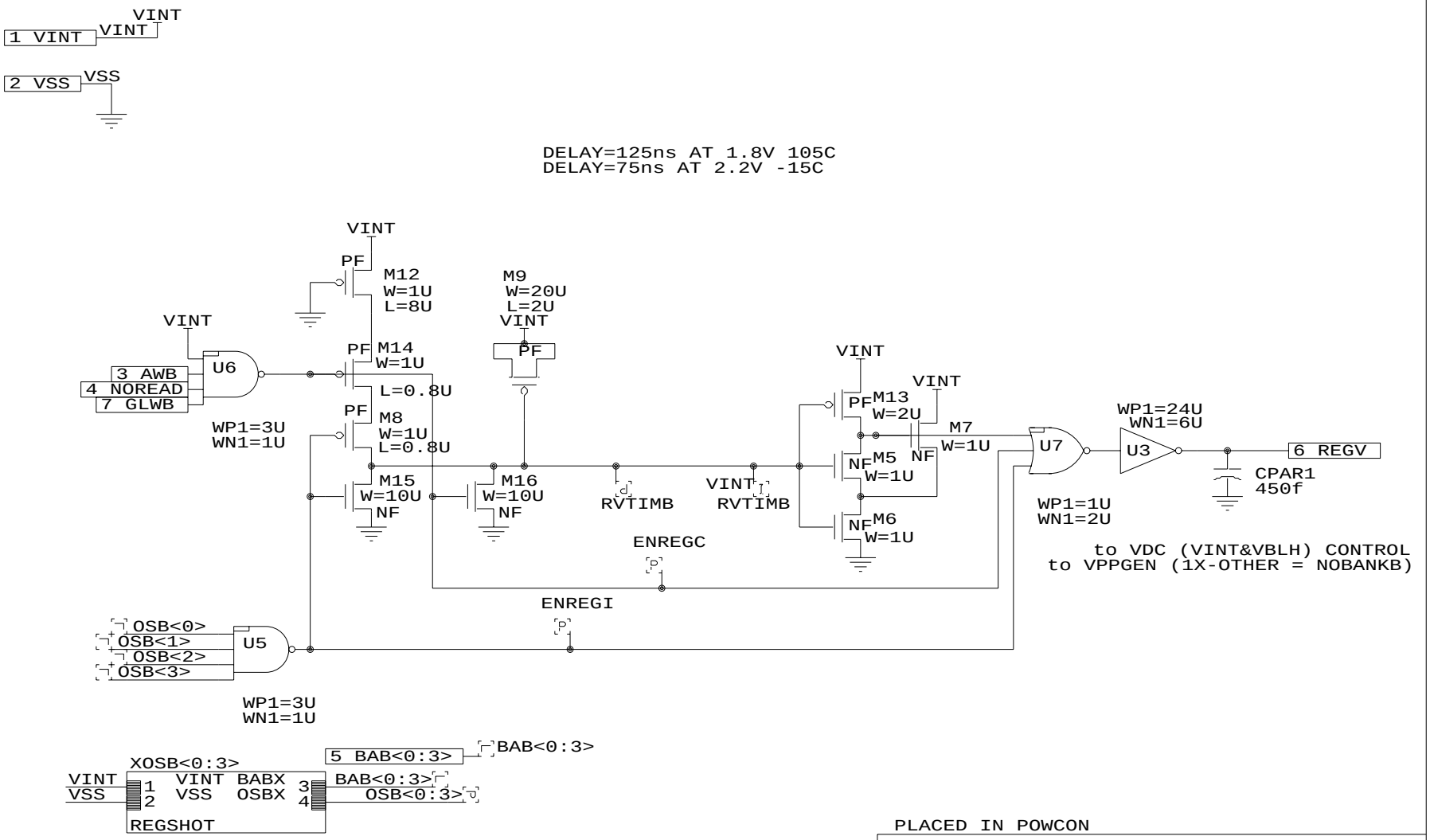
FOR DDR BL-2 MAYBE GAP
IN ALR TO SR, TIMER IS OK
BUT SR=0 FOR SDR

*GLW GOES HIGH THE FASTEST TO START REGV

PLACED IN CONBLK

UNITED MEMORIES INC
PROJECT: 128D14

Title		
POWER CONTROL - REGULATORS/BUFFERS/HIZ		
Size	Document Number	REV
B	POWCON	A
Date: November 5, 2001	Sheet 1 of 1	

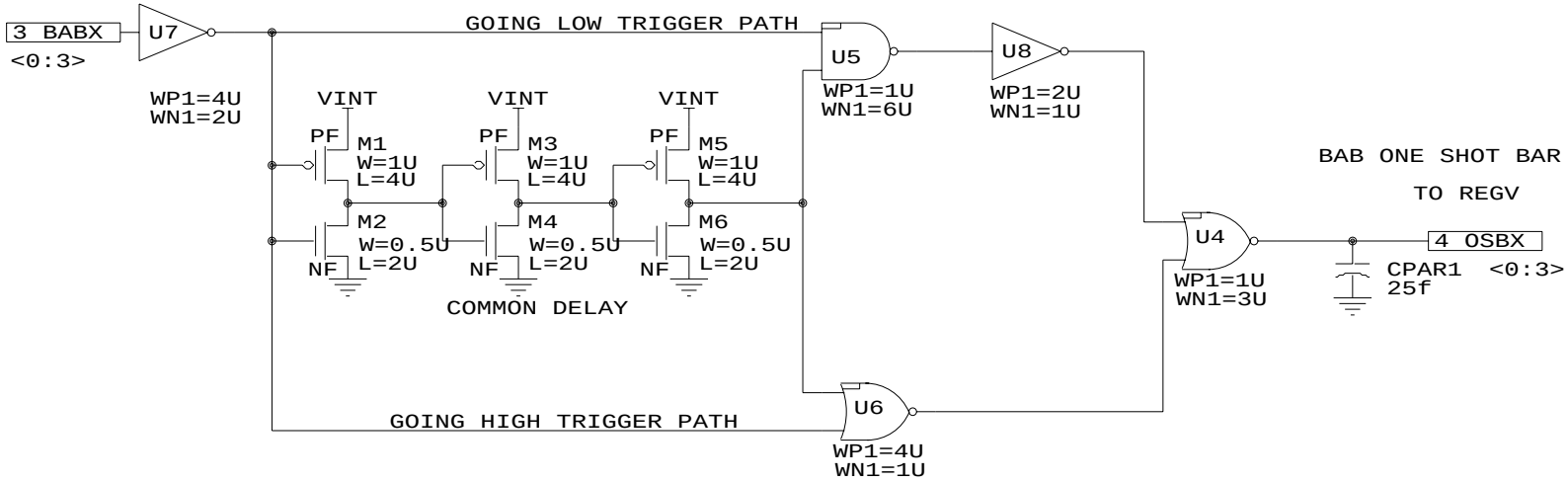


PLACED IN POWCON

ENABLE BOTH VINT AND VBLH REGS AT SAME TIME
ANY BAB TRANSITION EDGE (ACTIVE OR PRECHARGE)
IF READ OR WRITE IS ACTIVE IN STAGE
(MRS COMMANDS-NOT COVERED)

VPP MAY ALSO BE REGULATED FROM THESE SIGNALS

UNITED MEMORIES INC. PROJECT: 128D14		
Title VBLH(1.8V)/VINT(2.0V) + VPP REG ENABLE		
Size A	Document Number REGV	REV A
Date: November 5, 2001	Sheet 1 of 1	

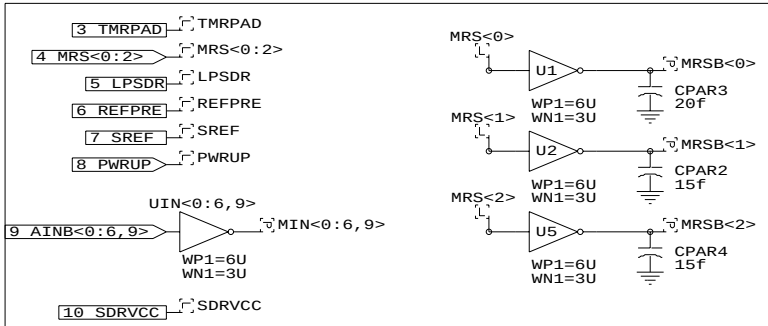


TRIGGERS ON RISING OR FALLING EDGE OF ANY BANK.

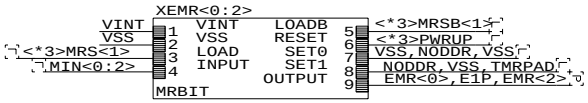
THE FOUR OS'BS ARE COMBINED TO ENABLE REGV.

PLACED IN POWCON
PLACED IN REGV

UNITED MEMORIES INC PROJECT: 128D14		
Title BAB ONE-SHOT FOR VOLTAGE REGULATOR CON		
Size A	Document Number REGSHOT	REV A
Date: August 24, 2001	Sheet 1 of 1	



EXTENDED BITS

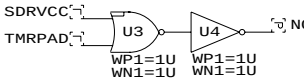


0=DLLOFF
1=IO HALF STRENGTH DRIVE
2=NOTHING (WAS QFC)

6=TEST MODE POWER ENABLE
(TMPEN,ACTIVATES POWER TO
TEST MODE COMMANDS)

ALL MRS/EMRS COMMANDS DISABLED IN REDPAD

SET0 OR SET 1 = TMRPAD

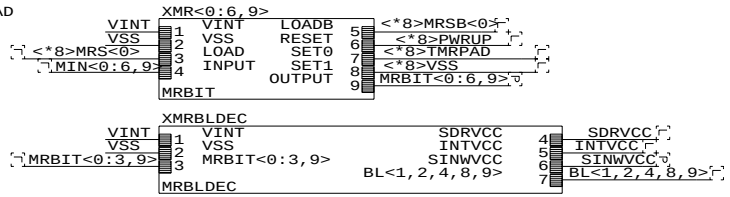


EXT_REG	SET0	SET1	RESULT
0	VSS	NODDR	(DLLOFF!)
1	VSS	NODDR	(HALF STRENGTH)
2	VSS	TMRPAD	(TMPEN, WAS QFC OFF)

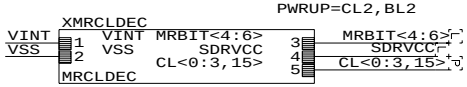
MODE REGISTER BITS

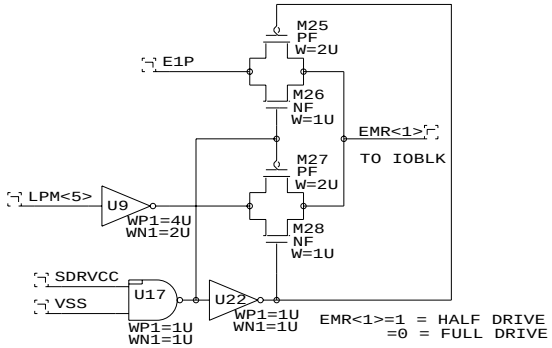
ALL MRS/EMRS COMMANDS DISABLED IN REDPAD
SO....
SET0 OR SET 1 = TMRPAD

MODE_REG	SET0	SET1	RESULT
0	TMRPAD	VSS	(BL1)
1	TMRPAD	VSS	
2	TMRPAD	VSS	(NOT USED)
3	TMRPAD	VSS	SEQUENTIAL
4	TMRPAD	VSS	(CL=2)
5	TMRPAD	VSS	
6	TMRPAD	VSS	



PWRUP=CL2,BL2





EMR<1>=1 = HALF DRIVE
=0 = FULL DRIVE

M1 OPTION TO LPSDR

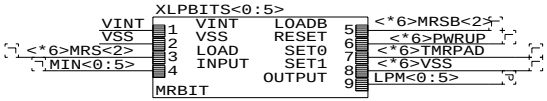
NEED M1/GC CHANGES
IN OUTDRIVE TO
USE THIS FEATURE

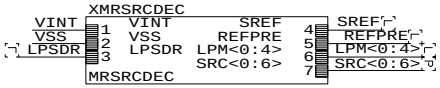
FOR SDR AND LPSDR
LPM<5> IS DRIVE DESIGNATOR

=0 = HALF DRIVE (DEFAULT)
=1 = FULL DRIVE

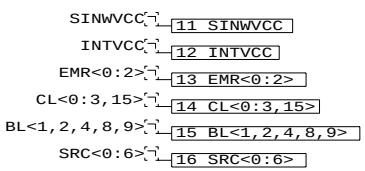
FOR OTHER PARTS, (DDR AND NORM SDR)
E1P=EMR<1>

LOW POWER SDR MODE BITS



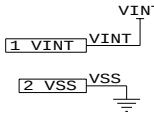


OUTS TO SAVE PORTS,



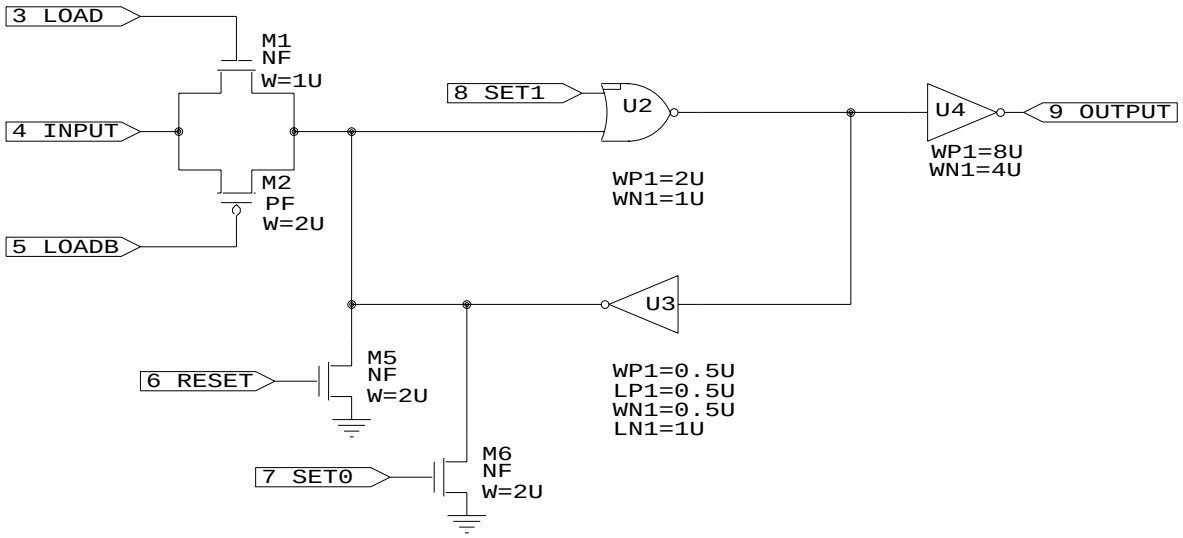
EMR BITS ARE NOT "NAMED"
EMR<0>=DLLOFF
EMR<1>=HALF STRENGTH I/O

EMR<2>=TMPEN



PLACED IN CONBLK

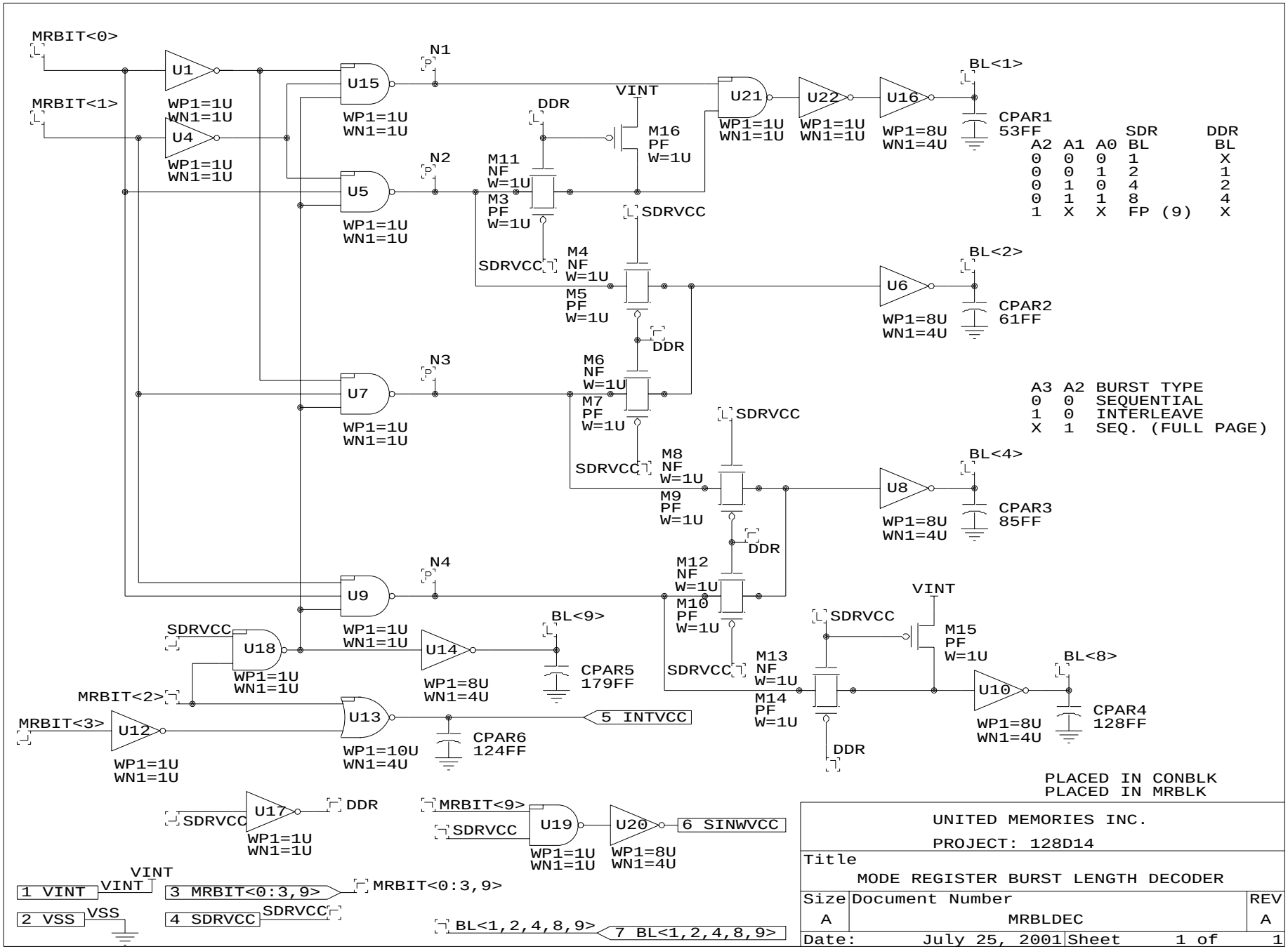
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title: MODE REGISTER BLOCK		
Size: B	Document Number: MRBLK	REV: A
Date: December 6, 2001	Sheet 1 of 1	



SET0/SET1 USED IN TMRPAD
MODE TO SET THE MR/EMR SINCE
THERE IS NO ACCESS TO THE INPUTS
OR MRS COMMANDS IN THIS TEST MODE

PLACED IN MRBLK

UNITED MEMORIES INC. PROJECT: 128D14		
Title MODE REGISTER BIT (NORM & EXTENDED)		
Size A	Document Number MRBIT	REV A
Date: August 24, 2001	Sheet 1 of 1	



A2	A1	A0	SDR BL	DDR BL
0	0	0	1	X
0	0	1	2	1
0	1	0	4	2
0	1	1	8	4
1	X	X	FP (9)	X

A3	A2	BURST TYPE
0	0	SEQUENTIAL
1	0	INTERLEAVE
X	1	SEQ. (FULL PAGE)

PLACED IN CONBLK
PLACED IN MRBLK

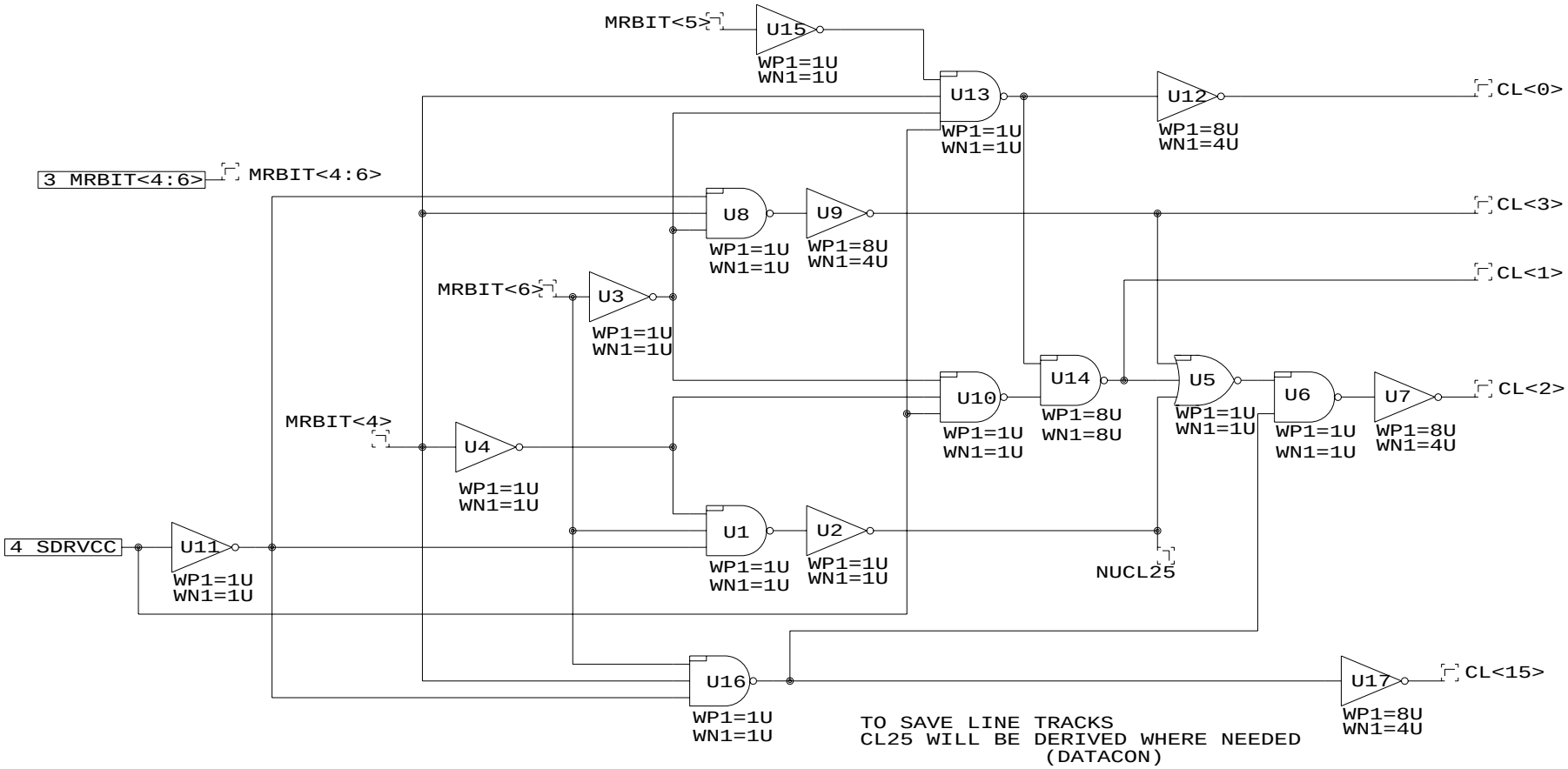
UNITED MEMORIES INC.

PROJECT: 128D14

Title
MODE REGISTER BURST LENGTH DECODER

Size	Document Number	REV
A	MRBLDEC	A

Date: July 25, 2001 Sheet 1 of 1



TO SAVE LINE TRACKS
CL25 WILL BE DERIVED WHERE NEEDED
(DATACON)

CL<0:3,15> 5 CL<0:3,15>

PLACED IN CONBLK
PLACED IN MRBLK

VINT
1 VINT VINT

2 VSS VSS

DDR=1

A6	A5	A4	CL	
0	X	0	2	PWRUP DEFAULT
0	X	1	3	
1	X	0	2.5	
1	X	1	1.5	

SDR=1

A6	A5	A4	CL	CL(DDR)	
0	0	1	1	1 & 0	
0	X	0	2	1	PWRUP DEFAULT
0	1	1	3	2	
1	X	X	2	2	(ILLEGAL-TO COVER ALL CASES)

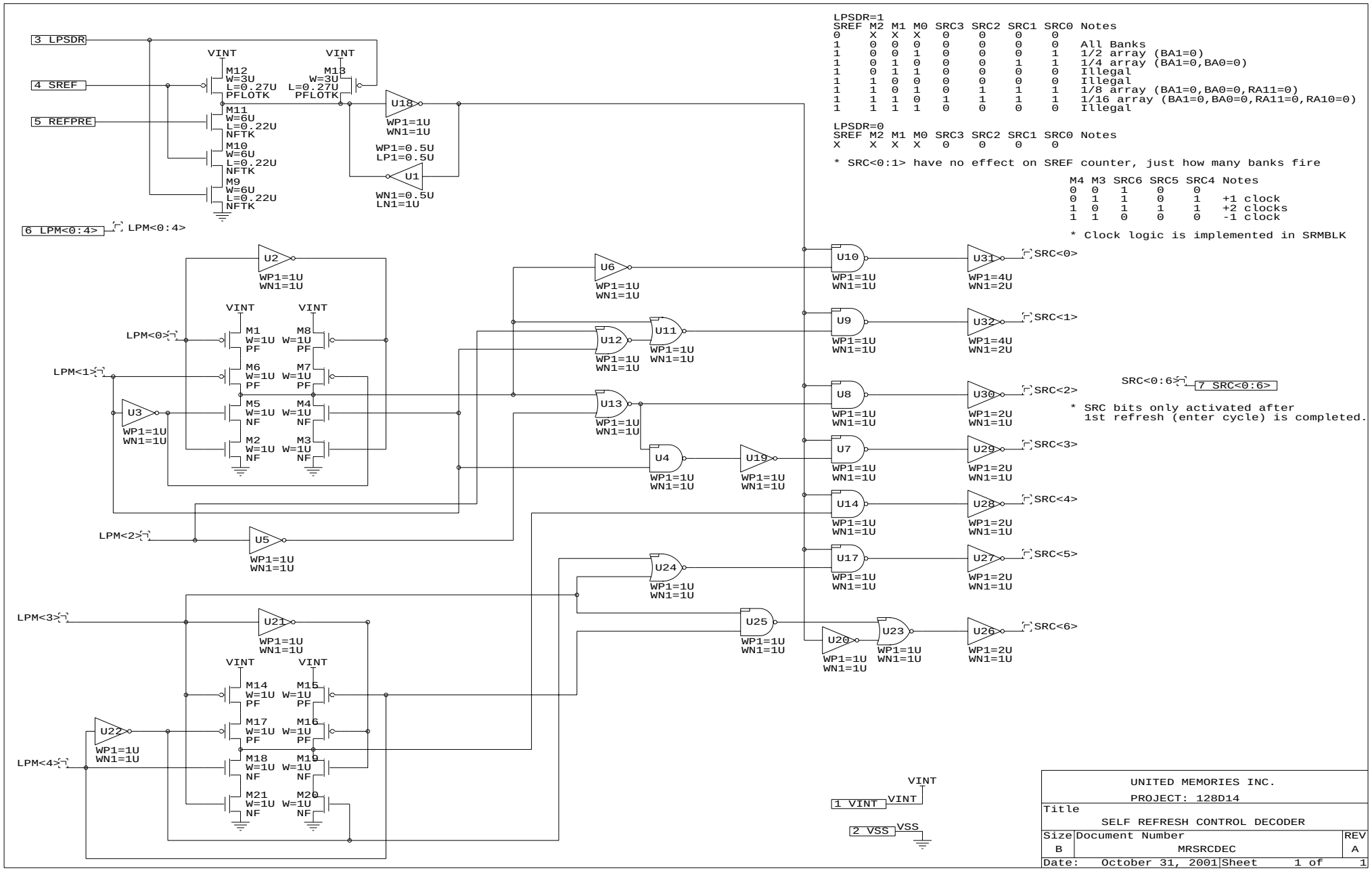
UNITED MEMORIES INC.

PROJECT: 128D14

Title: CAS-LATENCY DECODER

Size	Document Number	REV
A	MRCLDEC	A

Date: December 6, 2001 Sheet 1 of 1



LPSDR=1

SREF	M2	M1	M0	SRC3	SRC2	SRC1	SRC0	Notes
0	X	X	X	0	0	0	0	
1	0	0	0	0	0	0	0	All Banks
1	0	0	1	0	0	0	1	1/2 array (BA1=0)
1	0	1	0	0	0	1	1	1/4 array (BA1=0,BA0=0)
1	0	1	1	0	0	0	0	Illegal
1	1	0	0	0	0	0	0	Illegal
1	1	0	1	0	1	1	1	1/8 array (BA1=0,BA0=0,RA11=0)
1	1	1	0	1	1	1	1	1/16 array (BA1=0,BA0=0,RA11=0,RA10=0)
1	1	1	1	0	0	0	0	Illegal

LPSDR=0

SREF	M2	M1	M0	SRC3	SRC2	SRC1	SRC0	Notes
X	X	X	X	0	0	0	0	

* SRC<0:1> have no effect on SREF counter, just how many banks fire

M4	M3	SRC6	SRC5	SRC4	Notes
0	0	1	0	0	
0	1	1	0	1	+1 clock
1	0	1	1	1	+2 clocks
1	1	0	0	0	-1 clock

* Clock logic is implemented in SRMBLK

* SRC bits only activated after 1st refresh (enter cycle) is completed.

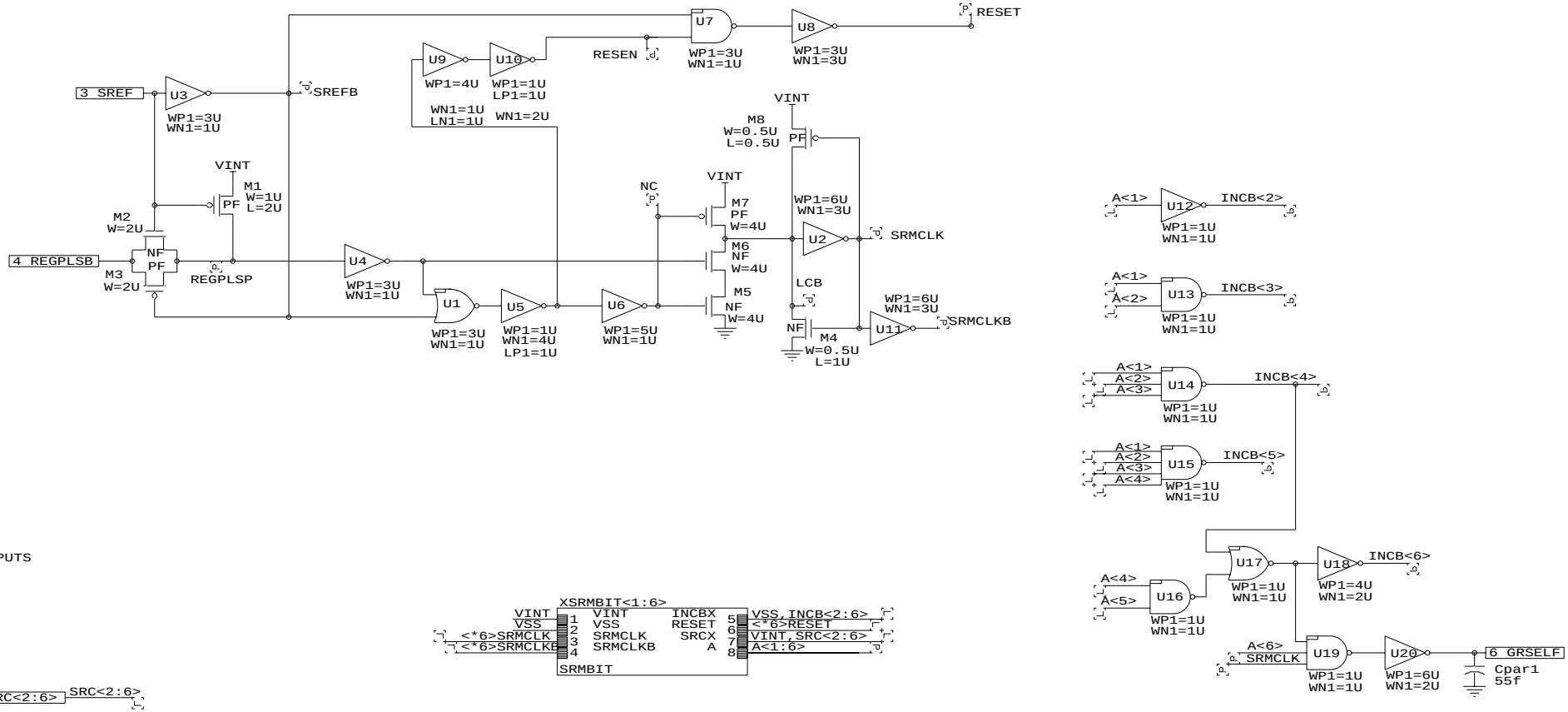
UNITED MEMORIES INC.

PROJECT: 128D14

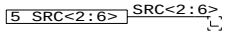
Title: SELF REFRESH CONTROL DECODER

Size	Document Number	REV
B	MRSRCDEC	A

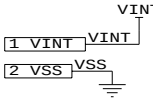
Date: October 31, 2001 | Sheet 1 of 1



INPUTS

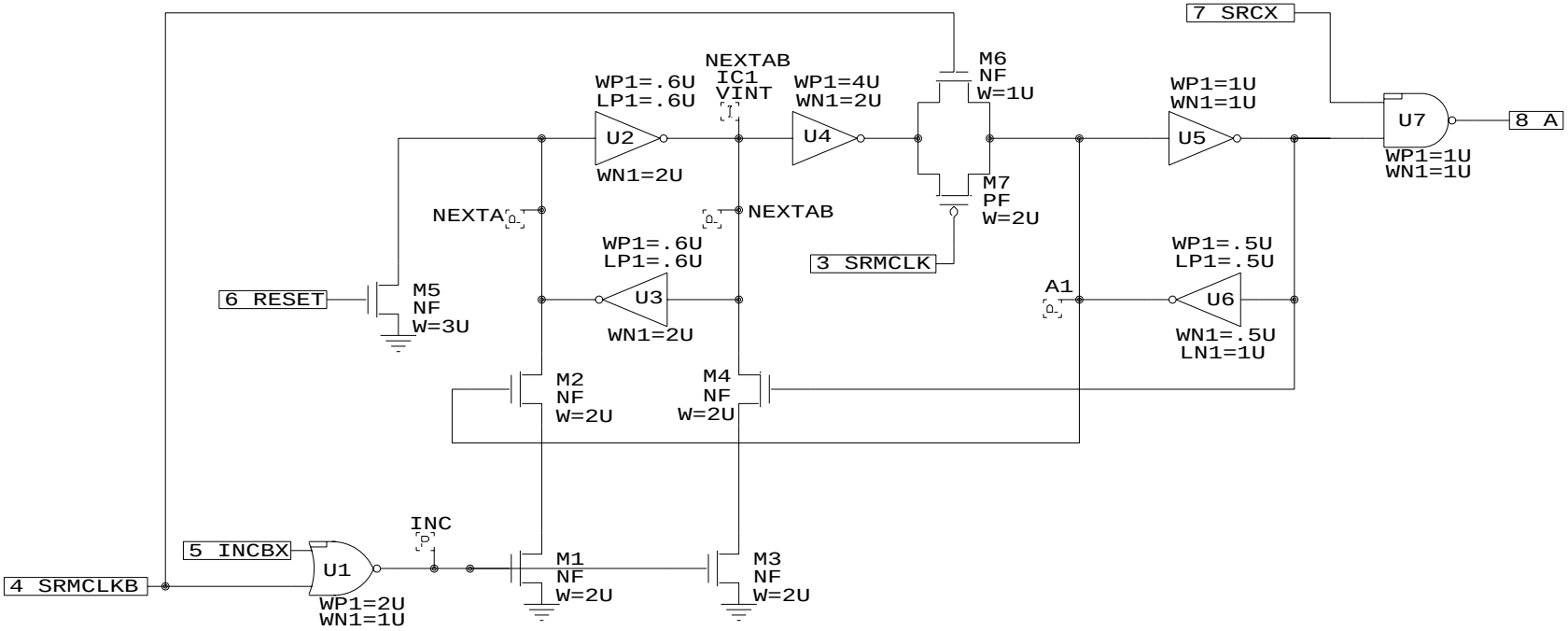


VCCI	Temp	REGPLS period	Refresh** time
2.7v	-5	8.4us	138ms
2.3v	105	13.7us	224ms

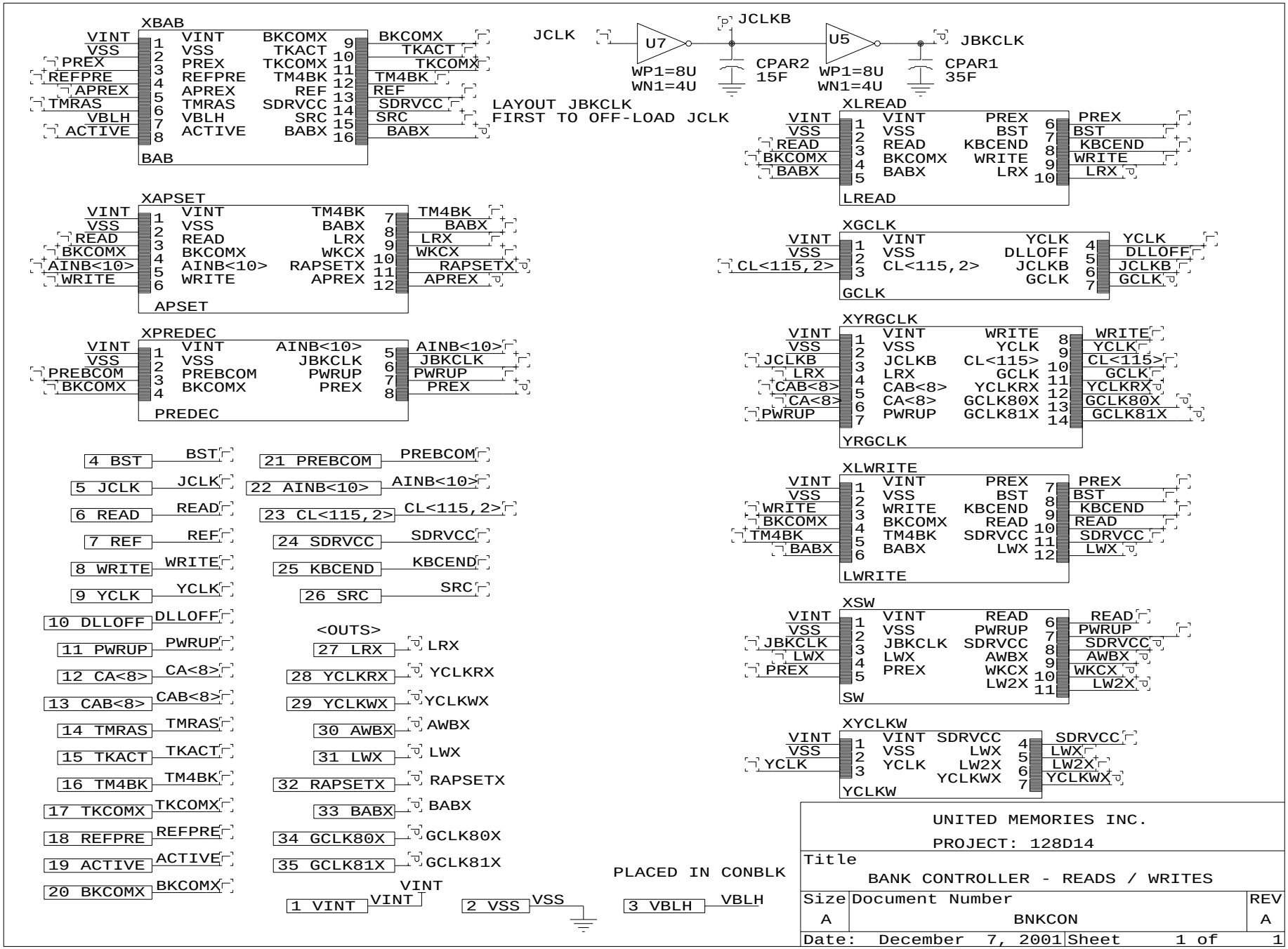


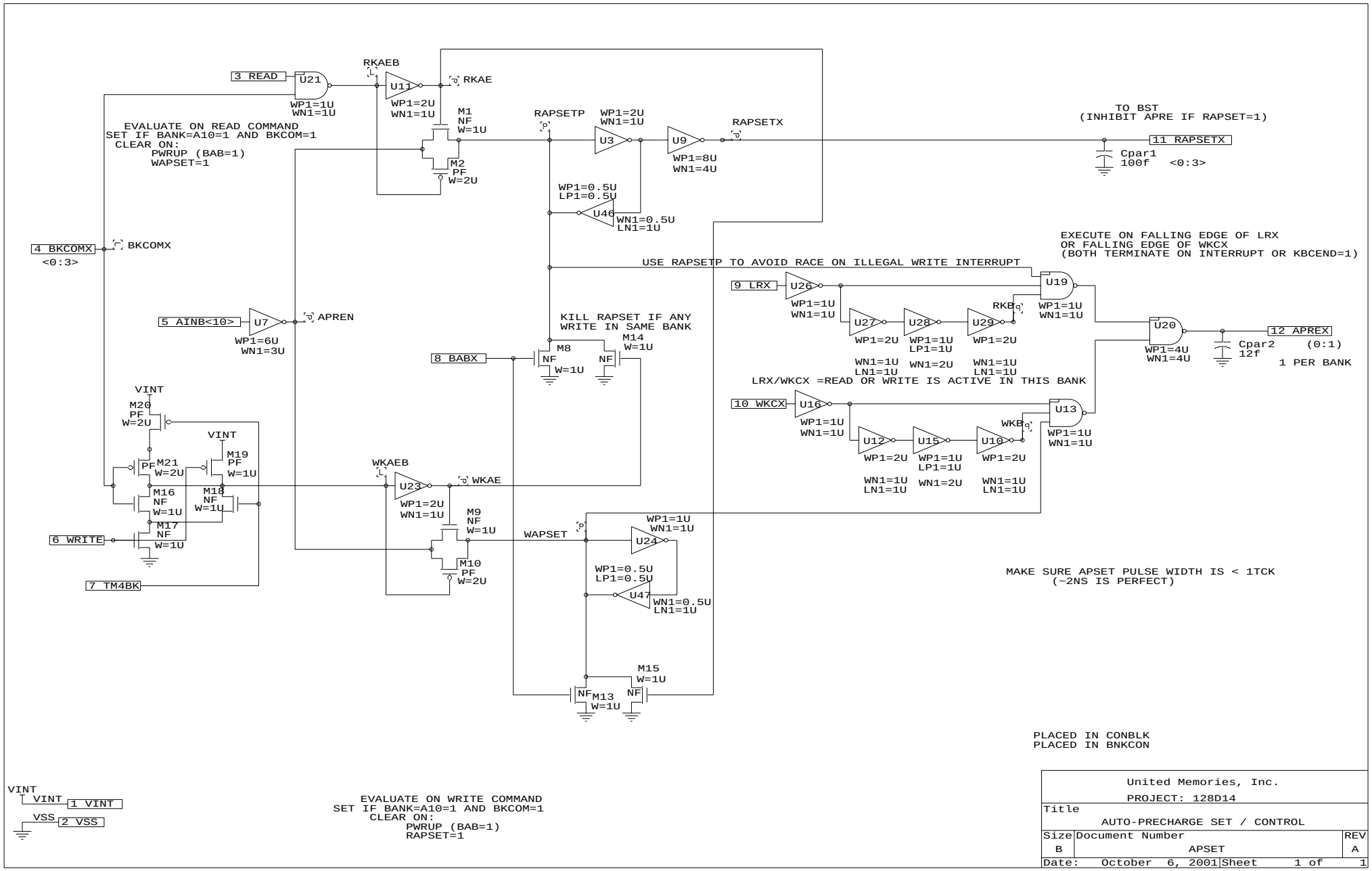
REFRESH EVERY 4 PERIODS
4096 REFRESHES TO COVER ENTIRE PART

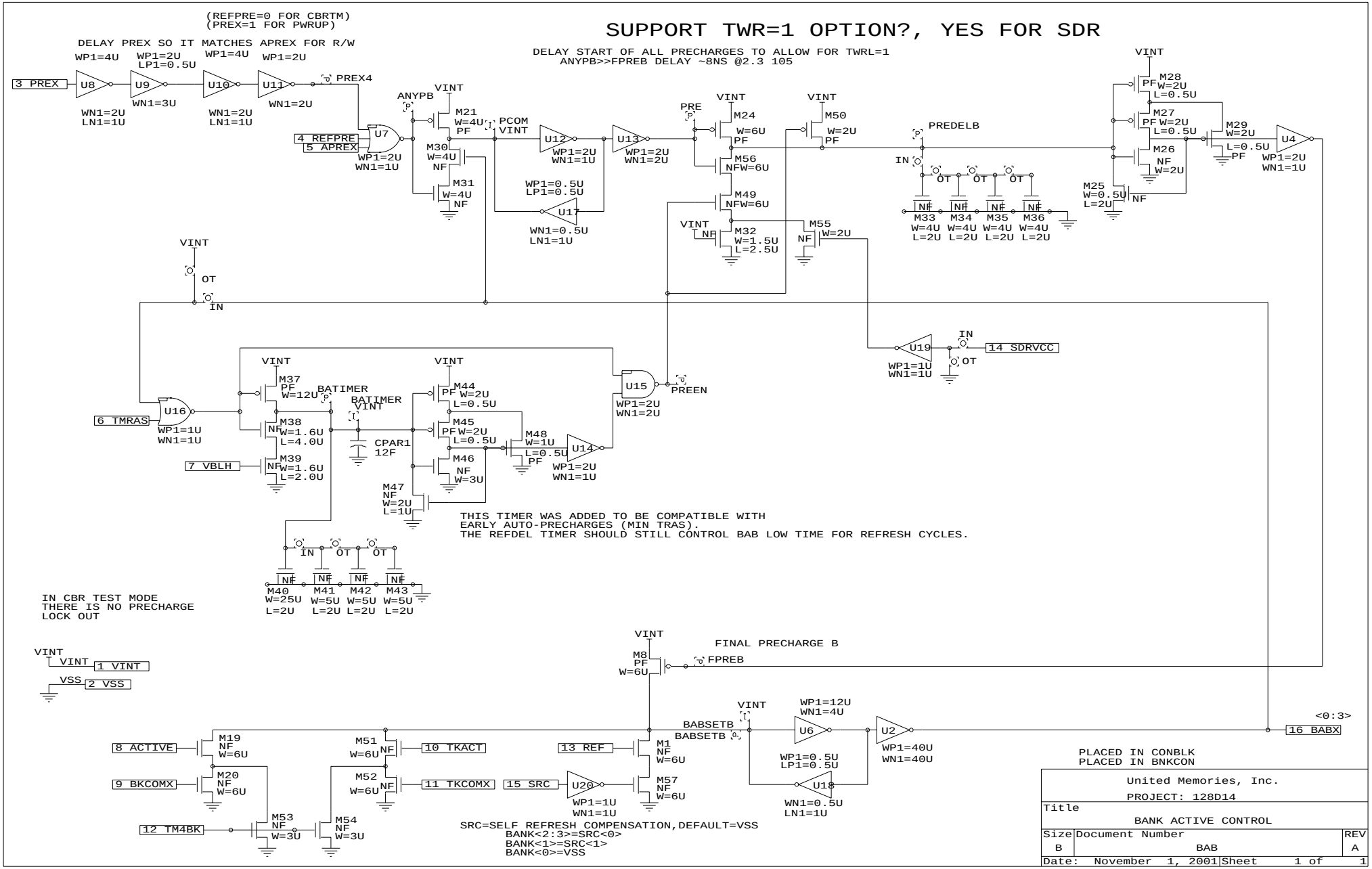
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title	SELF REFRESH MODE BLOCK	
Size B	Document Number SRMBLK	REV A
Date: November 5, 2001	Sheet 1 of 1	

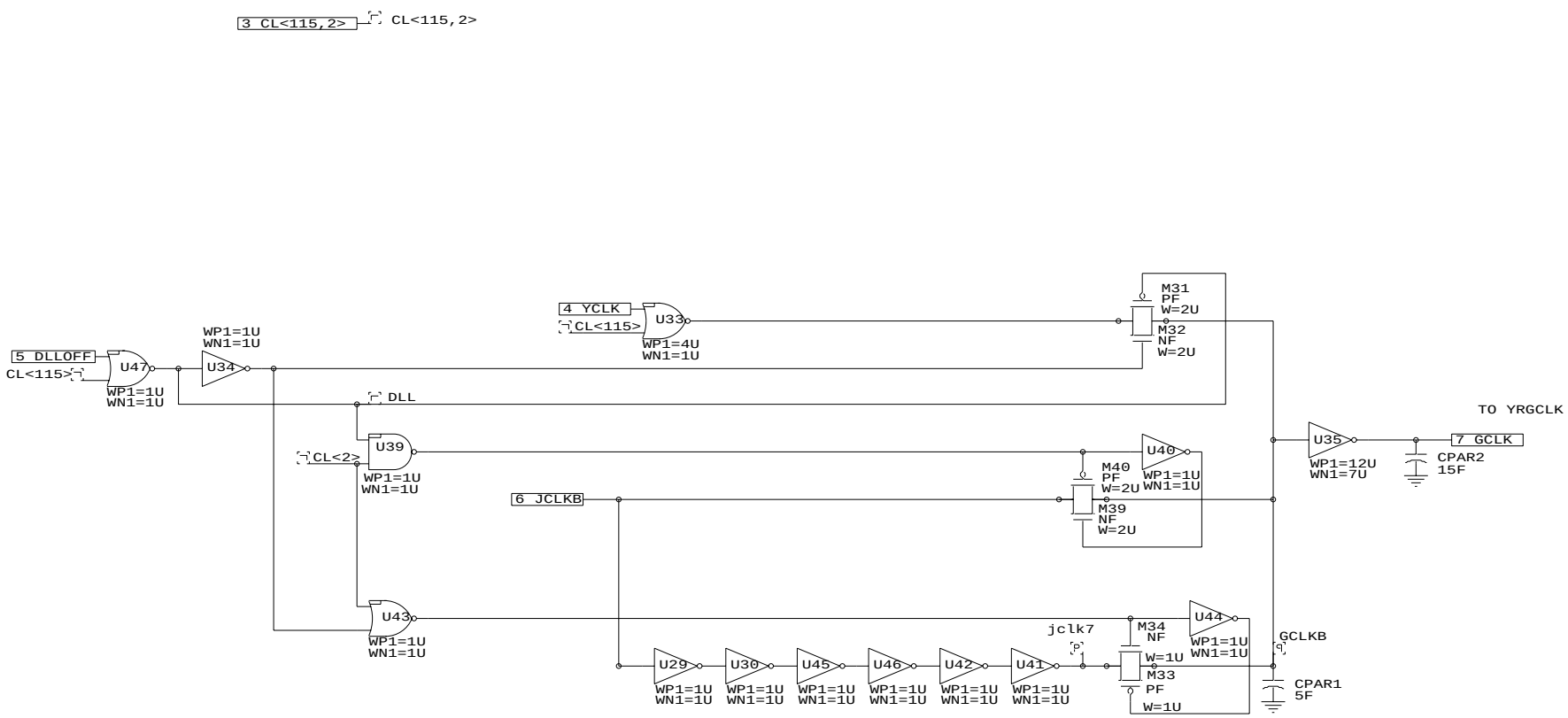


UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
SELF REFRESH MODE BIT COUNTER		
Size	Document Number	REV
A	SRMBIT	A
Date: November 5, 2001	Sheet 1 of 1	


XBAB
VINT VSS PREX REFPRE APREX TMRAS VBLH ACTIVE
VINT VSS PREX REFPRE APREX TMRAS VBLH ACTIVE
BKCOMX TKACT TKCOMX TM4BK REF SDRVCC SRC BABX
BKCOMX TKACT TKCOMX TM4BK REF SDRVCC SRC BABX
BAB
JCLK
U7
WP1=8U
WN1=4U
JCLKB
CPAR2
15F
U5
WP1=8U
WN1=4U
JBKCLK
CPAR1
35F
LAYOUT JBKCLK
FIRST TO OFF-LOAD JCLK
XLREAD
VINT VSS READ BKCOMX BABX
VINT VSS READ BKCOMX BABX
PREX BST KBCEND WRITE LRX
PREX BST KBCEND WRITE LRX
LREAD
XAPSET
VINT VSS READ BKCOMX AINB<10> WRITE
VINT VSS READ BKCOMX AINB<10> WRITE
TM4BK BABX LRX WKCX RAPSETX APREX
TM4BK BABX LRX WKCX RAPSETX APREX
APSET
XGCLK
VINT VSS CL<115,2>
VINT VSS CL<115,2>
YCLK DLLOFF JCLKB GCLK
YCLK DLLOFF JCLKB GCLK
GCLK
XPREDEC
VINT VSS PREBCOM BKCOMX
VINT VSS PREBCOM BKCOMX
AINB<10> JBKCLK PWRUP PREX
AINB<10> JBKCLK PWRUP PREX
PREDEC
XYRGCLK
VINT VSS JCLKB LRX CAB<8> CA<8> PWRUP
VINT VSS JCLKB LRX CAB<8> CA<8> PWRUP
WRITE YCLK CL<115> GCLK YCLKRX GCLK80X GCLK81X
WRITE YCLK CL<115> GCLK YCLKRX GCLK80X GCLK81X
YRGCLK
XLWRITE
VINT VSS WRITE BKCOMX TM4BK BABX
VINT VSS WRITE BKCOMX TM4BK BABX
PREX BST KBCEND READ SDRVCC LWX
PREX BST KBCEND READ SDRVCC LWX
LWRITE
XSW
VINT VSS JBKCLK LWX PREX
VINT VSS JBKCLK LWX PREX
READ PWRUP SDRVCC AWBX WKCX LW2X
READ PWRUP SDRVCC AWBX WKCX LW2X
SW
XYCLKW
VINT VSS YCLK
VINT VSS YCLK
SDRVCC LWX LW2X YCLKWX
SDRVCC LWX LW2X YCLKWX
YCLKW
4 BST BST
5 JCLK JCLK
6 READ READ
7 REF REF
8 WRITE WRITE
9 YCLK YCLK
10 DLLOFF DLLOFF
11 PWRUP PWRUP
12 CA<8> CA<8>
13 CAB<8> CAB<8>
14 TMRAS TMRAS
15 TKACT TKACT
16 TM4BK TM4BK
17 TKCOMX TKCOMX
18 REFPRE REFPRE
19 ACTIVE ACTIVE
20 BKCOMX BKCOMX
21 PREBCOM PREBCOM
22 AINB<10> AINB<10>
23 CL<115,2> CL<115,2>
24 SDRVCC SDRVCC
25 KBCEND KBCEND
26 SRC SRC
<OUTS>
27 LRX LRX
28 YCLKRX YCLKRX
29 YCLKWX YCLKWX
30 AWBX AWBX
31 LWX LWX
32 RAPSETX RAPSETX
33 BABX BABX
34 GCLK80X GCLK80X
35 GCLK81X GCLK81X
1 VINT VINT
2 VSS VSS
PLACED IN CONBLK
3 VBLH VBLH
UNITED MEMORIES INC.
PROJECT: 128D14
Title
BANK CONTROLLER - READS / WRITES
Size A
Document Number
BNKCON
REV A
Date: December 7, 2001
Sheet 1 of 1


3 READ
U21
WP1=1U
WN1=1U
RKAEB
U11
WP1=2U
WN1=1U
RKAE
EVALUATE ON READ COMMAND
SET IF BANK=A10=1 AND BKCOM=1
CLEAR ON:
PWRUP (BAB=1)
WAPSET=1
M1
NF
W=1U
M2
PF
W=2U
RAPSETP
WP1=2U
WN1=1U
U3
U9
WP1=8U
WN1=4U
RAPSETX
TO BST
(INHIBIT APRE IF RAPSET=1)
11 RAPSETX
Cpar1
100f
<0:3>
WP1=0.5U
LP1=0.5U
U46
WN1=0.5U
LN1=1U
4 BKCOMX
<0:3>
BKCOMX
EXECUTE ON FALLING EDGE OF LRX
OR FALLING EDGE OF WKCX
(BOTH TERMINATE ON INTERRUPT OR KBCEND=1)
USE RAPSETP TO AVOID RACE ON ILLEGAL WRITE INTERRUPT
9 LRX
U26
WP1=1U
WN1=1U
U19
WP1=1U
WN1=1U
RKB
U27
U28
U29
WP1=2U
WP1=1U
LP1=1U
WP1=2U
WN1=1U
LN1=1U
WN1=2U
WN1=1U
LN1=1U
5 AINB<10>
U7
WP1=6U
WN1=3U
APREN
KILL RAPSET IF ANY
WRITE IN SAME BANK
M14
W=1U
M8
NF
W=1U
8 BABX
U20
WP1=4U
WN1=4U
12 APREX
Cpar2
12f
(0:1)
1 PER BANK
LRX/WKCX =READ OR WRITE IS ACTIVE IN THIS BANK
10 WKCX
U16
WP1=1U
WN1=1U
U13
WP1=1U
WN1=1U
WKB
U12
U15
U10
WP1=2U
WP1=1U
LP1=1U
WP1=2U
WN1=1U
LN1=1U
WN1=2U
WN1=1U
LN1=1U
VINT
M20
PF
W=2U
VINT
M19
PF
W=1U
PF
M21
W=2U
M16
NF
W=1U
M18
NF
W=1U
M17
NF
W=1U
6 WRITE
7 TM4BK
WKAEB
U23
WP1=2U
WN1=1U
WKAE
M9
NF
W=1U
M10
PF
W=2U
WAPSET
WP1=1U
WN1=1U
U24
WP1=0.5U
LP1=0.5U
U47
WN1=0.5U
LN1=1U
MAKE SURE APSET PULSE WIDTH IS < 1TCK
(~2NS IS PERFECT)
M15
W=1U
NF
M13
W=1U
NF
PLACED IN CONBLK
PLACED IN BNKCON
VINT
VINT
1 VINT
VSS
2 VSS
EVALUATE ON WRITE COMMAND
SET IF BANK=A10=1 AND BKCOM=1
CLEAR ON:
PWRUP (BAB=1)
RAPSET=1
United Memories, Inc.
PROJECT: 128D14
Title
AUTO-PRECHARGE SET / CONTROL
Size
B
Document Number
APSET
REV
A
Date: October 6, 2001
Sheet 1 of 1


SUPPORT TWR=1 OPTION?, YES FOR SDR
(REFPRE=0 FOR CBRTM)
(PREX=1 FOR PWRUP)
DELAY PREX SO IT MATCHES APREX FOR R/W
DELAY START OF ALL PRECHARGES TO ALLOW FOR TWRL=1
ANYPB>>FPREB DELAY ~8NS @2.3 105
3 PREX
U8
U9
U10
U11
PREX4
4 REFPRE
5 APREX
U7
ANYPB
VINT
M21
M30
M31
PCOM
U12
U13
U17
PRE
M24
M56
M49
M32
M50
M55
PREDELB
IN
OT
M33
M34
M35
M36
M28
M27
M26
M25
M29
U4
U19
14 SDRVCC
U15
PREEN
U16
6 TMRAS
7 VBLH
M37
M38
M39
BATIMER
CPAR1
12F
M44
M45
M46
M47
M48
U14
THIS TIMER WAS ADDED TO BE COMPATIBLE WITH
EARLY AUTO-PRECHARGES (MIN TRAS).
THE REFDEL TIMER SHOULD STILL CONTROL BAB LOW TIME FOR REFRESH CYCLES.
M40
M41
M42
M43
IN CBR TEST MODE
THERE IS NO PRECHARGE
LOCK OUT
1 VINT
VSS
2 VSS
FINAL PRECHARGE B
M8
FPREB
BABSETB
U6
U2
U18
U20
<0:3>
16 BABX
8 ACTIVE
9 BKCOMX
12 TM4BK
M19
M20
M53
M54
M51
M52
10 TKACT
11 TKCOMX
13 REF
15 SRC
M1
M57
SRC=SELF REFRESH COMPENSATION,DEFAULT=VSS
BANK<2:3>=SRC<0>
BANK<1>=SRC<1>
BANK<0>=VSS
PLACED IN CONBLK
PLACED IN BNKCON
United Memories, Inc.
PROJECT: 128D14
Title
BANK ACTIVE CONTROL
Size B
Document Number
BAB
REV A
Date: November 1, 2001
Sheet 1 of 1



ANY DLL-OFF GCLK=YCLK

SDR CL2 (CL<1>) GCLK=DC ON

CL3/DLLON GCLK=JCLK+++

CL2/DLLON GCLK=JCLK+

PLACED IN CONBLK
PLACED IN BNKCON

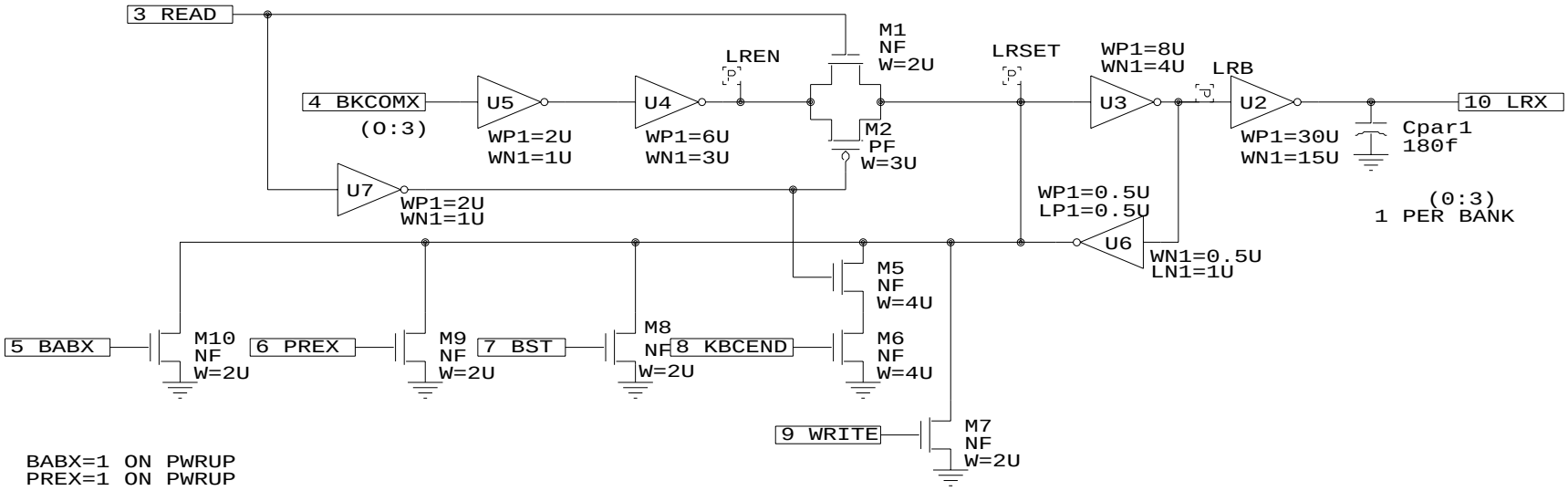
VINT
VINT 1 VINT
VSS 2 VSS

United Memories, Inc.		
PROJECT: 128D14		
Title GCLK GENERATION		
Size B	Document Number GCLK	REV A
Date: December 7, 2001	Sheet 1 of 1	

SET LR ON READ COMMAND IF BANK ADDRESS IS MATCH
(IFF BABX=0=ACTIVE)

TERMINATE ON : PREX
BST
WRITE(EMERGENCY ABORT)
READ (TO OTHER BANK)
KBCEND=NORMAL BURST END(CLOCKED BCEND)

READ COMMAND DISABLED DURING REFRESH CYCLES



BABX=1 ON PWRUP
PREX=1 ON PWRUP

PLACED IN CONBLK
PLACED IN BNKCON

VINT
VINT 1 VINT
VSS 2 VSS

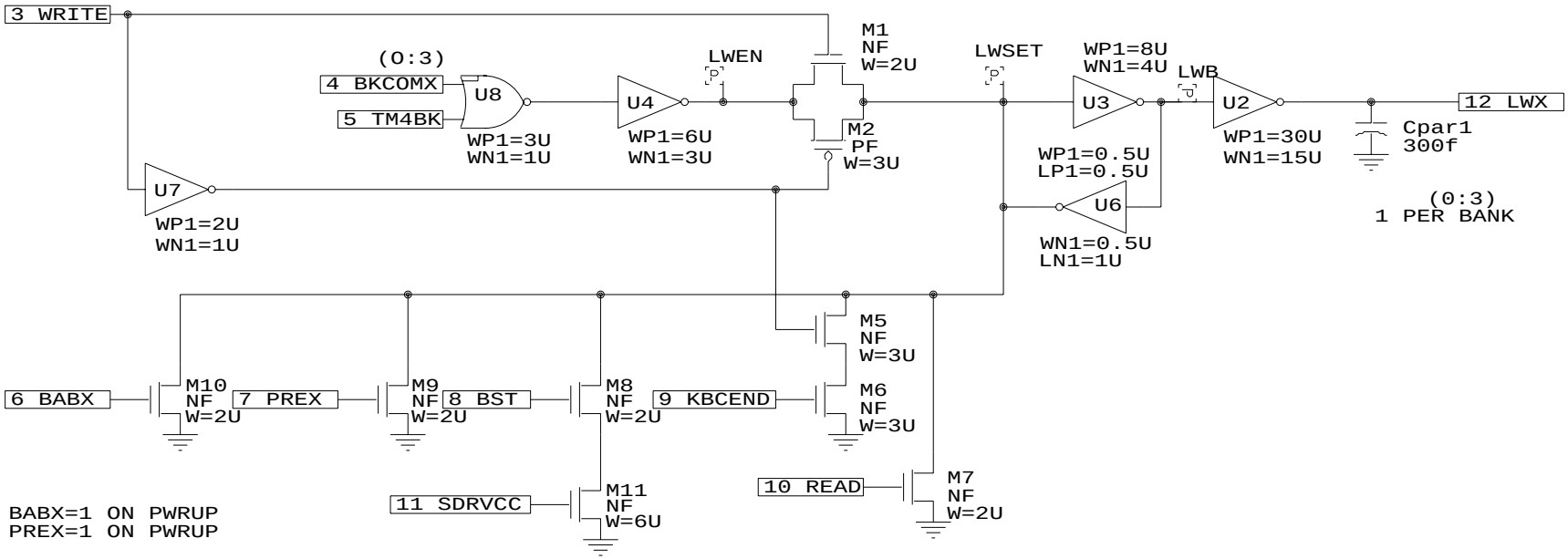
United Memories, Inc. PROJECT: 128D14		
Title LATCHED READ COMMAND GENERATION		
Size A	Document Number LREAD	REV A
Date: October 6, 2001	Sheet 1 of 1	

SET LW ON WRITE COMMAND IF BANK ADDRESS IS MATCH
(IFF BABX=0=ACTIVE)

TERMINATE ON : PREX
READ(EMERGENCY ABORT)
WRITE (TO OTHER BANK)
KBCEND=NORMAL BURST END

BST (NOW DISABLED)

WRITE COMMAND DISABLED DURING REFRESH CYCLES

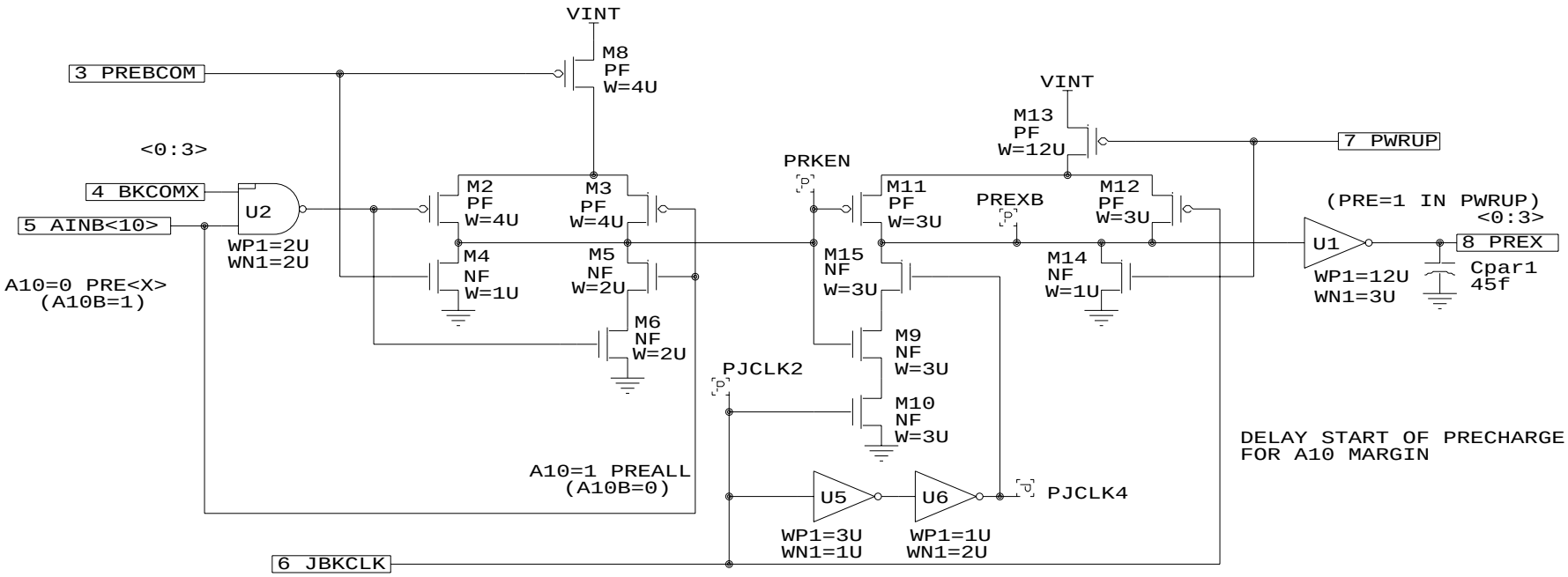


BABX=1 ON PWRUP
PREX=1 ON PWRUP

PLACED IN CONBLK
PLACED IN BNKCON

VINT
VINT 1 VINT
VSS 2 VSS

United Memories, Inc. PROJECT: 128D14		
Title LATCHED WRITE CONTROLLER		
Size A	Document Number LWRITE	REV A
Date: October 6, 2001	Sheet 1 of 1	

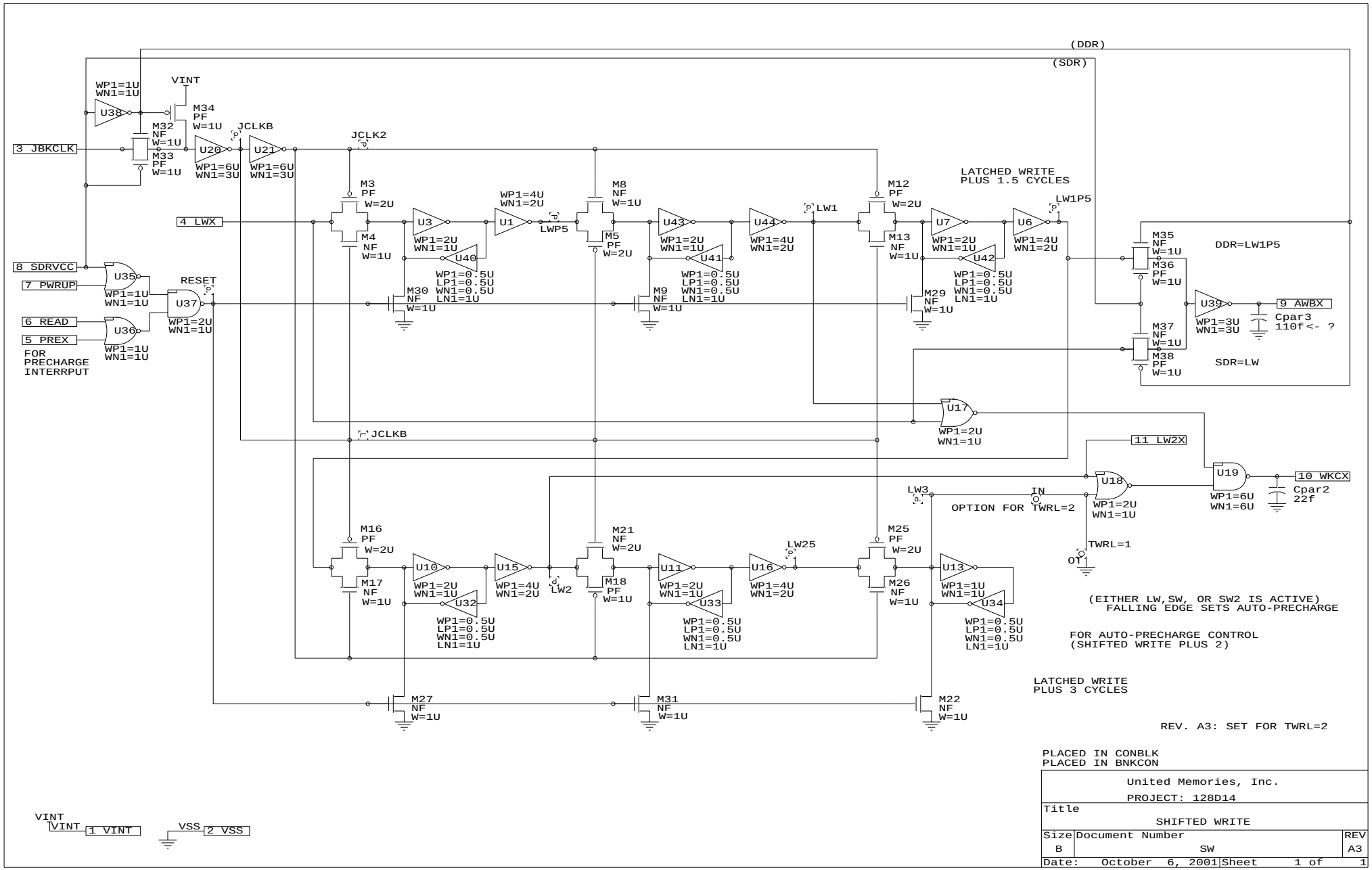


VINT
VINT 1 VINT

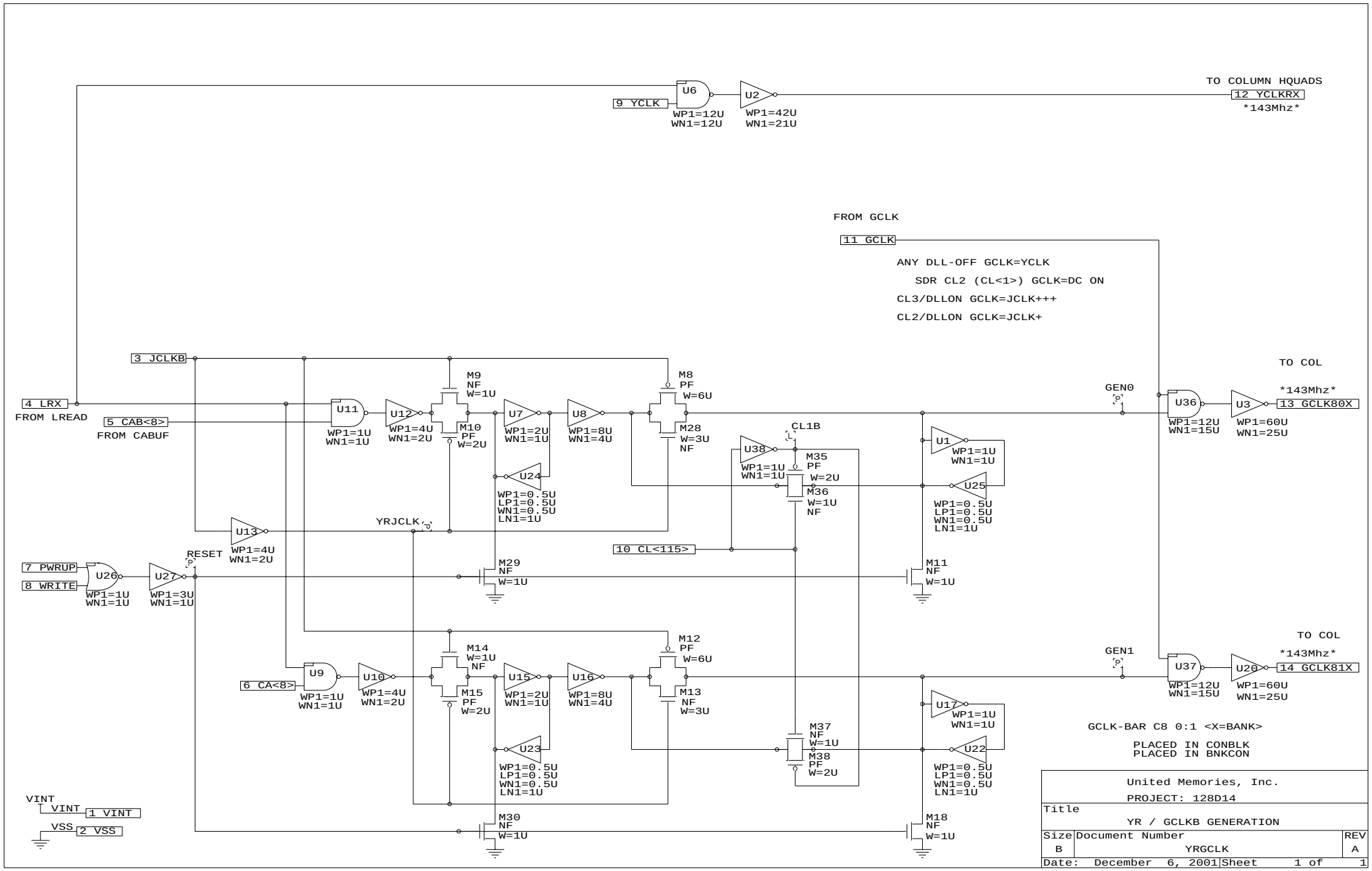
VSS 2 VSS

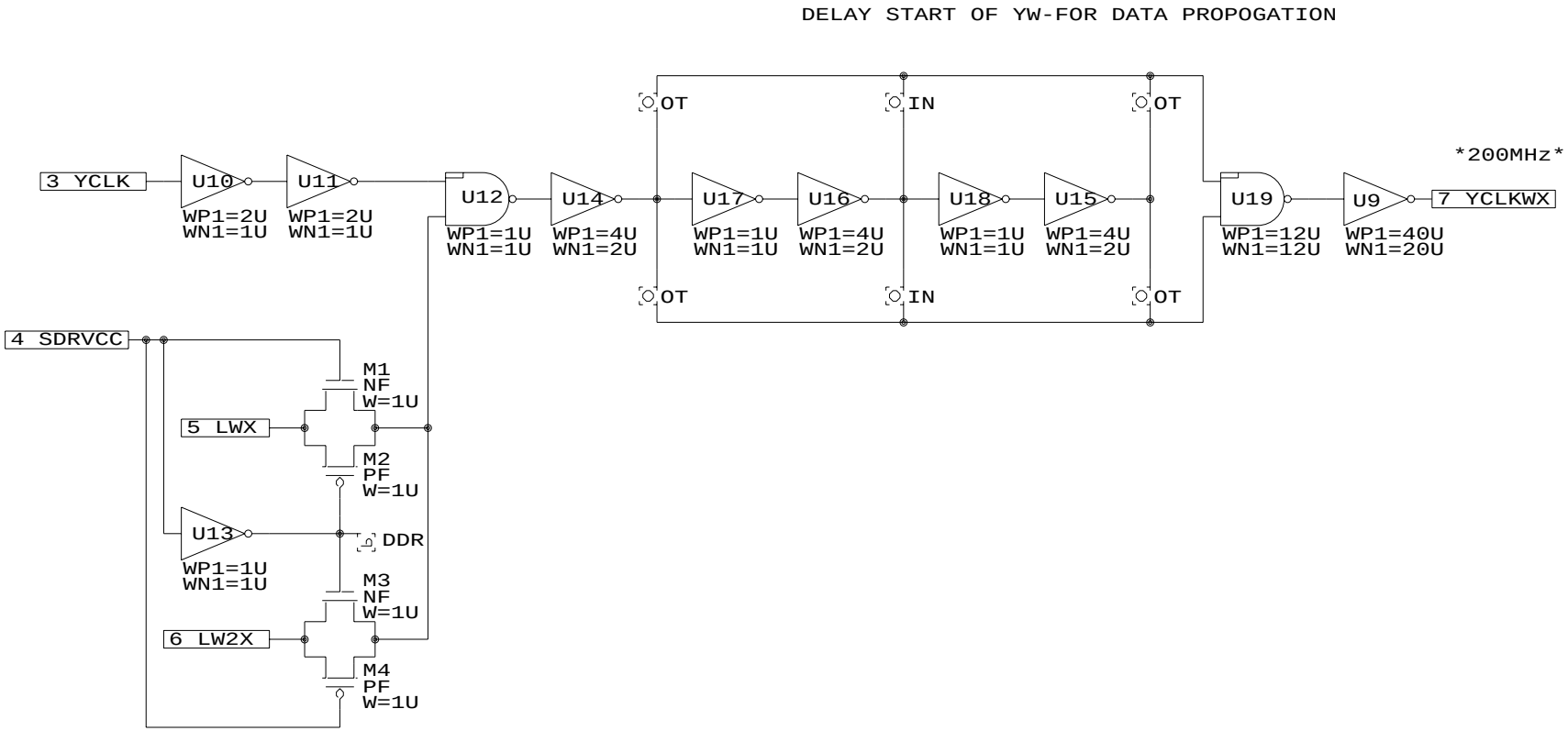
PLACED IN CONBLK
PLACED IN BNKCON

United Memories, Inc. PROJECT: 128D14		
Title BANK PRECHARGE COMMAND GENERATION		
Size A	Document Number PREDEC	REV A
Date: October 6, 2001	Sheet 1 of 1	



United Memories, Inc.		
PROJECT: 128D14		
Title SHIFTED WRITE		
Size B	Document Number SW	REV A3
Date: October 6, 2001	Sheet 1 of 1	


TO COLUMN HQUADS
12 YCLKRX
143Mhz
9 YCLK
U6
WP1=12U
WN1=12U
U2
WP1=42U
WN1=21U
FROM GCLK
11 GCLK
ANY DLL-OFF GCLK=YCLK
SDR CL2 (CL<1>) GCLK=DC ON
CL3/DLLON GCLK=JCLK+++
CL2/DLLON GCLK=JCLK+
3 JCLKB
4 LRX
FROM LREAD
5 CAB<8>
FROM CABUF
U11
WP1=1U
WN1=1U
U12
WP1=4U
WN1=2U
M9
NF
W=1U
M10
PF
W=2U
U7
WP1=2U
WN1=1U
U8
WP1=8U
WN1=4U
M8
PF
W=6U
M28
W=3U
NF
U24
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
YRJCLK
U13
WP1=4U
WN1=2U
RESET
7 PWRUP
8 WRITE
U26
WP1=1U
WN1=1U
U27
WP1=3U
WN1=1U
M29
NF
W=1U
10 CL<115>
CL1B
U38
WP1=1U
WN1=1U
M35
PF
W=2U
M36
W=1U
NF
U1
WP1=1U
WN1=1U
U25
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
M11
NF
W=1U
GEN0
U36
WP1=12U
WN1=15U
U3
WP1=60U
WN1=25U
TO COL
143Mhz
13 GCLK80X
6 CA<8>
U9
WP1=1U
WN1=1U
U10
WP1=4U
WN1=2U
M14
W=1U
NF
M15
PF
W=2U
U15
WP1=2U
WN1=1U
U16
WP1=8U
WN1=4U
M12
PF
W=6U
M13
NF
W=3U
U23
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
M37
NF
W=1U
M38
PF
W=2U
U17
WP1=1U
WN1=1U
U22
WP1=0.5U
LP1=0.5U
WN1=0.5U
LN1=1U
M30
NF
W=1U
M18
NF
W=1U
GEN1
U37
WP1=12U
WN1=15U
U20
WP1=60U
WN1=25U
TO COL
143Mhz
14 GCLK81X
GCLK-BAR C8 0:1 <X=BANK>
PLACED IN CONBLK
PLACED IN BNKCON
VINT
VINT
1 VINT
VSS
2 VSS
United Memories, Inc.
PROJECT: 128D14
Title
YR / GCLKB GENERATION
Size
B
Document Number
YRGCLK
REV
A
Date: December 6, 2001
Sheet 1 of 1

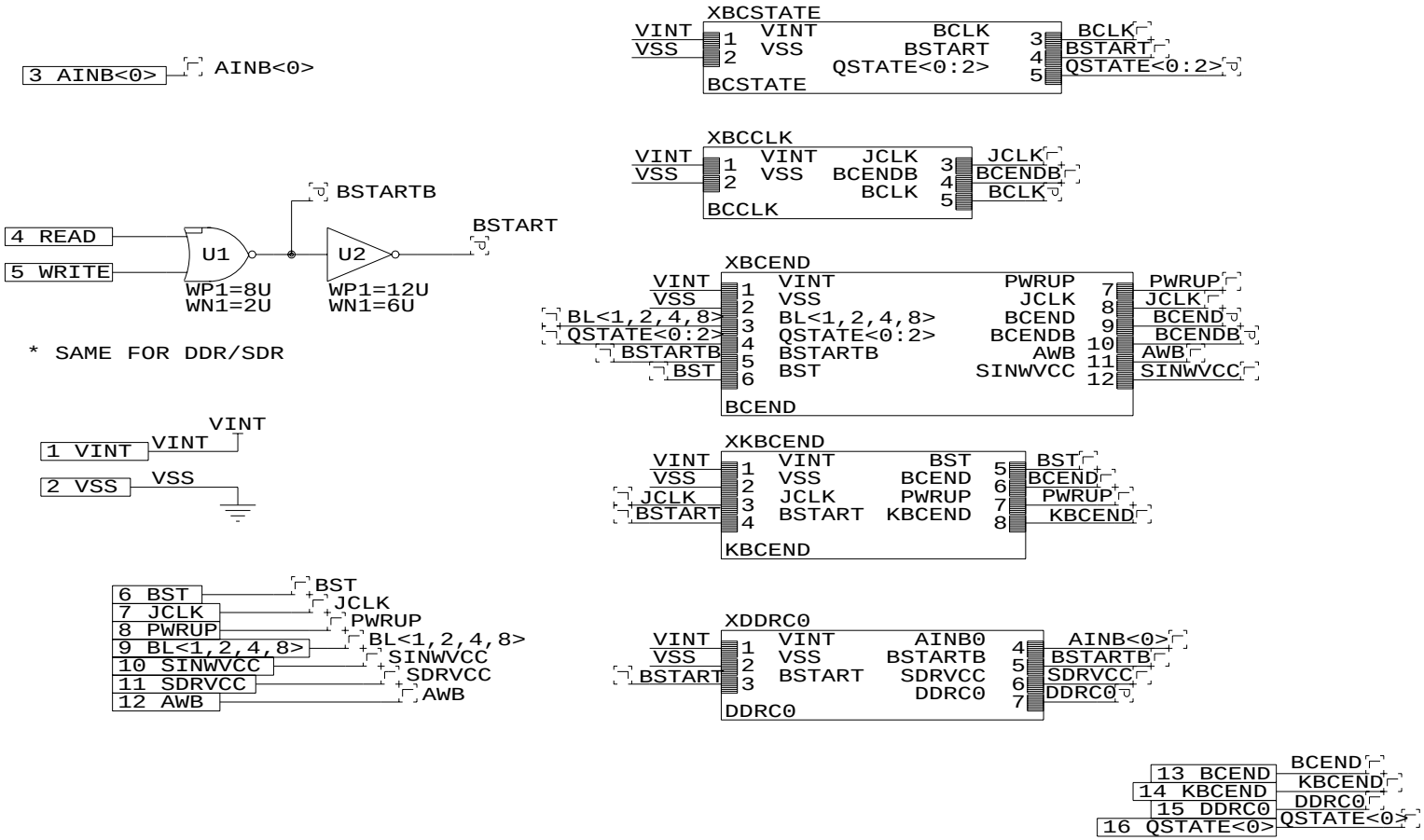


PLACED IN CONBLK
PLACED IN BNKCON

VINT
VINT 1 VINT

VSS 2 VSS

United Memories, Inc. PROJECT: 128D14		
Title YCLK-WRITE GENERATION		
Size A	Document Number YCLKW	REV A
Date: July 6, 2001	Sheet 1 of 1	



Description: THIS CIRCUIT ONLY COUNTS THE BURST LENGTH FOR THE CONTROLLER.
SINCE READS AND WRITES HAPPEN AT DIFFERENT TIMES,
ALL COLUMN COUNTING AND INCREMENTING IS HANDLED SEPARATELY

NEW FOR S14, PLACED IN CABLK

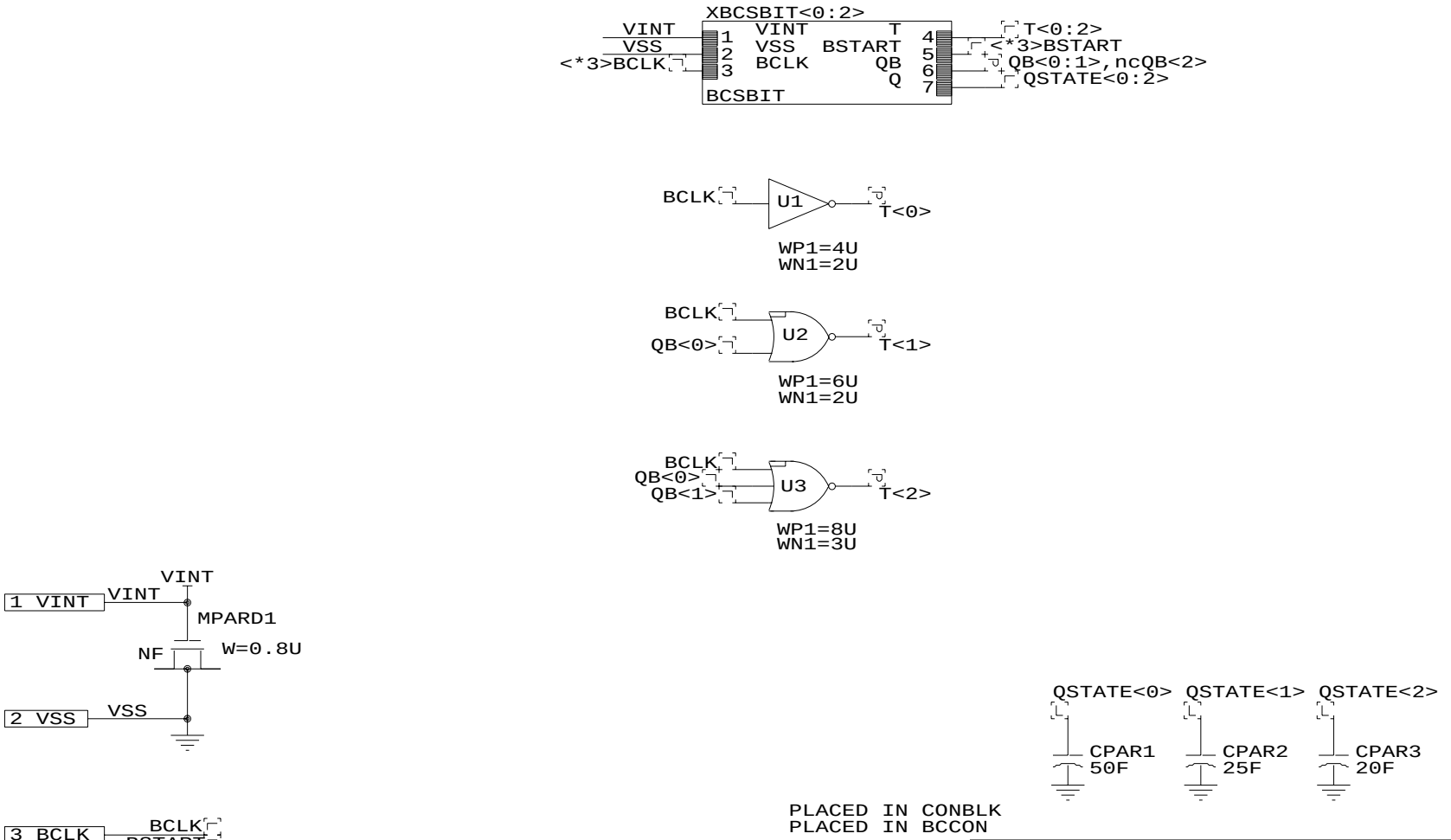
Inputs: READ / WRITE (COMMANDS)
BST (Burst counter STop from IDEC)
PWRUP (PoWeR UP signal is high during power-up)
BL<2,4,8> (Burst Length 2,4 and 8 from MRBLDEC)
JCLK - EXTERNAL BUFFERED CLOCK
AINB0, A0 INPUT FROM PAD BUFFER

Outputs: BCEND (Burst Counter END of burst to CONBLK.CABUF.BAEGEN)
KBCEND (CLOCKED BCEND - NEXT RISING EDGE)
REND (NEXT FALLING EDGE FROM KBCEND-CANCELS READS)

C0 LATCHED A0 FOR USE IN SHIFTING
(INPUT FOR SHIFT 0 PATH IN READS)

PLACED IN CABLK
PLACED IN CONBLK

United Memories Inc. Project: 128D14		
Title Burst Count CONtrol		
Size A	Document Number BCCON	REV A
Date: July 10, 2001	Sheet 1 of 1	



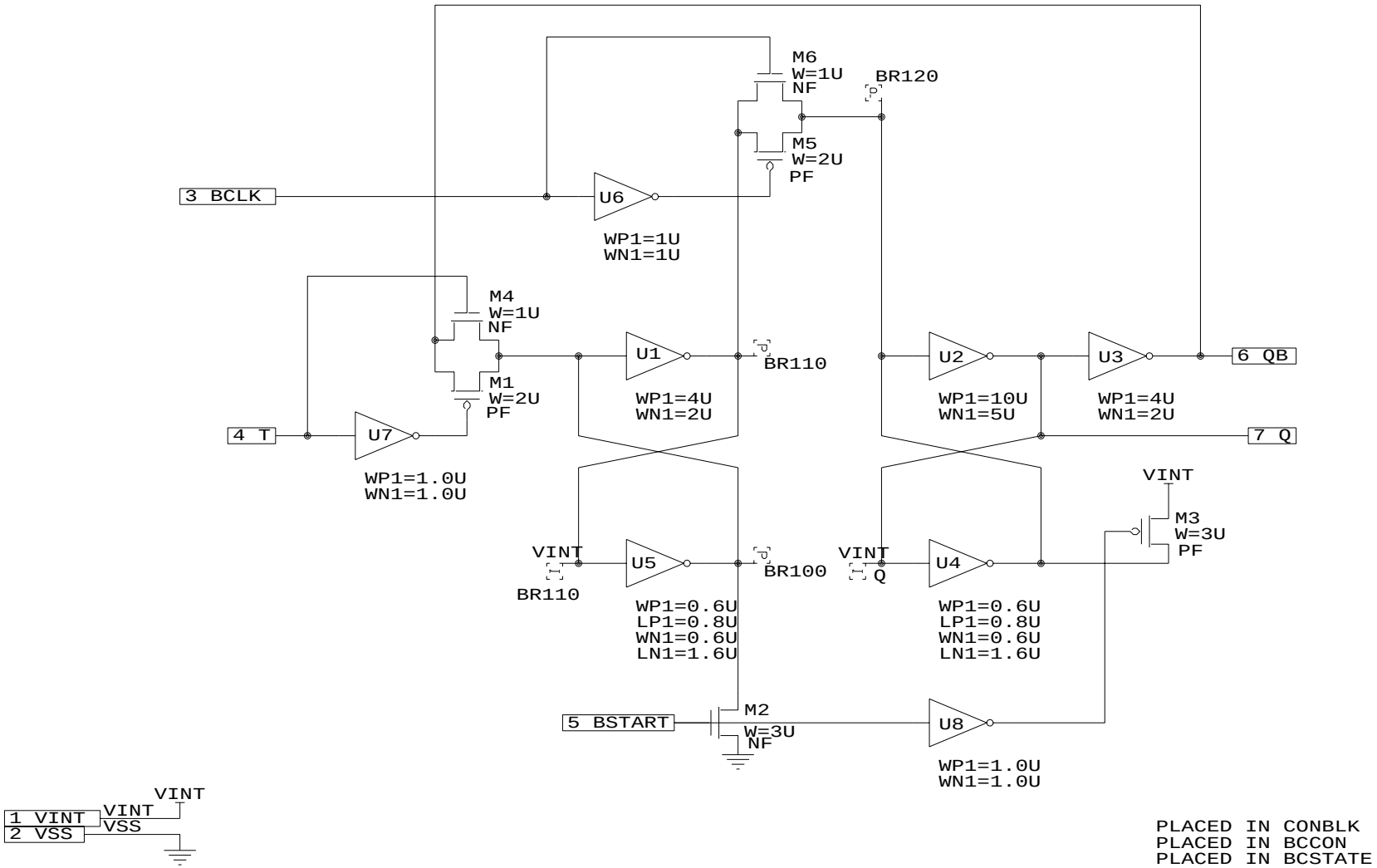
PLACED IN CONBLK
PLACED IN BCCON

Description: This circuit counts 0,1,2,3
the interleaved address sequence in the Burst Counter

Inputs: BCLK (CLocK from BCCLK)
CAE (Column Address Enable from BCCON)

Outputs: QSTATE<0:1> (Output STATE count to BCEND & BCTOGGLE)

United Memories Inc. Project: 128D14		
Title Burst Counter STATE counter		
Size A	Document Number BCSTATE	REV A
Date: October 12, 2001	Sheet 1 of 1	



PLACED IN CONBLK
PLACED IN BCCON
PLACED IN BCSTATE

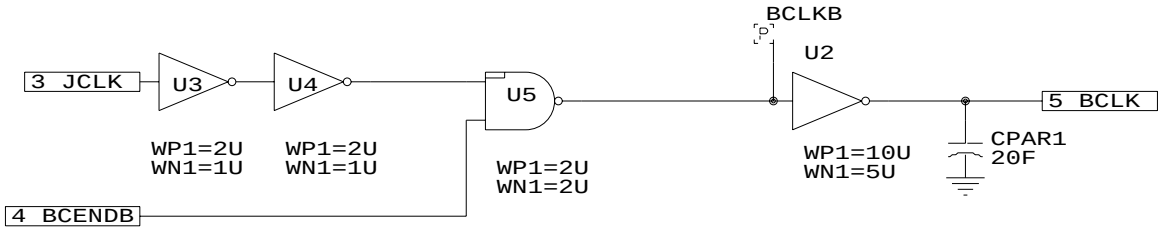
Description: This circuit is an element in a counter. The counter is used to count an interleaved sequence and to terminate count length column address bursts of length 2,4,8

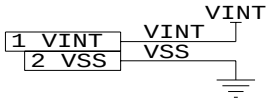
Inputs: BCLK (CLocK from BCCLK)
CAE (Resets latches - from BCCON)
T (Toggle from BCSTATE)

Outputs: Q (Output to BCTOGGLE)
QB (Output Bar to BCTOGGLE)

64S300 COPY

United Memories Inc.		
Project: 128D14		
Title		
Burst Counter State counter BIT		
Size	Document Number	REV
A	BCSBIT	A
Date: July 4, 2001	Sheet 1 of 1	





Description: This circuit generates the clock and load signals for the burst mode counter.

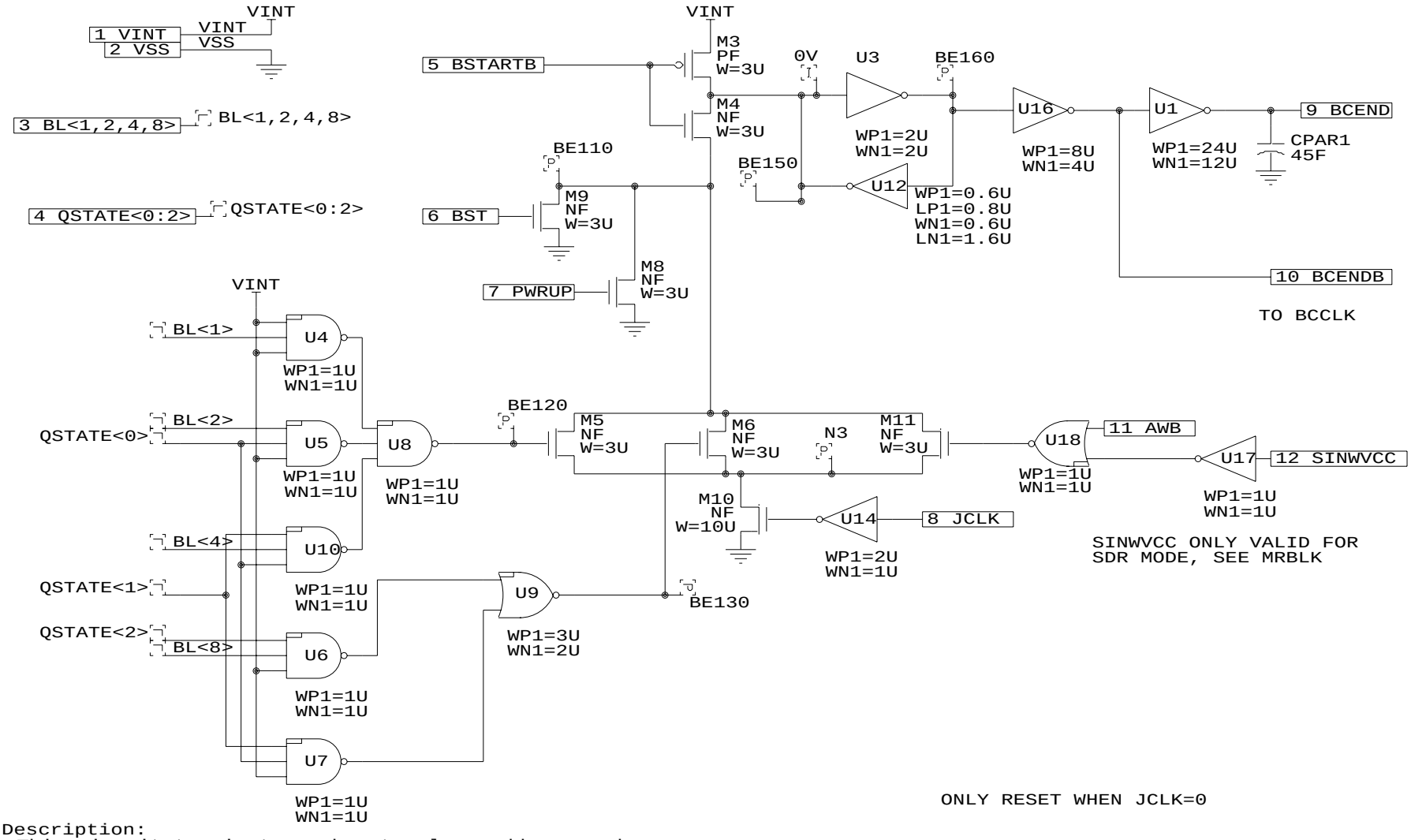
Inputs: JCLK (EXTERNAL BUFFERED CLOCK)

BCENDB (Burst Count END Bar from BCEND)

Outputs: BCLK (CLocK to BCBIT, BCEND & BCSTATE)

PLACED IN CONBLK
PLACED IN BCCON

United Memories Inc. Project: 128D14		
Title Burst Counter CLocK		
Size A	Document Number BCCLK	REV A
Date: October 12, 2001	Sheet 1 of 1	



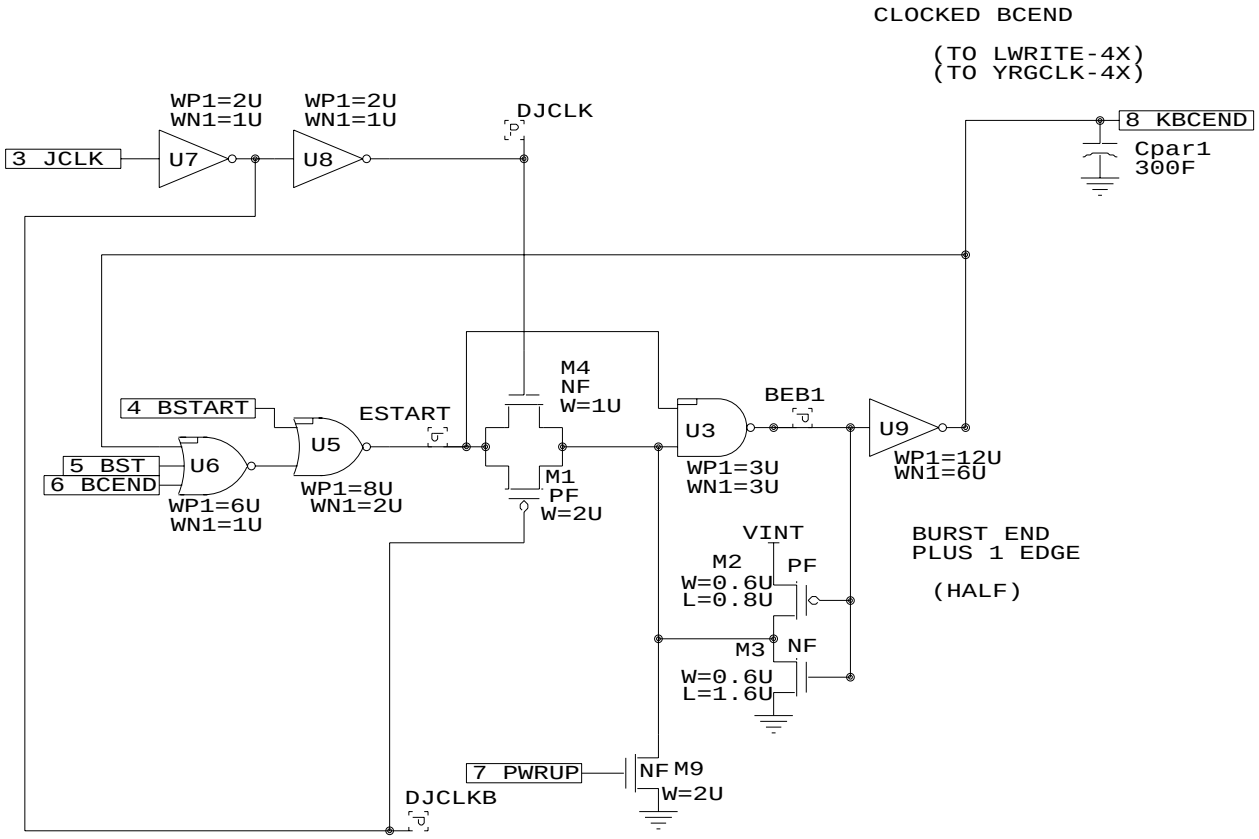
Description:
This circuit terminates a burst column address mode cycle based on burst length or write interupt.

Inputs: BL1,2,4,8 (Burst Length 2,4,8 from MRBLK)
SINWVCC-SINGLE WRITE MODE-FROM MRBLK
ALW (ANY LATCHED WRITE)
JCLK (EXTERNAL BUFFERED CLOCK)
BST (Burst STop from COMDEC)
QSTATE<0:2> (Output STATE count from BCSTATE)
PWRUP (PoWeR UP is high during power-up)

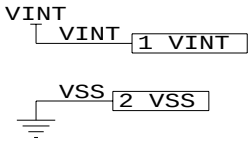
Outputs: BCEND (Burst Count END to BAEGEN, SHEND)
BCENDB (FOR USE IN BCCLK)

PLACED IN BCCON

United Memories Inc. Project: 128D14		
Title Burst Counter END of count		
Size A	Document Number BCEND	REV A
Date: October 12, 2001	Sheet 1 of 1	



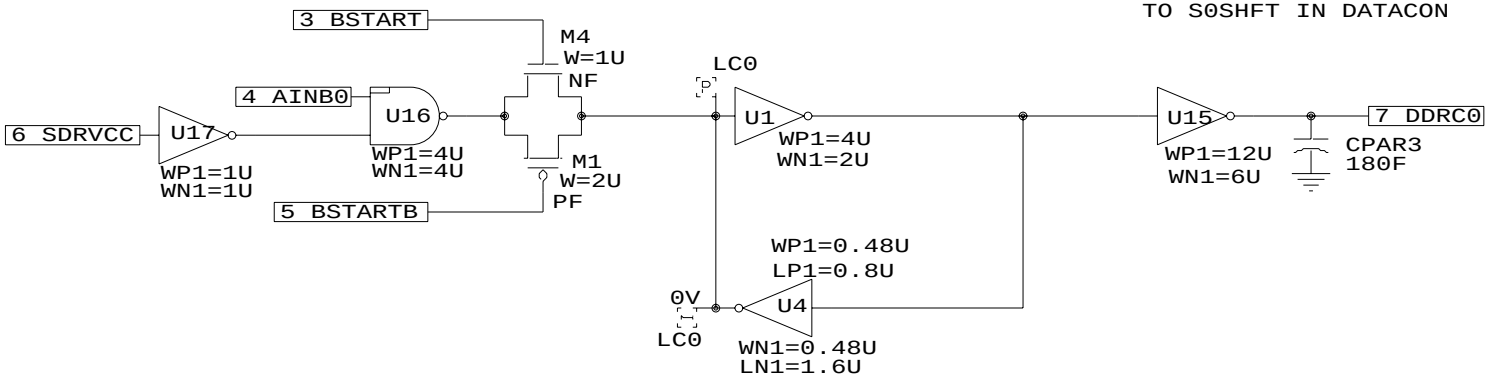
PLACED IN CONBLK (GENERATES CLOCKED REND, KBCEND)
PLACED IN BCCON



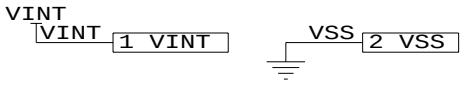
United Memories, Inc. PROJECT: 128D14		
Title SHIFTED BURST END DETECT		
Size A	Document Number KBCEND	REV A
Date: October 6, 2001	Sheet 1 of 1	

LATCHED CO FOR READ/WRITE CONTROL

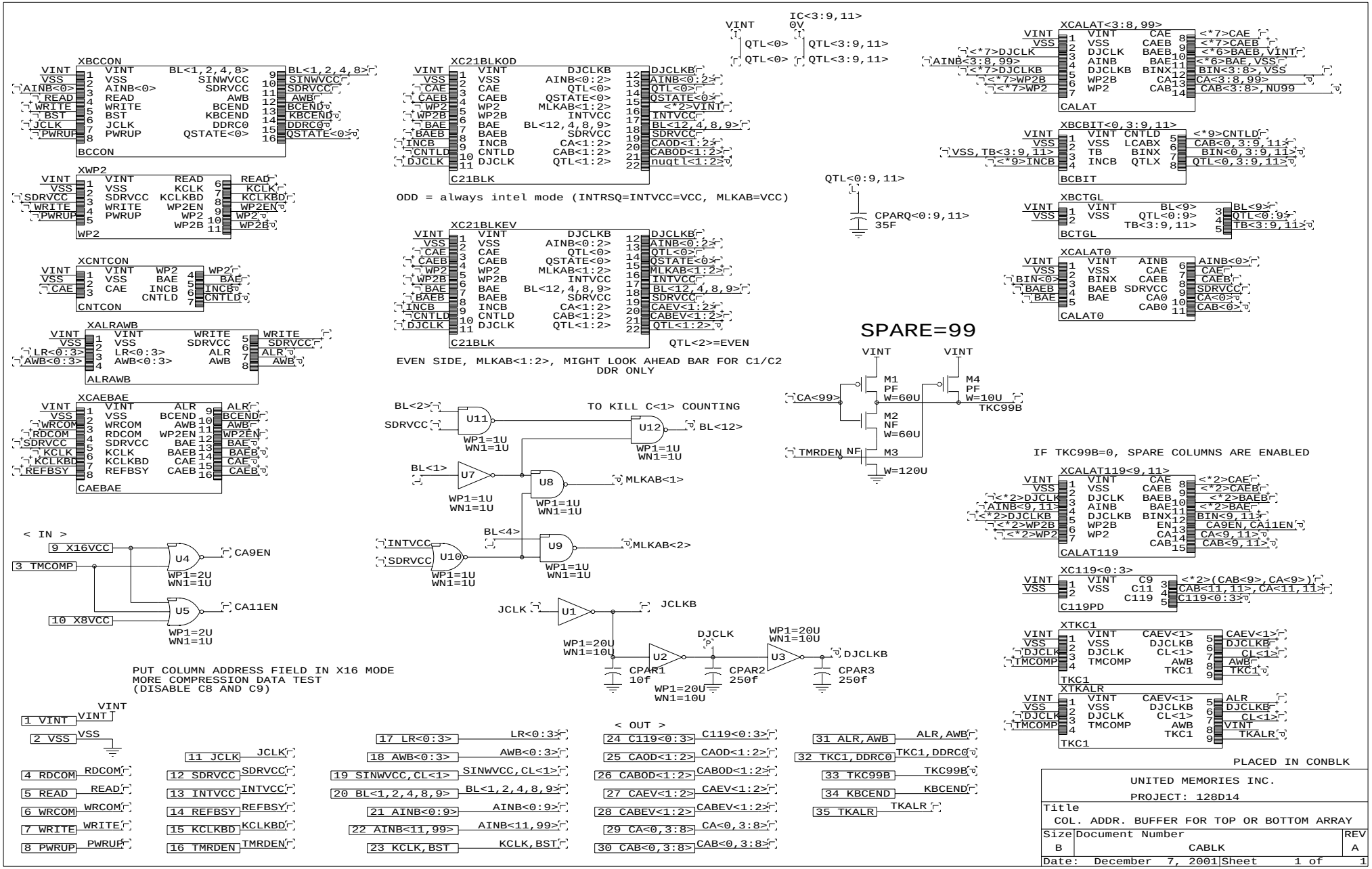
TO S0SHFT IN DATACON

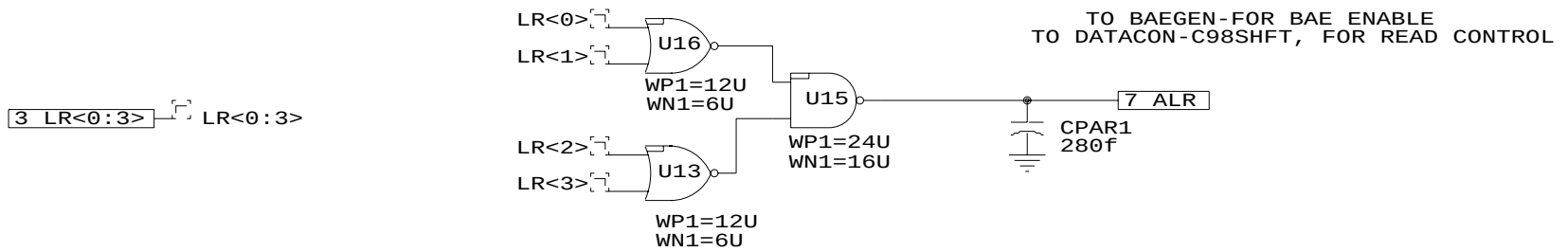


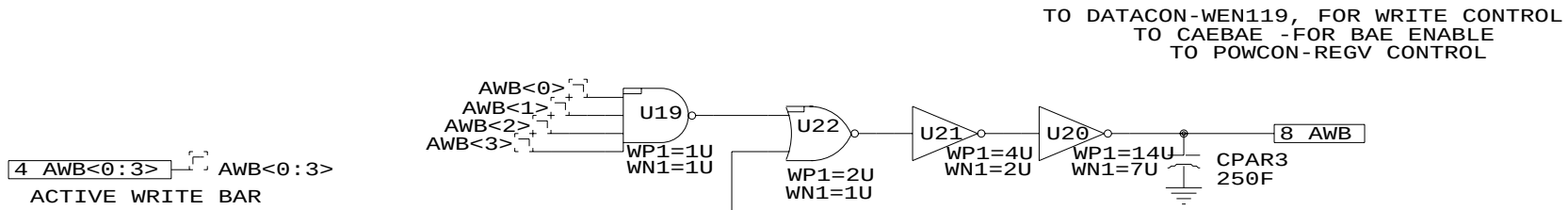
PLACED IN CONBLK
PLACED IN BCCON



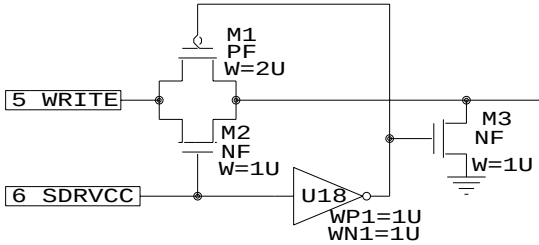
United Memories, Inc. PROJECT: 128D14		
Title C0 (ODD-EVEN) LATCH/BUFFER		
Size A	Document Number DDRC0	REV A
Date: October 12, 2001	Sheet 1 of 1	


XBCCON
BCCON
XWP2
WP2
XCNTCON
CNTCON
XALRAWB
ALRAWB
XCAEBAE
CAEBAE
XC21BLKOD
C21BLK
ODD = always intel mode (INTRSQ=INTVCC=VCC, MLKAB=VCC)
XC21BLKEV
C21BLK
QTL<2>=EVEN
EVEN SIDE, MLKAB<1:2>, MIGHT LOOK AHEAD BAR FOR C1/C2
DDR ONLY
IC<3:9,11>
QTL<0:9,11>
CPARQ<0:9,11>
35F
XCALAT<3:8,99>
CALAT
XBCBIT<0,3:9,11>
BCBIT
XBCTGL
BCTGL
XCALAT0
CALAT0
SPARE=99
M1
PF
W=60U
M2
NF
W=60U
M3
W=120U
M4
PF
W=10U
TKC99B
TMRDEN
CA<99>
IF TKC99B=0, SPARE COLUMNS ARE ENABLED
XCALAT119<9,11>
CALAT119
XC119<0:3>
C119PD
XTKC1
TKC1
XTKALR
TKC1
TO KILL C<1> COUNTING
U11
U12
U7
U8
U9
U10
U4
U5
U1
U2
U3
WP1=1U
WN1=1U
WP1=2U
WN1=1U
WP1=20U
WN1=10U
CPAR1
10f
CPAR2
250f
CPAR3
250f
< IN >
9 X16VCC
3 TMCOMP
10 X8VCC
CA9EN
CA11EN
PUT COLUMN ADDRESS FIELD IN X16 MODE
MORE COMPRESSION DATA TEST
(DISABLE C8 AND C9)
< OUT >
PLACED IN CONBLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
COL. ADDR. BUFFER FOR TOP OR BOTTOM ARRAY
Size B
Document Number CABLK
REV A
Date: December 7, 2001
Sheet 1 of 1





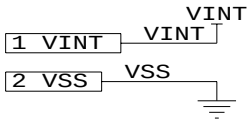
FOR SDR AWB=LW
FOR DDR AWB=LW1P5 (+1.5 CYCLES)



Description:

Inputs:

Outputs:

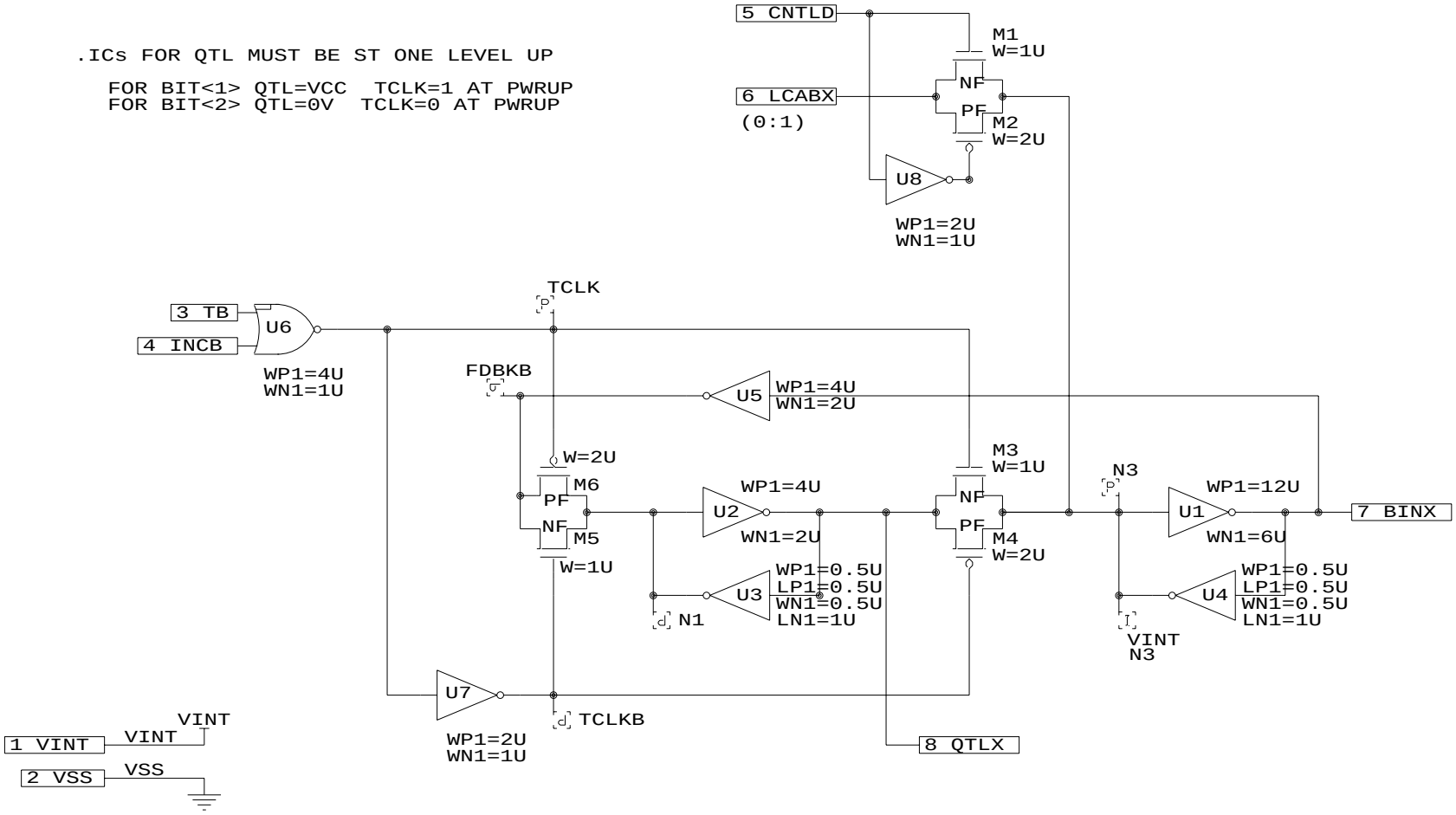


PLACED IN CONBLK
PLACED IN CABLK

United Memories Inc.		
Project: 128D14		
Title		
ANY LATCHED READ / ANY WRITE BAR		
Size A	Document Number ALRAWB	REV A
Date: October 12, 2001	Sheet 1 of 1	

.ICs FOR QTL MUST BE ST ONE LEVEL UP

FOR BIT<1> QTL=VCC TCLK=1 AT PWRUP
FOR BIT<2> QTL=0V TCLK=0 AT PWRUP



PLACED IN CONBLK
PLACED IN CABLK
PLACED IN C21BLK

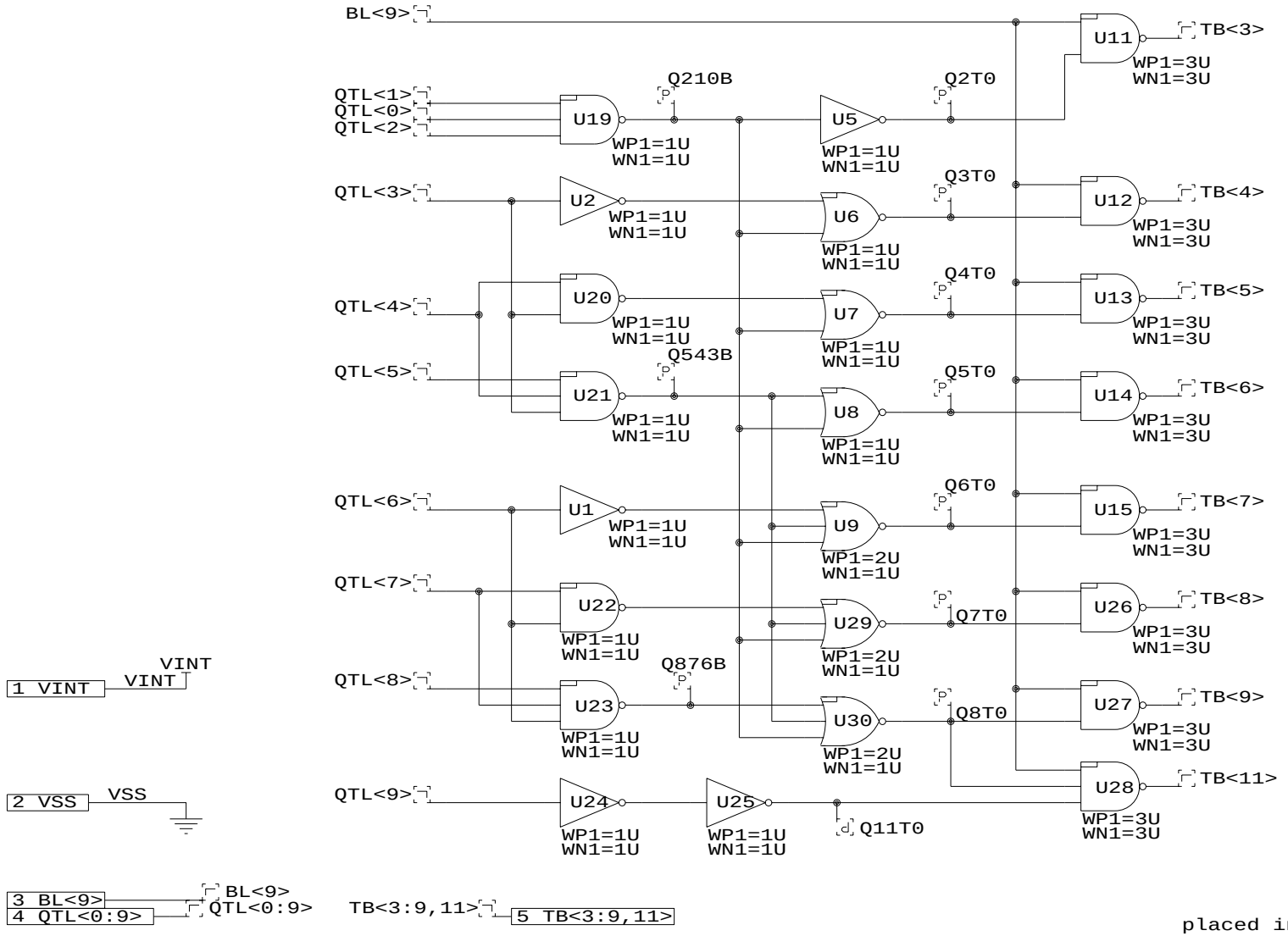
64S300 COPY

Description: This circuit is a register element for storing the current state of the burst mode counter. The state of the register is changed by loading a starting address into the register or by toggling to the next state.

Inputs: INCB - INCREMENT SIGNAL
TB (Toggle Bar from BCTOGGLE)
CNTLD - COUNTER LOAD (START POSITION)
LCAB - LATCHED COLUMN ADDRESS (START)

Outputs: BIN (Burst address INput to CBUF21'S
QTL (Output Toggle Lookahead to BCTOGGLE)

United Memories Inc.		
Project: 128D14		
Title		
Burst Counter Register BIT -FOR C0 AND C1		
Size	Document Number	REV
A	BCBIT	A
Date: July 7, 2001	Sheet 1 of 1	



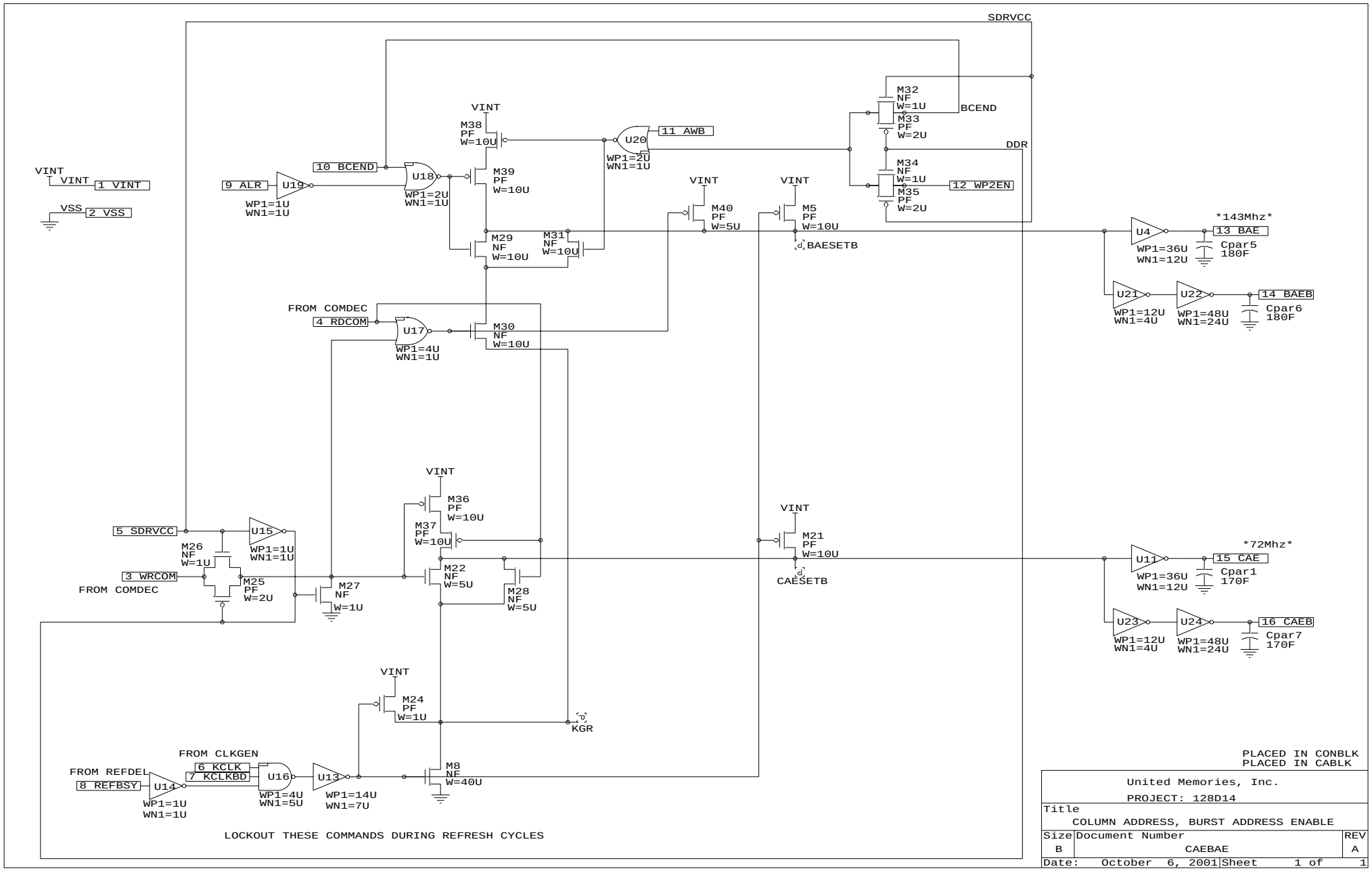
placed in CABLK block

Description: This circuit controls the toggle of the burst mode counter register bits 3 to 9 producing a linear count.

Inputs: BL<9> (Burst Length <9> full page from MRBLDEC)
QTL<0:6> OUTPUT TOGGLE LOOK-AHEAD

Outputs: TB<3:7> TOGGLE BAR - PER BIT

United Memories Inc.		
Project: 128D14		
Title		
Burst Counter ToGgLe page 2		
Size A	Document Number BCTGL	REV A
Date: July 5, 2001	Sheet 1 of 1	



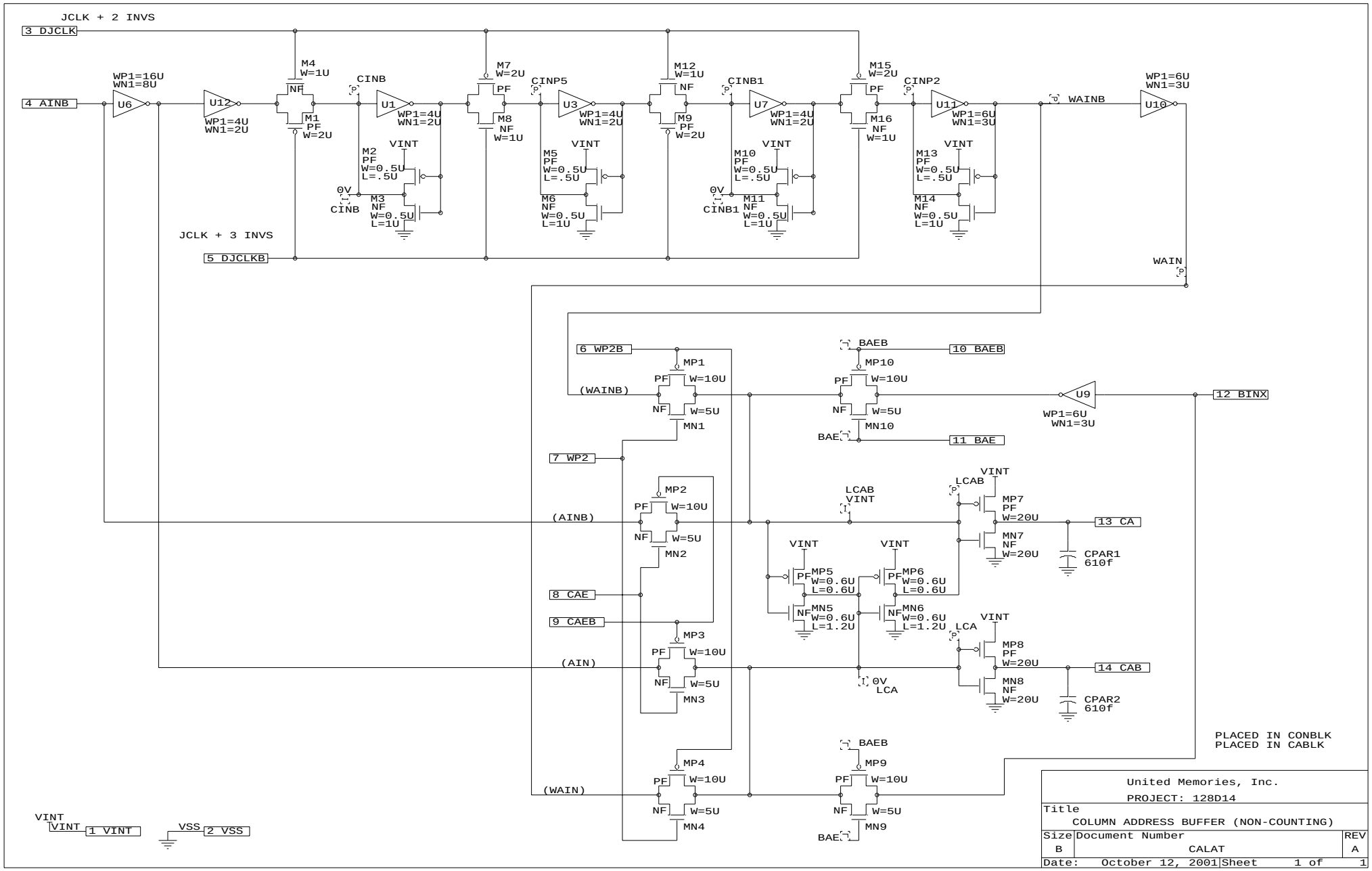
United Memories, Inc.

PROJECT: 128D14

Title: COLUMN ADDRESS, BURST ADDRESS ENABLE

Size	Document Number	REV
B	CAEBAE	A

Date: October 6, 2001 | Sheet 1 of 1



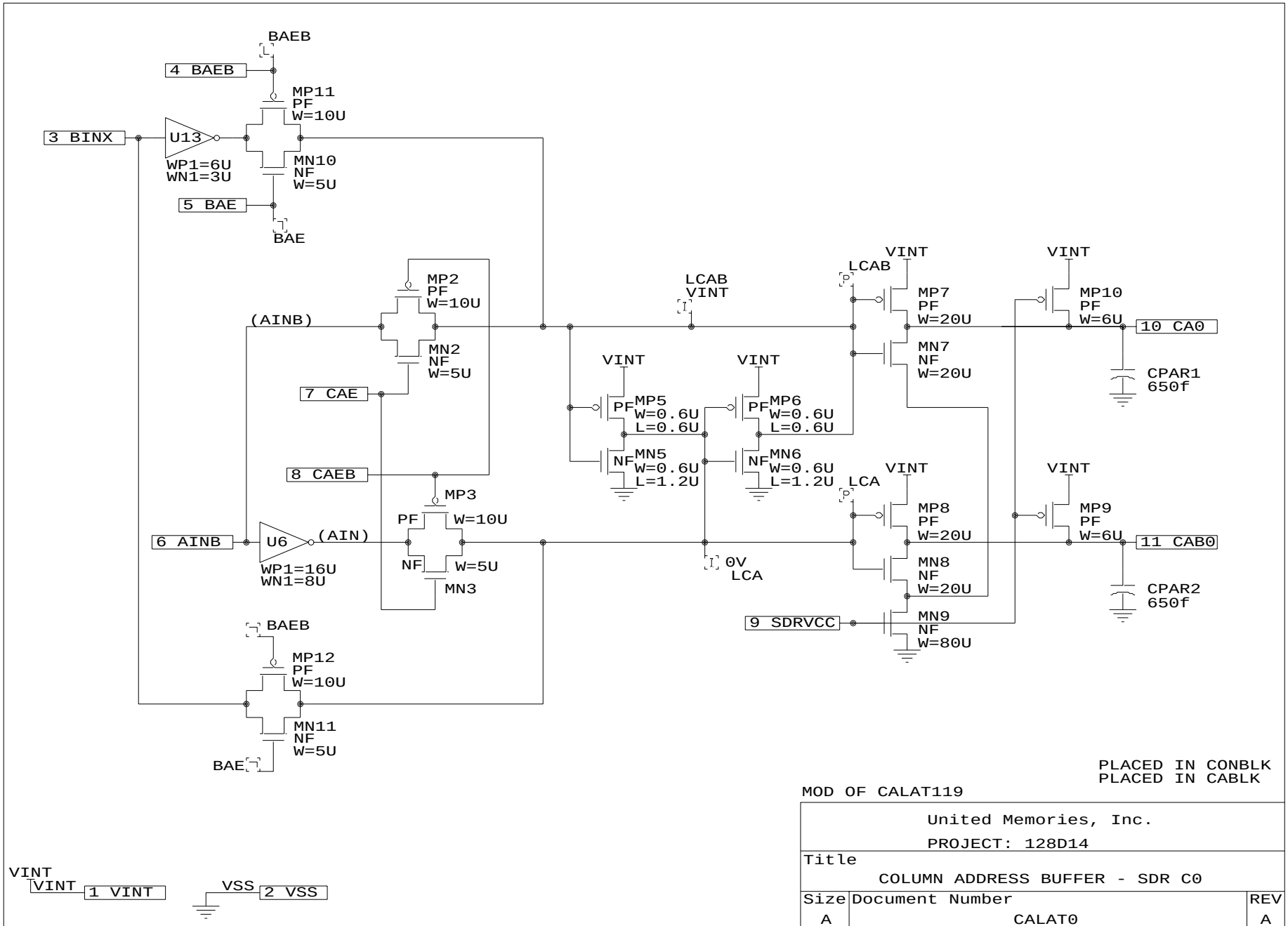
United Memories, Inc.

PROJECT: 128D14

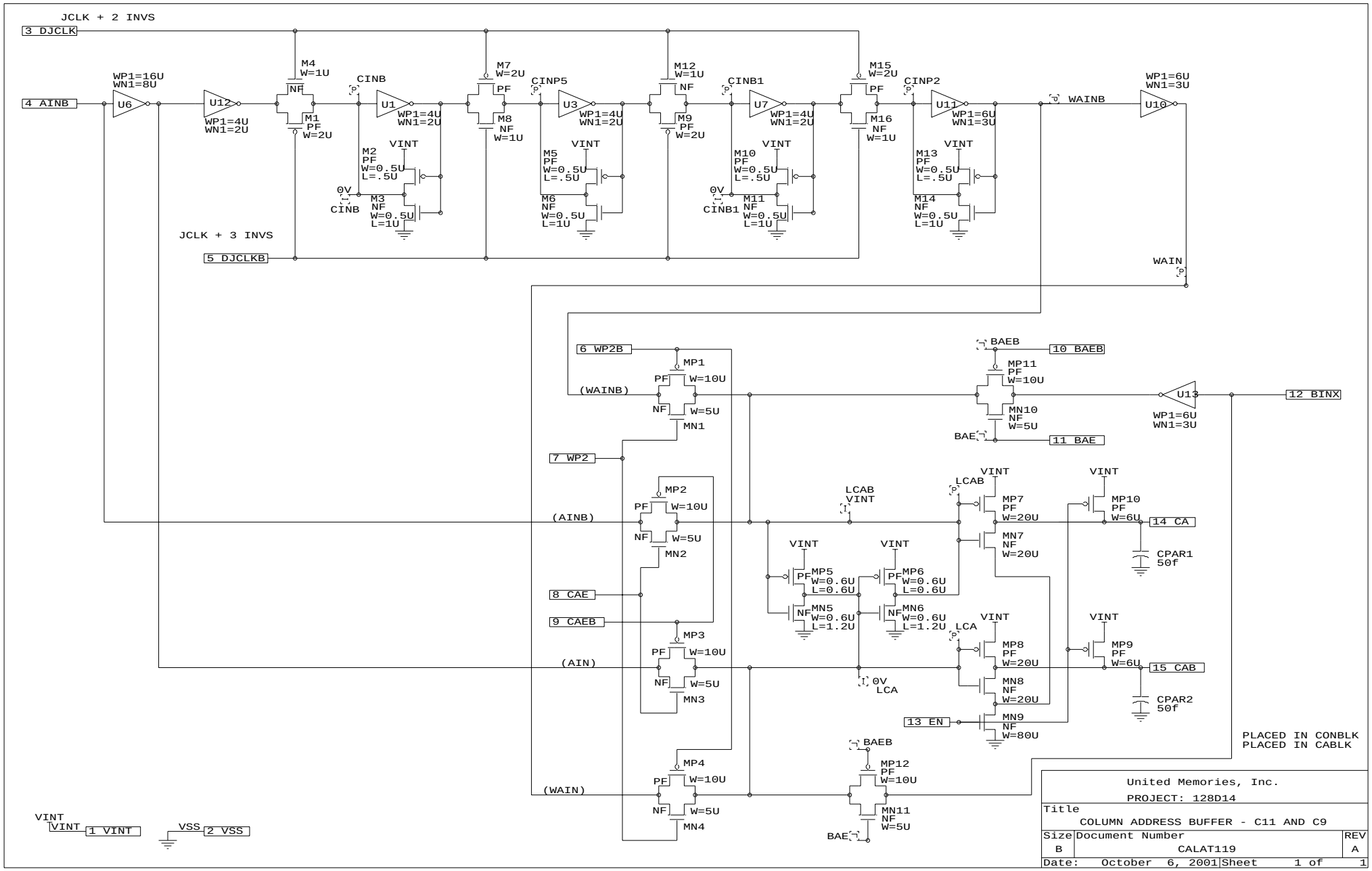
Title
COLUMN ADDRESS BUFFER (NON-COUNTING)

Size	Document Number	REV
B	CALAT	A

Date: October 12, 2001 Sheet 1 of 1



United Memories, Inc. PROJECT: 128D14		
Title COLUMN ADDRESS BUFFER - SDR C0		
Size A	Document Number CALAT0	REV A
Date: October 12, 2001	Sheet 1 of 1	



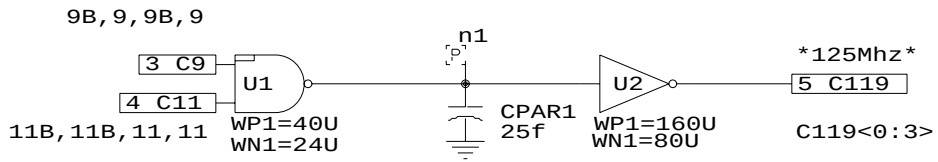
United Memories, Inc.

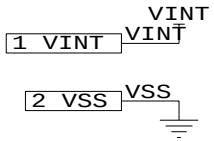
PROJECT: 128D14

Title: COLUMN ADDRESS BUFFER - C11 AND C9

Size	Document Number	REV
B	CALAT119	A

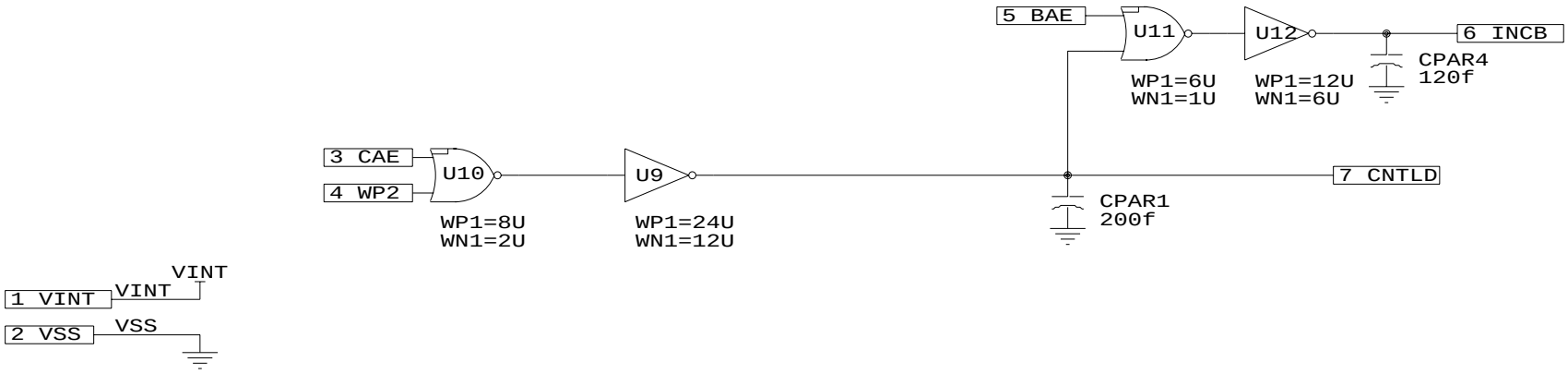
Date: October 6, 2001 | Sheet 1 of 1





PLACED IN CONBLK
PLACED IN CABLK

UNITED MEMORIES INC. PROJECT: 128D14		
Title C11 C9 COLUMN PREDECODER (1X)		
Size A	Document Number C119PD	REV A
Date: August 24, 2001	Sheet 1 of 1	



PLACED IN CONBLK
PLACED IN CABLK

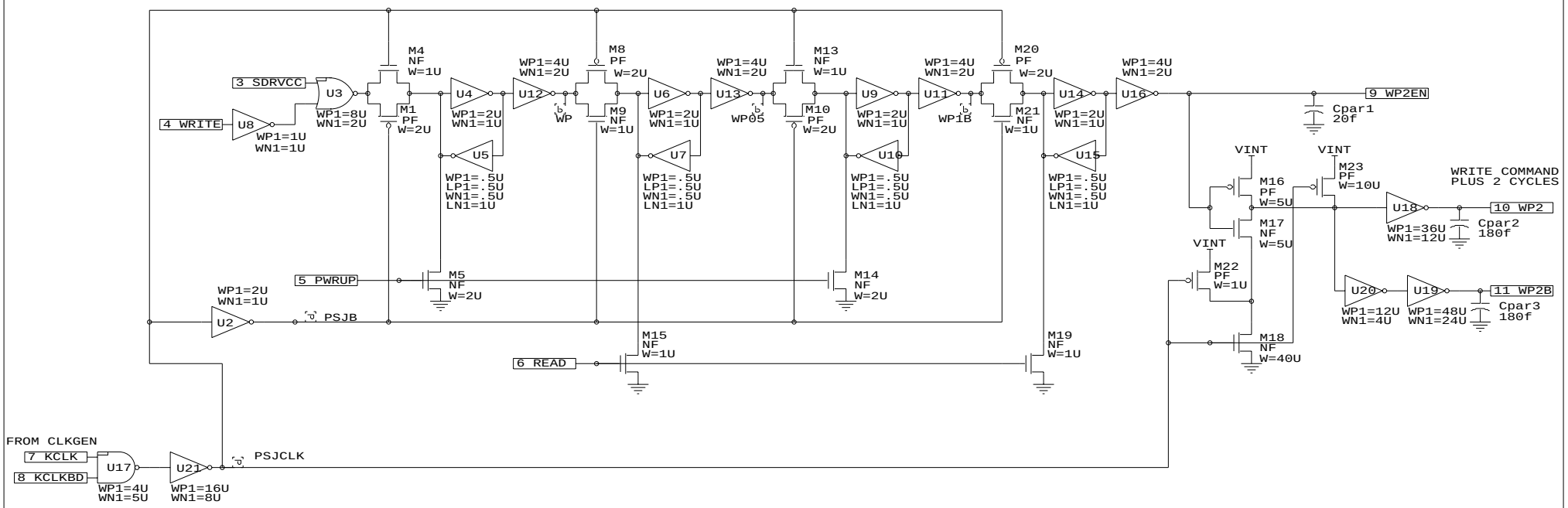
Description: CLOCKS FOR COLUMN CIRCUITS

Inputs:

COLUMN ADDRESS COUNT CONTROL

Outputs:

United Memories Inc. Project: 128D14		
Title INCB / CNTLD GENERATION		
Size A	Document Number CNTCON	REV A
Date: October 24, 2001	Sheet 1 of 1	



PSEUDO-JCLK USED TO SHIFT WP2
THROUGH, NOT JCLK,
TO MATCH TIMING IN TMSCLK MODE
WHERE JCLK IS ON A LOT
LONGER THAN KCLK.

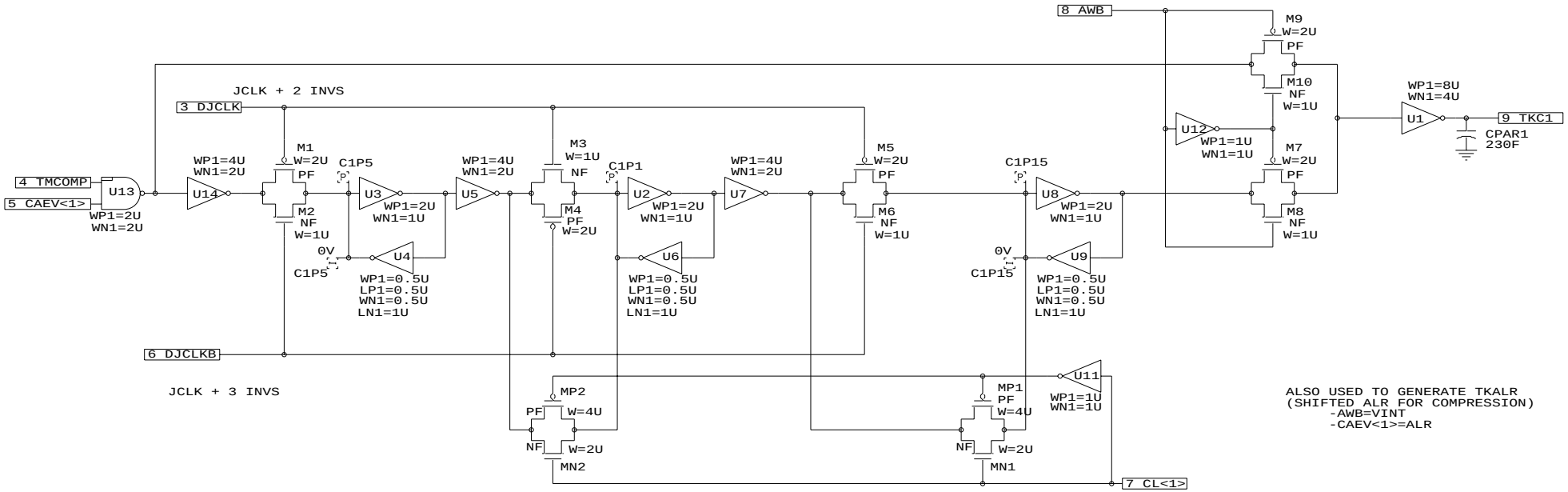
WRITE/WP2 ACTUALLY TURNED OFF FROM
KCLK, NOT KCLKBD IN THIS SCENARIO

PLACED IN CONBLK
PLACED IN CABLK

VINT
VINT 1 VINT

VSS 2 VSS

United Memories, Inc.		
PROJECT: 128D14		
Title		
WRITE COMMAND PULSE - DELAYED 2 CYCLES		
Size	Document Number	REV
B	WP2	A
Date: October 6, 2001	Sheet 1 of 1	



ALSO USED TO GENERATE TKALR
(SHIFTED ALR FOR COMPRESSION)
-AWB=VINT
-CAEV<1>=ALR

CHECK PIPELINE FOR WRITES (ASWB?)

CHECK PIPELINE FOR CL2/2.5

CHECK PIPELINE FOR DLL ON/OFF

PLACED IN CONBLK
PLACED IN CABLK

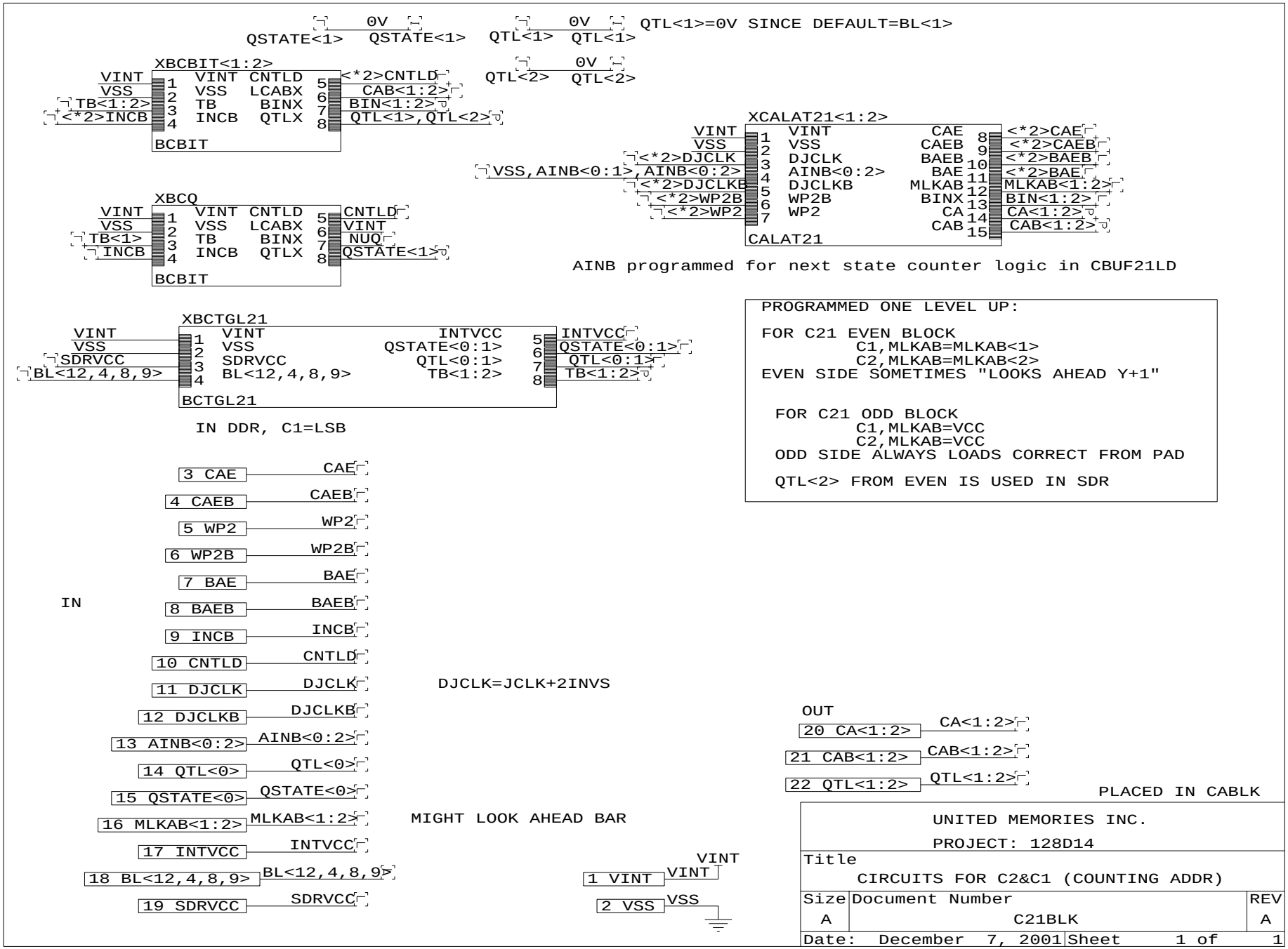
128DDR S17 MOD

(ALSO USED FOR SPARE COL SELECT)
(CARED)

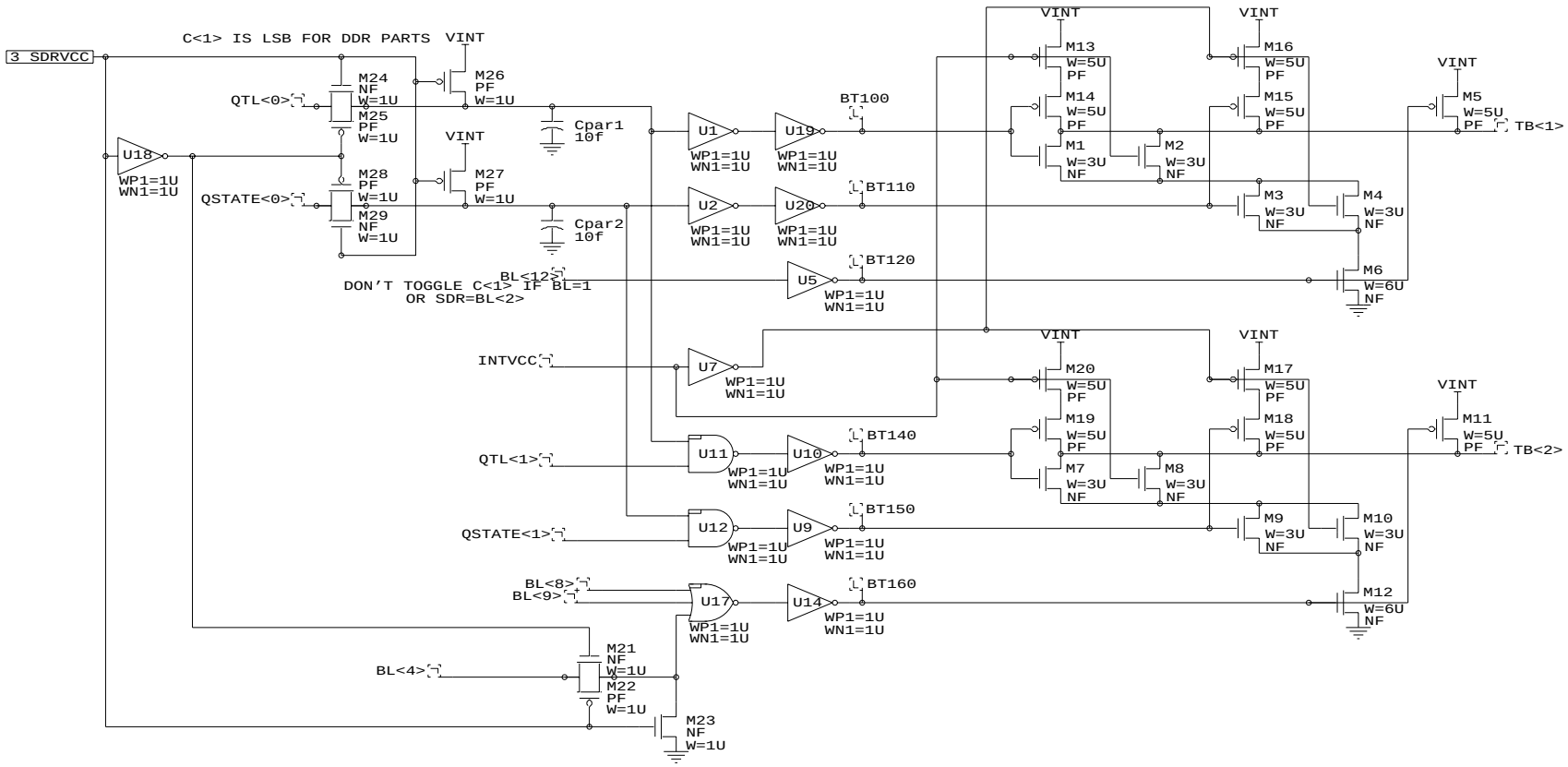
VINT
VINT 1 VINT

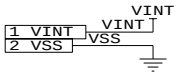
VSS 2 VSS

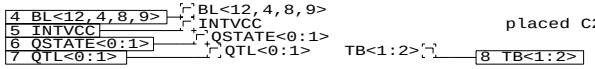
United Memories, Inc.		
PROJECT: 128D14		
Title		
SHIFTED C1 FOR COMPRESSION		
Size	Document Number	REV
B	TKC1	A
Date: October 6, 2001	Sheet 1 of 1	


0V
QSTATE<1> QSTATE<1>
0V
QTL<1> QTL<1>
QTL<1>=0V SINCE DEFAULT=BL<1>
0V
QTL<2> QTL<2>
XBCBIT<1:2>
VINT 1 VINT CNTLD 5 <*2>CNTLD
VSS 2 VSS LCABX 6 CAB<1:2>
TB<1:2> 3 TB BINX 7 BIN<1:2>
<*2>INCB 4 INCB QTLX 8 QTL<1>,QTL<2>
BCBIT
XCALAT21<1:2>
VINT 1 VINT CAE 8 <*2>CAE
VSS 2 VSS CAEB 9 <*2>CAEB
<*2>DJCLK 3 DJCLK BAEB 10 <*2>BAEB
VSS,AINB<0:1>,AINB<0:2> 4 AINB<0:2> BAE 11 <*2>BAE
<*2>DJCLKB 5 DJCLKB MLKAB 12 MLKAB<1:2>
<*2>WP2B 6 WP2B BINX 13 BIN<1:2>
<*2>WP2 7 WP2 CA 14 CA<1:2>
CAB 15 CAB<1:2>
CALAT21
XBCQ
VINT 1 VINT CNTLD 5 CNTLD
VSS 2 VSS LCABX 6 VINT
TB<1> 3 TB BINX 7 NUQ
INCB 4 INCB QTLX 8 QSTATE<1>
BCBIT
AINB programmed for next state counter logic in CBUF21LD
XBCTGL21
VINT 1 VINT INTVCC 5 INTVCC
VSS 2 VSS QSTATE<0:1> 6 QSTATE<0:1>
SDRVCC 3 SDRVCC QTL<0:1> 7 QTL<0:1>
BL<12,4,8,9> 4 BL<12,4,8,9> TB<1:2> 8 TB<1:2>
BCTGL21
IN DDR, C1=LSB
PROGRAMMED ONE LEVEL UP:
FOR C21 EVEN BLOCK
C1,MLKAB=MLKAB<1>
C2,MLKAB=MLKAB<2>
EVEN SIDE SOMETIMES "LOOKS AHEAD Y+1"
FOR C21 ODD BLOCK
C1,MLKAB=VCC
C2,MLKAB=VCC
ODD SIDE ALWAYS LOADS CORRECT FROM PAD
QTL<2> FROM EVEN IS USED IN SDR
IN
3 CAE CAE
4 CAEB CAEB
5 WP2 WP2
6 WP2B WP2B
7 BAE BAE
8 BAEB BAEB
9 INCB INCB
10 CNTLD CNTLD
11 DJCLK DJCLK
12 DJCLKB DJCLKB
13 AINB<0:2> AINB<0:2>
14 QTL<0> QTL<0>
15 QSTATE<0> QSTATE<0>
16 MLKAB<1:2> MLKAB<1:2>
17 INTVCC INTVCC
18 BL<12,4,8,9> BL<12,4,8,9>
19 SDRVCC SDRVCC
DJCLK=JCLK+2INVS
MIGHT LOOK AHEAD BAR
OUT
20 CA<1:2> CA<1:2>
21 CAB<1:2> CAB<1:2>
22 QTL<1:2> QTL<1:2>
PLACED IN CABLK
VINT
1 VINT VINT
2 VSS VSS
UNITED MEMORIES INC.
PROJECT: 128D14
Title
CIRCUITS FOR C2&C1 (COUNTING ADDR)
Size A
Document Number C21BLK
REV A
Date: December 7, 2001
Sheet 1 of 1

BL<#> REFERS TO NUMBER OF YCLKS NEEDED
I.E. DDR BURST LENGTH 4 = BL<2>
SDR BURST LENGTH 4 = BL<4>







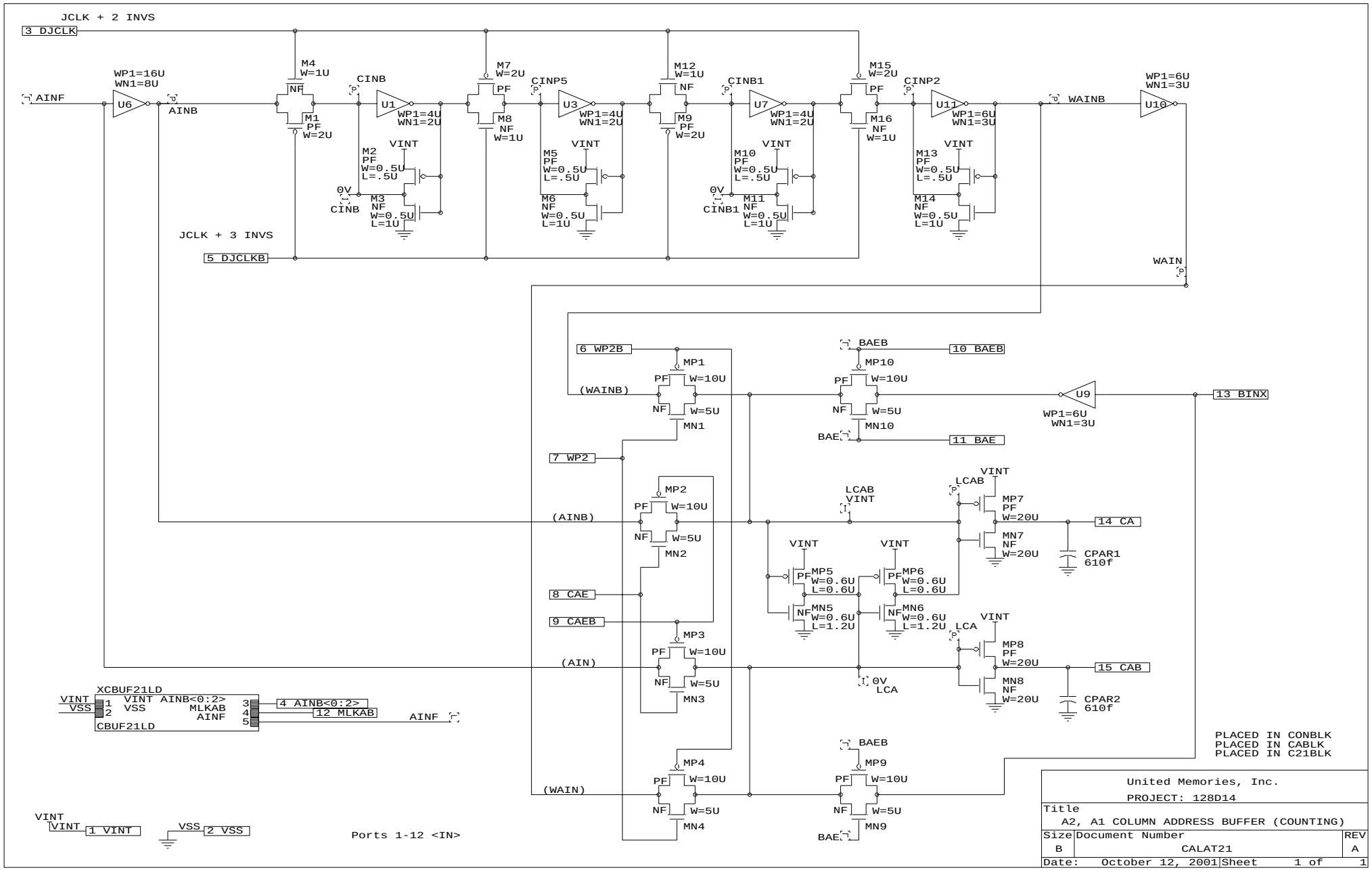
placed C21BLK

Description: This circuit controls the toggle of the burst mode register 1 & 2 bits in order to produce either a binary or interleaved count.

Inputs: BL<1,4,8,9> (Burst Length 1,4, 8, 9 (full) from MRBLDEC)
INTL (InterLeaved mode from MRBLK)
QSTATE<0,1> (Output STATE count 1 & 2 from BCSTATE)
QTL<0,1> (Output Toggle Lookahead from BCBIT)

Outputs: TB<1,2> (Toggle Bar stage 1 & 2 to BCBIT)

United Memories Inc.		
Project: 128D14		
Title: Burst Counter ToGgLe page 1		
Size: B	Document Number: BCTGL21	REV: A
Date: December 7, 2001	Sheet 1 of 1	



United Memories, Inc.

PROJECT: 128D14

Title

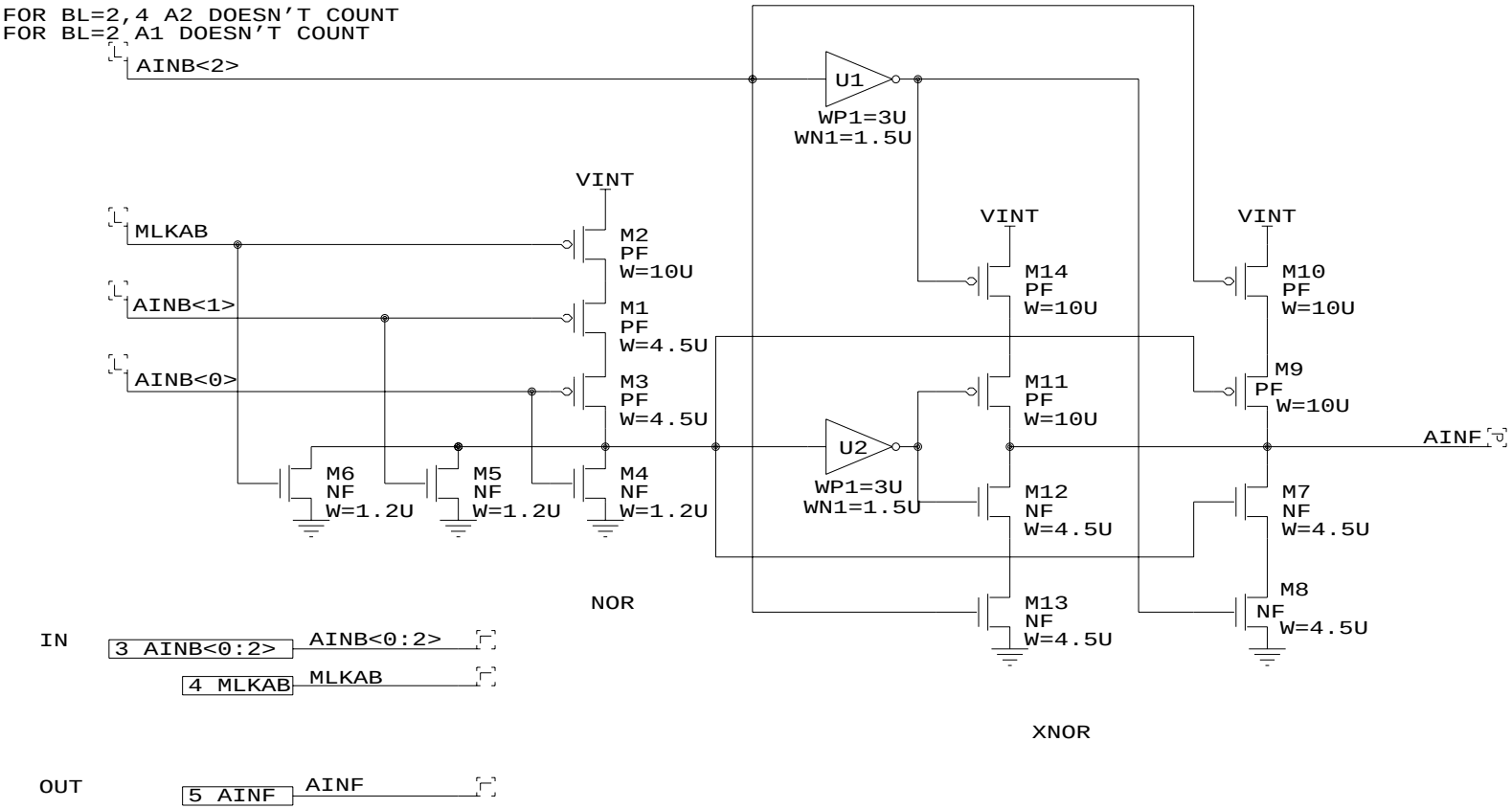
A2, A1 COLUMN ADDRESS BUFFER (COUNTING)

Size	Document Number	REV
B	CALAT21	A

Date: October 12, 2001 Sheet 1 of 1

```
BL=8 CASE SHOWN                    NEXT STATE LOGIC DESCRIPTION
     ABC||A'B'C'
     000||0 0 1    Now, for ease of writing eqns, let C' denote Cprime=Cp, and let C' denote Cbar
     001||0 1 0    Ap=A'BC+AB'C'+AB'C+ABC'=A'BC+A(B'+C')=A'BC+A(BC)'=A XOR (BC) = A' XNOR (B' NOR C')
     010||0 1 1    Bp=A'B'C+A'BC'+AB'C+ABC'=B'C(A'+A)+BC'(A+A')=B'C+BC'=B XOR C=B' XNOR C=B' XNOR (C'+VSS)'
     011||1 0 0    Cp=C'
     100||1 0 1
     101||1 1 0
     110||1 1 1    MLKAB allows for passthru(w/ invert);if MLKAB is hi, AINBF=AIN
     111||0 0 0    SSE 5/99

FOR BL=2,4 A2 DOESN'T COUNT
FOR BL=2,A1 DOESN'T COUNT
```



IN 3 AINB<0:2> AINB<0:2>

4 MLKAB MLKAB

OUT 5 AINF AINF

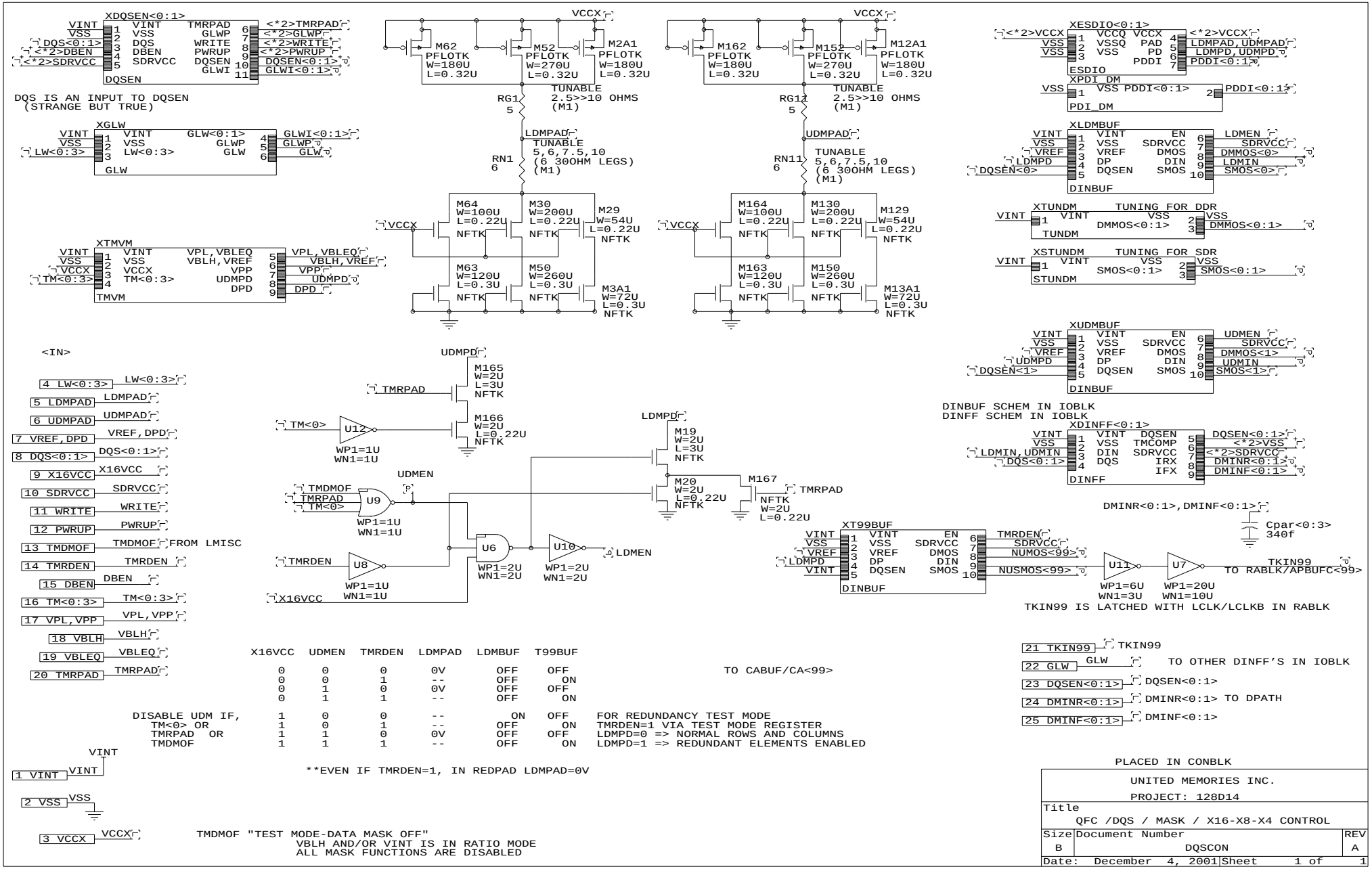
AINF=Addr In Fixed (for lin/int mode)

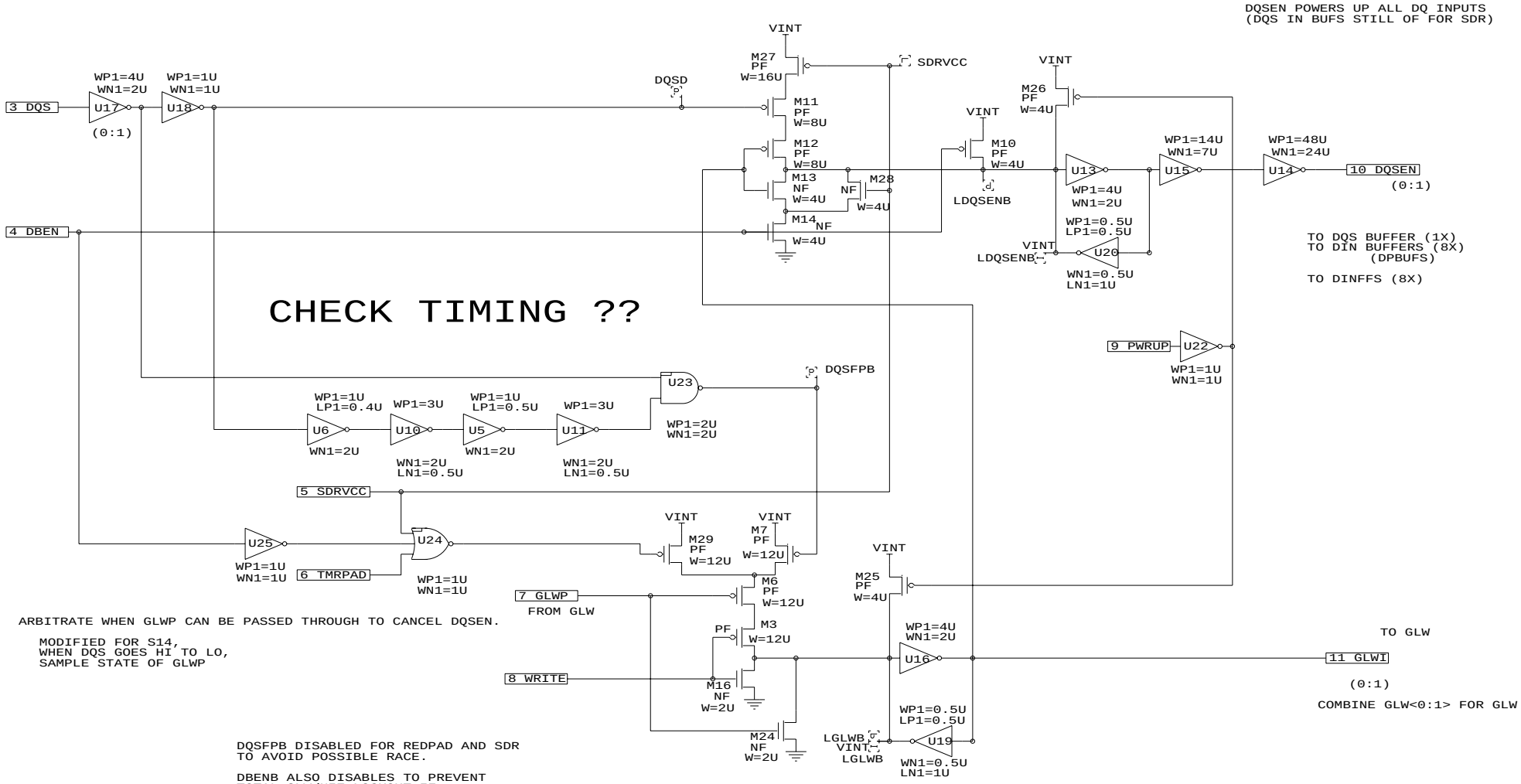
1 VINT VINT

2 VSS VSS

PLACED IN C21BLK/CBUF21

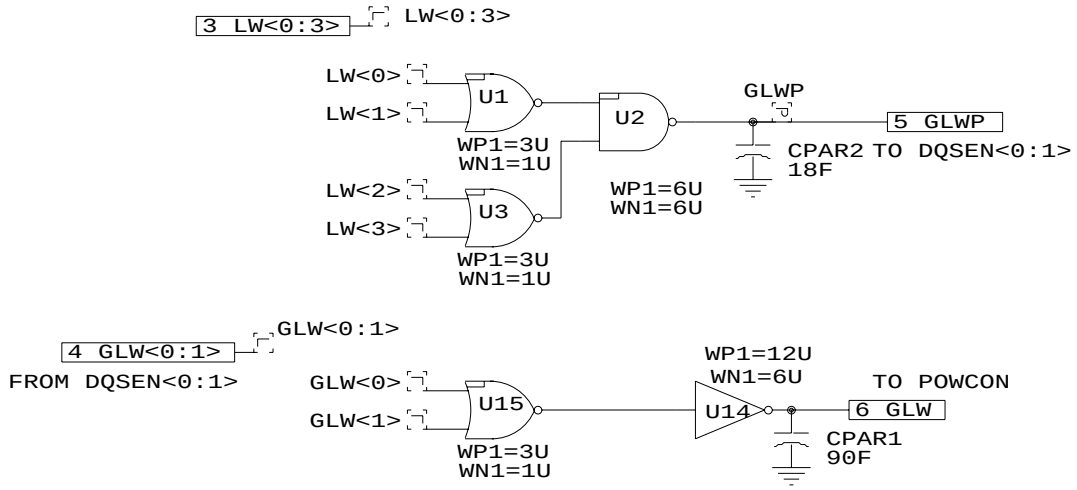
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
COLUMN COUNT LOGIC		
Size	Document Number	REV
A	CBUF21LD	A
Date: August 24, 2001	Sheet 1 of 1	


XDQSEN<0:1>
VINT VSS DQS<0:1> <*2>DBEN <*2>SDRVCC
VINT VSS DQS DBEN SDRVCC
TMRPAD GLWP WRITE PWRUP DQSEN GLWI
<*2>TMRPAD <*2>GLWP <*2>WRITE <*2>PWRUP DQSEN<0:1> GLWI<0:1>
DQSEN
DQS IS AN INPUT TO DQSEN
(STRANGE BUT TRUE)
XGLW
VINT VSS LW<0:3>
VINT VSS LW<0:3> GLW<0:1> GLWP GLW
GLWI<0:1> GLWP GLW
GLW
XTMVM
VINT VSS VCCX TM<0:3>
VINT VSS VCCX TM<0:3> VPL,VBLEQ VBLH,VREF VPP UDMPD DPD
VPL,VBLEQ VBLH,VREF VPP UDMPD DPD
TMVM
VCCX
M62 PFLOTK W=180U L=0.32U
M52 PFLOTK W=270U L=0.32U
M2A1 PFLOTK W=180U L=0.32U
M162 PFLOTK W=180U L=0.32U
M152 PFLOTK W=270U L=0.32U
M12A1 PFLOTK W=180U L=0.32U
RG1 5
RG11 5
TUNABLE 2.5>>10 OHMS (M1)
LDMPAD
UDMPAD
RN1 6
RN11 6
TUNABLE 5,6,7.5,10 (6 30OHM LEGS) (M1)
M64 W=100U L=0.22U NFTK
M30 W=200U L=0.22U NFTK
M29 W=54U L=0.22U NFTK
M63 W=120U L=0.3U NFTK
M50 W=260U L=0.3U NFTK
M3A1 W=72U L=0.3U NFTK
M164 W=100U L=0.22U NFTK
M130 W=200U L=0.22U NFTK
M129 W=54U L=0.22U NFTK
M163 W=120U L=0.3U NFTK
M150 W=260U L=0.3U NFTK
M13A1 W=72U L=0.3U NFTK
XESDIO<0:1>
<*2>VCCX VSS VSS
VCCQ VCCX VSSQ PAD VSS PD PDDI
<*2>VCCX LDMPAD,UDMPAD LDMPD,UDMPD PDDI<0:1>
ESDIO
XPDI_DM
VSS VSS PDDI<0:1> PDDI<0:1>
PDI_DM
XLDMBUF
VINT VSS VREF LDMPD DQSEN<0>
VINT VSS VREF DP DQSEN EN SDRVCC DMOS DIN SMOS
LDMEN SDRVCC DMMOS<0> LDMIN SMOS<0>
DINBUF
XTUNDM TUNING FOR DDR
VINT VINT VSS DMMOS<0:1> VSS DMMOS<0:1>
TUNDM
XSTUNDM TUNING FOR SDR
VINT VINT VSS SMOS<0:1> VSS SMOS<0:1>
STUNDM
XUDMBUF
VINT VSS VREF UDMPD DQSEN<1>
VINT VSS VREF DP DQSEN EN SDRVCC DMOS DIN SMOS
UDMEN SDRVCC DMMOS<1> UDMIN SMOS<1>
DINBUF
DINBUF SCHEM IN IOBLK
DINFF SCHEM IN IOBLK
XDINFF<0:1>
VINT VSS LDMIN,UDMIN DQS<0:1>
VINT VSS DIN DQS DQSEN TMCOMP SDRVCC IRX IFX
DQSEN<0:1> <*2>VSS <*2>SDRVCC DMINR<0:1> DMINF<0:1>
DINFF
<IN>
4 LW<0:3> LW<0:3>
5 LDMPAD LDMPAD
6 UDMPAD UDMPAD
7 VREF,DPD VREF,DPD
8 DQS<0:1> DQS<0:1>
9 X16VCC X16VCC
10 SDRVCC SDRVCC
11 WRITE WRITE
12 PWRUP PWRUP
13 TMDMOF TMDMOF FROM LMISC
14 TMRDEN TMRDEN
15 DBEN DBEN
16 TM<0:3> TM<0:3>
17 VPL,VPP VPL,VPP
18 VBLH VBLH
19 VBLEQ VBLEQ
20 TMRPAD TMRPAD
UDMPD
M165 W=2U L=3U NFTK
M166 W=2U L=0.22U NFTK
TMRPAD
TM<0>
U12
WP1=1U WN1=1U
LDMPD
M19 W=2U L=3U NFTK
M20 W=2U L=0.22U NFTK
M167 NFTK W=2U L=0.22U
TMRPAD
UDMEN
TMDMOF TMRPAD TM<0>
U9
WP1=1U WN1=1U
U6
WP1=2U WN1=2U
U10
WP1=2U WN1=2U
LDMEN
TMRDEN
U8
WP1=1U WN1=1U
X16VCC
XT99BUF
VINT VSS VREF LDMPD VINT
VINT VSS VREF DP DQSEN EN SDRVCC DMOS DIN SMOS
TMRDEN SDRVCC NUMOS<99> NUSMOS<99>
DINBUF
U11
WP1=6U WN1=3U
U7
WP1=20U WN1=10U
TKIN99
TO RABLK/APBUFC<99>
DMINR<0:1>,DMINF<0:1>
Cpar<0:3> 340f
TKIN99 IS LATCHED WITH LCLK/LCLKB IN RABLK
21 TKIN99 TKIN99
22 GLW GLW
TO OTHER DINFF'S IN IOBLK
23 DQSEN<0:1> DQSEN<0:1>
24 DMINR<0:1> DMINR<0:1> TO DPATH
25 DMINF<0:1> DMINF<0:1>
TO CABUF/CA<99>
X16VCC UDMEN TMRDEN LDMPAD LDMBUF T99BUF
0 0 0 0V OFF OFF
0 0 1 -- OFF ON
0 1 0 0V OFF OFF
0 1 1 -- OFF ON
DISABLE UDM IF, TM<0> OR TMRPAD OR TMDMOF
1 0 0 -- ON OFF
1 0 1 -- OFF ON
1 1 0 0V OFF OFF
1 1 1 -- OFF ON
FOR REDUNDANCY TEST MODE
TMRDEN=1 VIA TEST MODE REGISTER
LDMPD=0 => NORMAL ROWS AND COLUMNS
LDMPD=1 => REDUNDANT ELEMENTS ENABLED
**EVEN IF TMRDEN=1, IN REDPAD LDMPAD=0V
VINT
1 VINT VINT
2 VSS VSS
3 VCCX VCCX
TMDMOF "TEST MODE-DATA MASK OFF"
VBLH AND/OR VINT IS IN RATIO MODE
ALL MASK FUNCTIONS ARE DISABLED
PLACED IN CONBLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
QFC /DQS / MASK / X16-X8-X4 CONTROL
Size B
Document Number
DQSCON
REV A
Date: December 4, 2001
Sheet 1 of 1



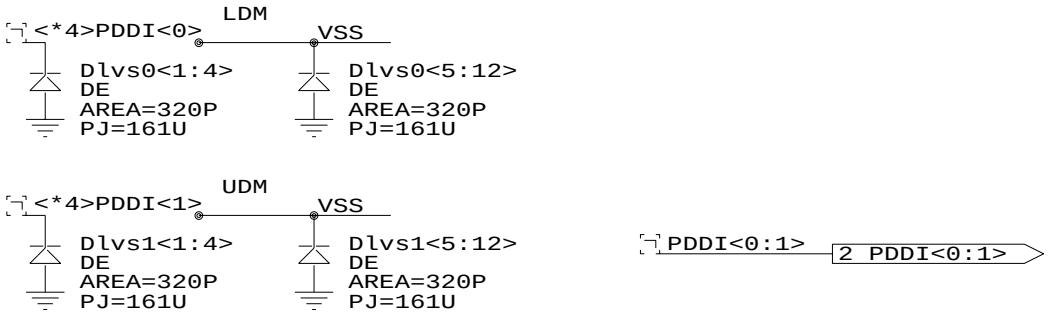
PLACED IN DQSCON

United Memories, Inc.		
PROJECT: 128D14		
Title	DQS- WRITE CONTROL	
Size B	Document Number DQSEN	REV A
Date: September 20, 2001	Sheet 1 of 1	



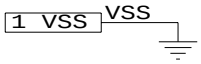
PLACED IN DQSCON

United Memories, Inc. PROJECT: 128D14		
Title GLOBAL LATCHED WRITE - DQS WRITE CONTROL		
Size A	Document Number GLW	REV A
Date: October 6, 2001	Sheet 1 of 1	



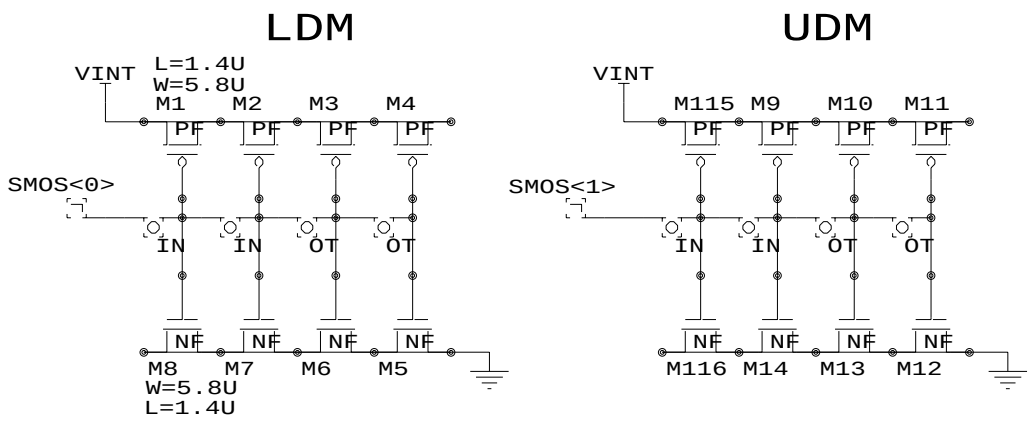
12 WELL DIODES UNDER THE PADS

THESE DIODES ARE TO ADD PAD CAPACITANCE



PLACED IN DQSCON

United Memories Inc. PROJECT: 128D14		
Title PAD DIODES FOR DM PINS		
Size A	Document Number PDI_DM	REV A
Date: October 3, 2001	Sheet 1 of 1	



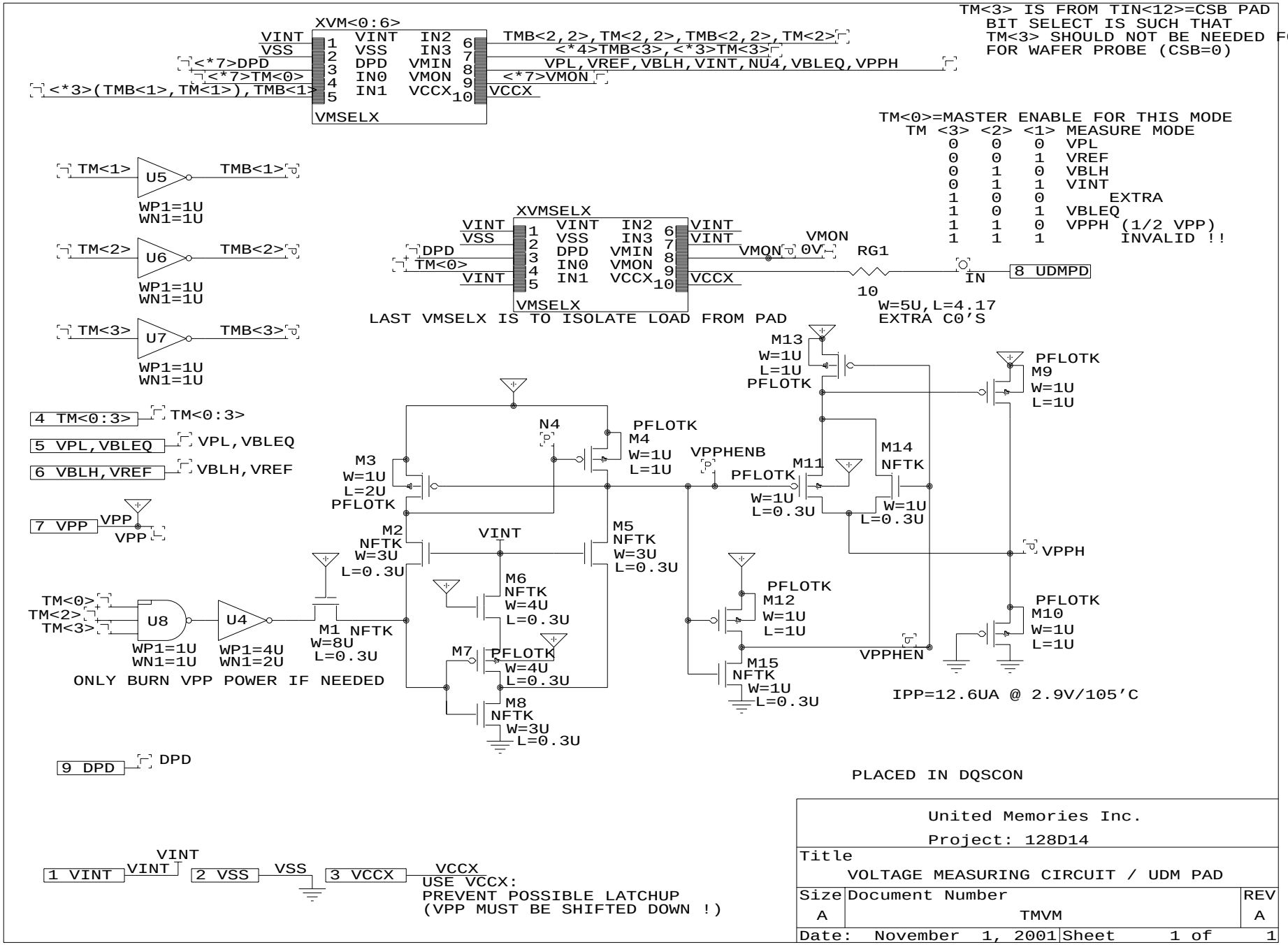
SIZED FOR 100PS/CAP

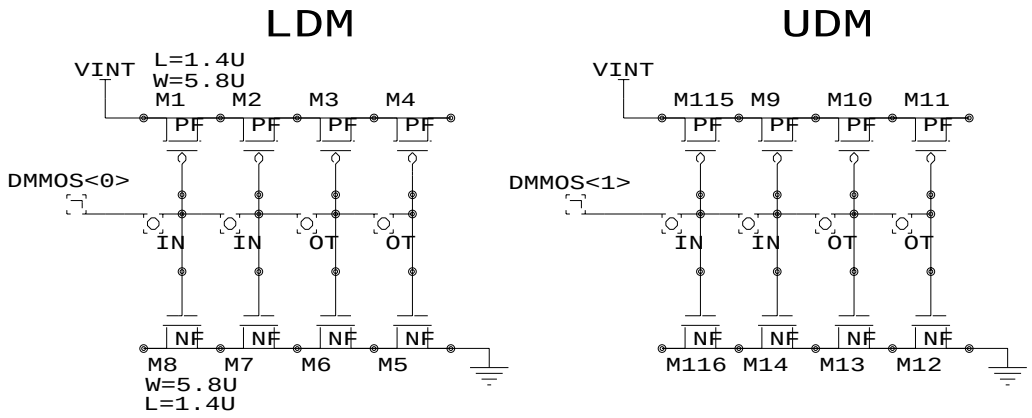
P-CHAN W=3U L=1.5U

N-CHAN W=3U L=1.5U

PLACED IN DQSCON

United Memories, Inc. PROJECT: 128D14		
Title SDR TUNING CIRCUIT FOR 2 DATA MASK SIGNALS		
Size A	Document Number STUNDM	REV A
Date: October 5, 2001	Sheet 1 of 1	


TM<3> IS FROM TIN<12>=CSB PAD
BIT SELECT IS SUCH THAT
TM<3> SHOULD NOT BE NEEDED FOR
FOR WAFER PROBE (CSB=0)
XVM<0:6>
VINT 1 VINT IN2 6 TMB<2,2>,TM<2,2>,TMB<2,2>,TM<2>
VSS 2 VSS IN3 7 <*4>TMB<3>,<*3>TM<3>
<*7>DPD 3 DPD VMIN 8 VPL,VREF,VBLH,VINT,NU4,VBLEQ,VPPH
<*7>TM<0> 4 IN0 VMON 9 <*7>VMON
<*3>(TMB<1>,TM<1>),TMB<1> 5 IN1 VCCX 10 VCCX
VMSELX
TM<0>=MASTER ENABLE FOR THIS MODE
TM <3> <2> <1> MEASURE MODE
0 0 0 VPL
0 0 1 VREF
0 1 0 VBLH
0 1 1 VINT
1 0 0 EXTRA
1 0 1 VBLEQ
1 1 0 VPPH (1/2 VPP)
1 1 1 INVALID !!
TM<1> U5 TMB<1>
WP1=1U
WN1=1U
TM<2> U6 TMB<2>
WP1=1U
WN1=1U
TM<3> U7 TMB<3>
WP1=1U
WN1=1U
XVMSELX
VINT 1 VINT IN2 6 VINT
VSS 2 VSS IN3 7 VINT
DPD 3 DPD VMIN 8 VMON
TM<0> 4 IN0 VMON 9 VMON 0V
VINT 5 IN1 VCCX 10 VCCX
VMSELX
RG1
10
IN
8 UDMPD
W=5U,L=4.17
EXTRA C0'S
LAST VMSELX IS TO ISOLATE LOAD FROM PAD
M13
W=1U
L=1U
PFLOTK
PFLOTK
M9
W=1U
L=1U
4 TM<0:3> TM<0:3>
5 VPL,VBLEQ VPL,VBLEQ
6 VBLH,VREF VBLH,VREF
7 VPP VPP
N4
PFLOTK
M4
W=1U
L=1U
M3
W=1U
L=2U
PFLOTK
VPPHENB
M11
PFLOTK
W=1U
L=0.3U
M14
NFTK
W=1U
L=0.3U
M2
NFTK
W=3U
L=0.3U
VINT
M5
NFTK
W=3U
L=0.3U
VPPH
M6
NFTK
W=4U
L=0.3U
PFLOTK
M12
W=1U
L=1U
PFLOTK
M10
W=1U
L=1U
TM<0>
TM<2>
TM<3>
U8
WP1=1U
WN1=1U
U4
WP1=4U
WN1=2U
M1 NFTK
W=8U
L=0.3U
M7
PFLOTK
W=4U
L=0.3U
VPPHEN
M15
NFTK
W=1U
L=0.3U
ONLY BURN VPP POWER IF NEEDED
IPP=12.6UA @ 2.9V/105'C
M8
NFTK
W=3U
L=0.3U
9 DPD DPD
PLACED IN DQSCON
1 VINT VINT
2 VSS VSS
3 VCCX VCCX
USE VCCX:
PREVENT POSSIBLE LATCHUP
(VPP MUST BE SHIFTED DOWN !)
United Memories Inc.
Project: 128D14
Title
VOLTAGE MEASURING CIRCUIT / UDM PAD
Size A
Document Number
TMVM
REV A
Date: November 1, 2001
Sheet 1 of 1



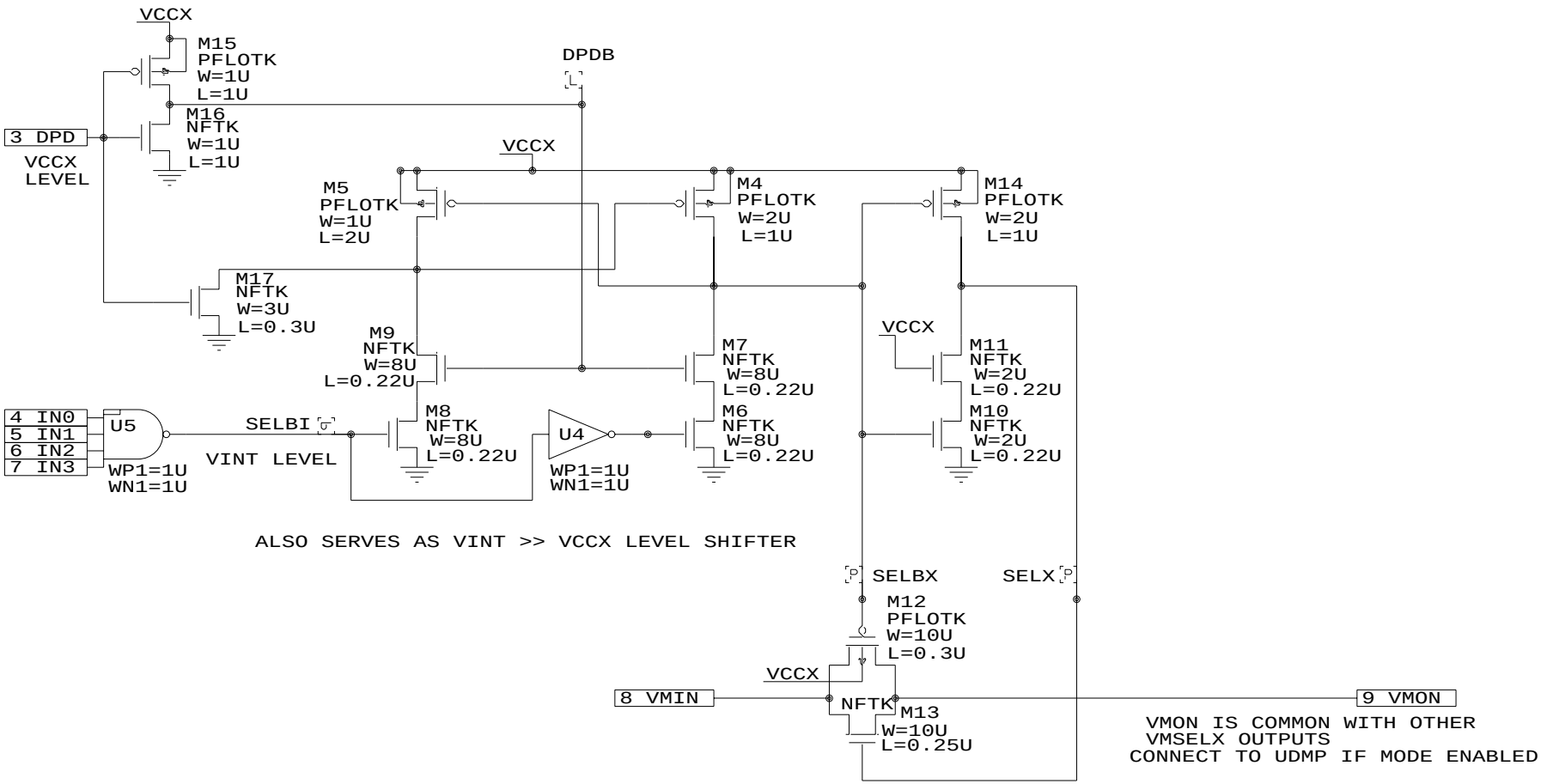
SIZED FOR 100PS/CAP

P-CHAN W=5.8U L=1.4U

N-CHAN W=5.8U L=1.4U

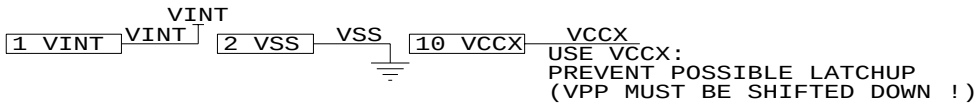
PLACED IN DQSCON

United Memories, Inc. PROJECT: 128D14		
Title TUNING CIRCUIT FOR 2 DATA MASK SIGNALS		
Size A	Document Number TUNDM	REV A
Date: September 22, 2001	Sheet 1 of 1	

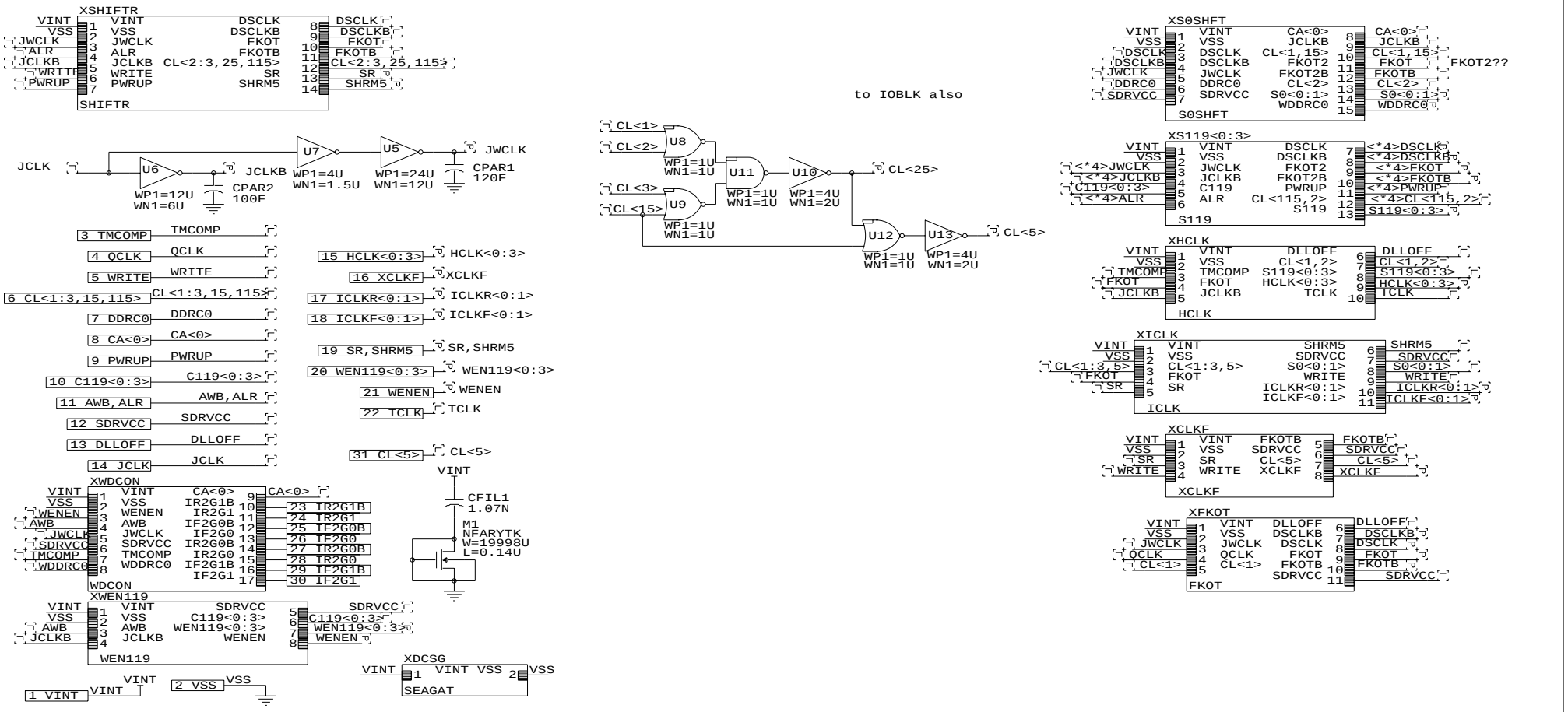


PRIMARY USE, SELECTING VOLTAGE MUXES IN TMVM

PLACED IN DQSCON

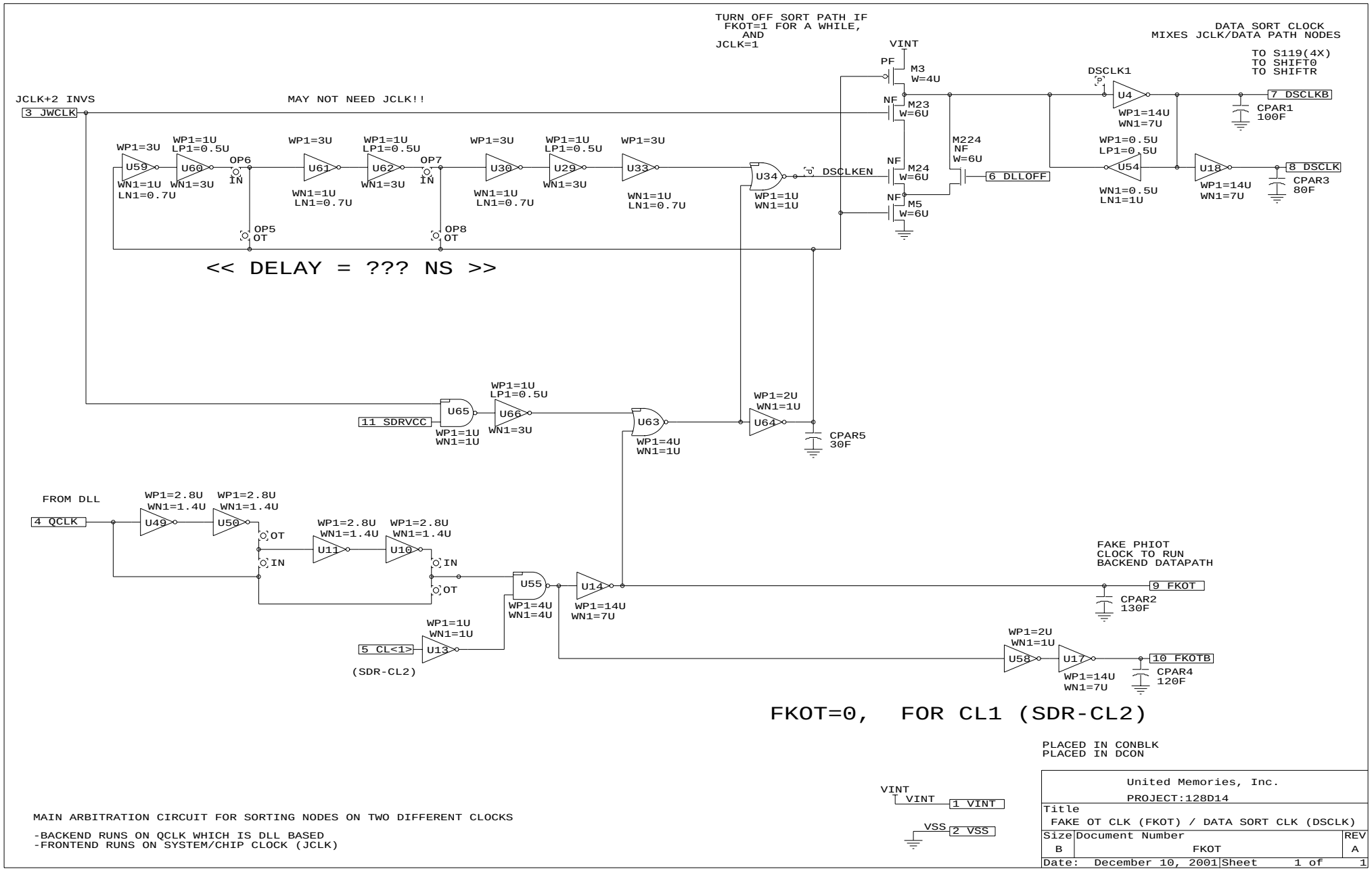


United Memories Inc. Project: 128D14		
Title SELECT CIRCUIT FOR V-MEAS MODES		
Size A	Document Number VMSELX	REV A
Date: November 1, 2001	Sheet 1 of 1	



PLACED IN CONBLK

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title DATA CONTROLLER (H/I/X CLKS & WEN)		
Size B	Document Number DCON	REV A
Date: December 7, 2001	Sheet 1 of 1	


TURN OFF SORT PATH IF
FKOT=1 FOR A WHILE,
AND
JCLK=1
DATA SORT CLOCK
MIXES JCLK/DATA PATH NODES
TO S119(4X)
TO SHIFT0
TO SHIFTR
VINT
PF
M3
W=4U
NF
M23
W=6U
NF
M24
W=6U
NF
M5
W=6U
M224
NF
W=6U
6 DLLOFF
DSCLK1
U4
WP1=14U
WN1=7U
7 DSCLKB
CPAR1
100F
WP1=0.5U
LP1=0.5U
U54
WN1=0.5U
LN1=1U
U18
WP1=14U
WN1=7U
8 DSCLK
CPAR3
80F
JCLK+2 INVS
3 JWCLK
MAY NOT NEED JCLK!!
WP1=3U
U59
WN1=1U
LN1=0.7U
WP1=1U
LP1=0.5U
U60
WN1=3U
OP6
IN
OP5
OT
WP1=3U
U61
WN1=1U
LN1=0.7U
WP1=1U
LP1=0.5U
U62
WN1=3U
OP7
IN
OP8
OT
WP1=3U
U30
WN1=1U
LN1=0.7U
WP1=1U
LP1=0.5U
U29
WN1=3U
WP1=3U
U33
WN1=1U
LN1=0.7U
U34
WP1=1U
WN1=1U
DSCLKEN
<< DELAY = ??? NS >>
WP1=1U
LP1=0.5U
U65
11 SDRVCC
WP1=1U
WN1=1U
U66
WN1=3U
U63
WP1=4U
WN1=1U
WP1=2U
WN1=1U
U64
CPAR5
30F
FROM DLL
4 QCLK
WP1=2.8U
WN1=1.4U
U49
WP1=2.8U
WN1=1.4U
U50
OT
IN
WP1=2.8U
WN1=1.4U
U11
WP1=2.8U
WN1=1.4U
U10
IN
OT
U55
WP1=4U
WN1=4U
U14
WP1=14U
WN1=7U
FAKE PHIOT
CLOCK TO RUN
BACKEND DATAPATH
9 FKOT
CPAR2
130F
WP1=1U
WN1=1U
5 CL<1>
U13
(SDR-CL2)
WP1=2U
WN1=1U
U58
U17
WP1=14U
WN1=7U
10 FKOTB
CPAR4
120F
FKOT=0, FOR CL1 (SDR-CL2)
PLACED IN CONBLK
PLACED IN DCON
VINT
VINT
1 VINT
VSS
2 VSS
MAIN ARBITRATION CIRCUIT FOR SORTING NODES ON TWO DIFFERENT CLOCKS
-BACKEND RUNS ON QCLK WHICH IS DLL BASED
-FRONTEND RUNS ON SYSTEM/CHIP CLOCK (JCLK)
United Memories, Inc.
PROJECT:128D14
Title
FAKE OT CLK (FKOT) / DATA SORT CLK (DSCLK)
Size
B
Document Number
FKOT
REV
A
Date: December 10, 2001
Sheet 1 of 1

FOR CL2.5,3 = JCLK

FOR CL2, =JCLKB

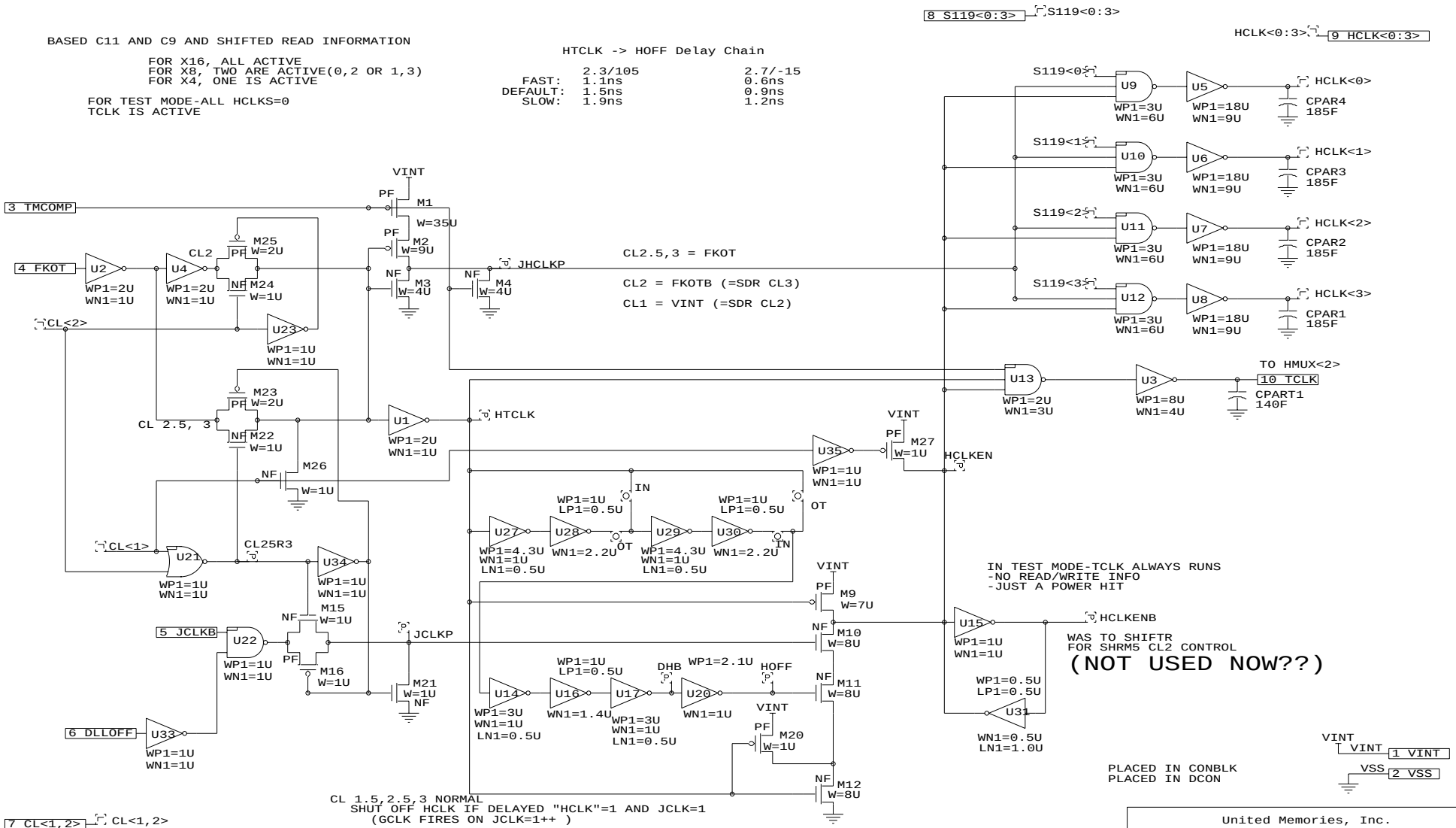
BASED C11 AND C9 AND SHIFTED READ INFORMATION

FOR X16, ALL ACTIVE
FOR X8, TWO ARE ACTIVE(0,2 OR 1,3)
FOR X4, ONE IS ACTIVE

FOR TEST MODE-ALL HCLKS=0
TCLK IS ACTIVE

HTCLK -> HOFF Delay Chain

	2.3/105	2.7/-15
FAST:	1.1ns	0.6ns
DEFAULT:	1.5ns	0.9ns
SLOW:	1.9ns	1.2ns



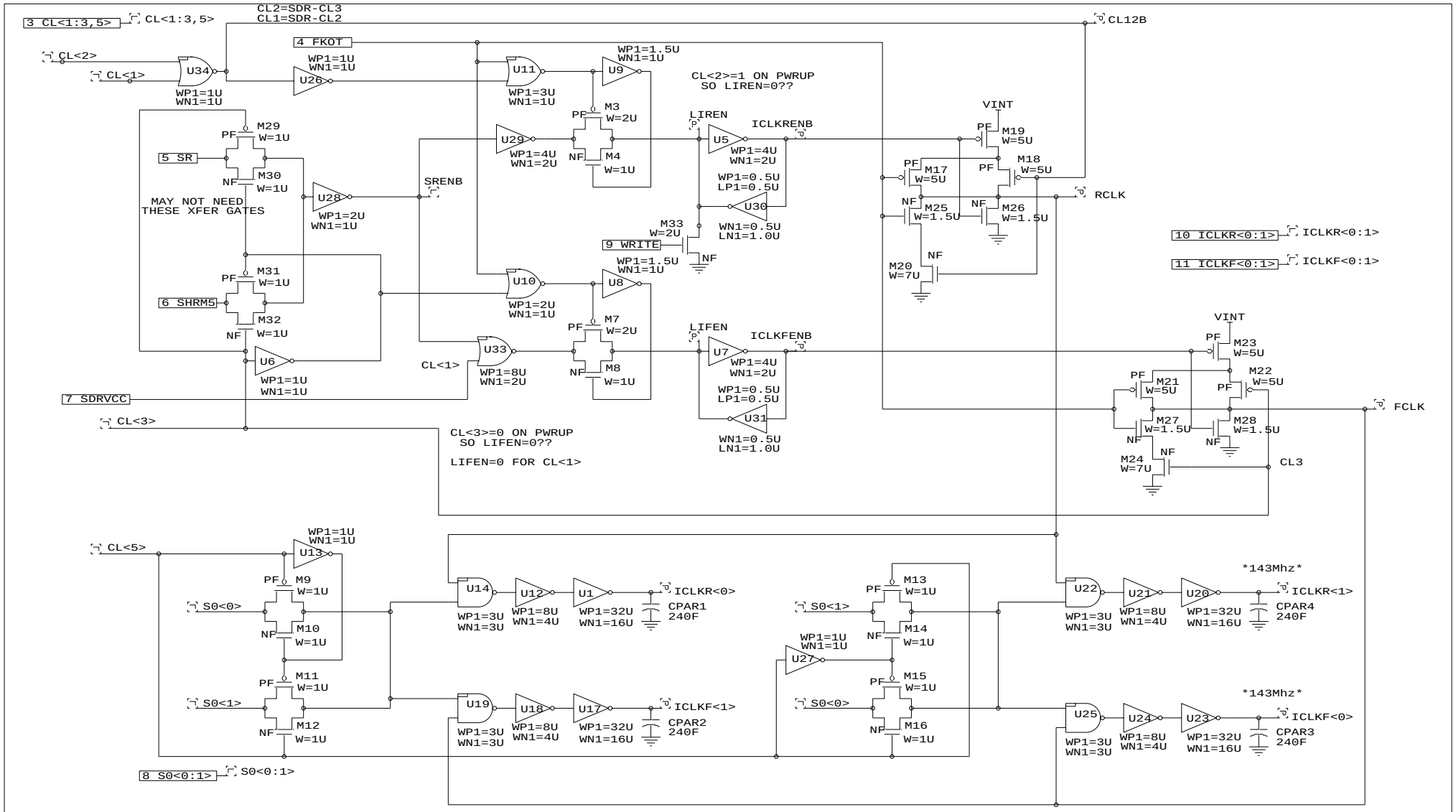
CL 1.5,2.5,3 NORMAL
SHUT OFF HCLK IF DELAYED "HCLK"=1 AND JCLK=1
(GCLK FIRES ON JCLK=1++)

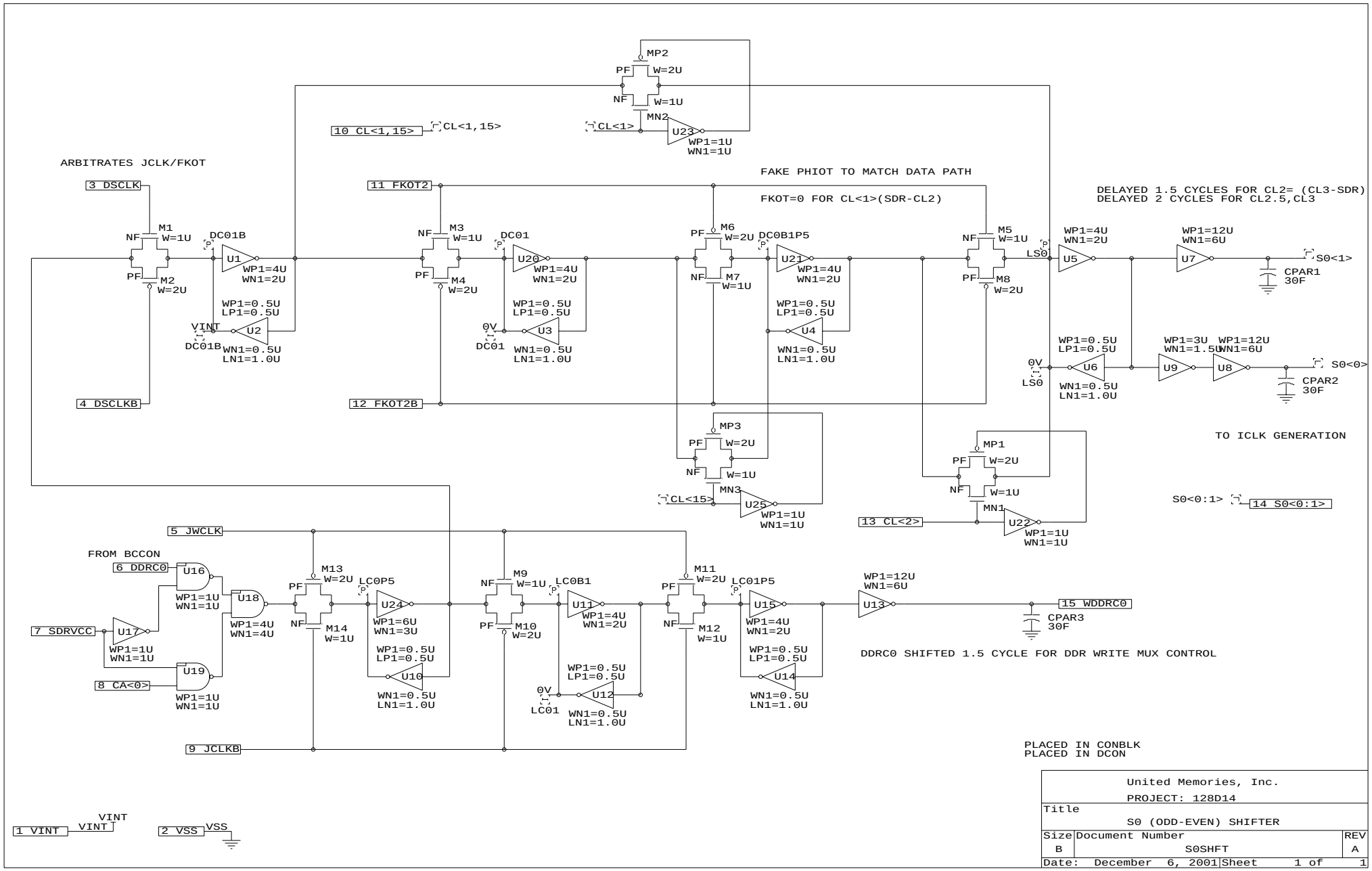
CL 1.5,2.5,3 DLL-OFF
SHUT OFF HCLK IF DELAYED "HCLK=1", MUST BE SHORTER THAN JCLK
(GCLK FIRES ON YCLK {JCLK=0} FOR DLL-OFF

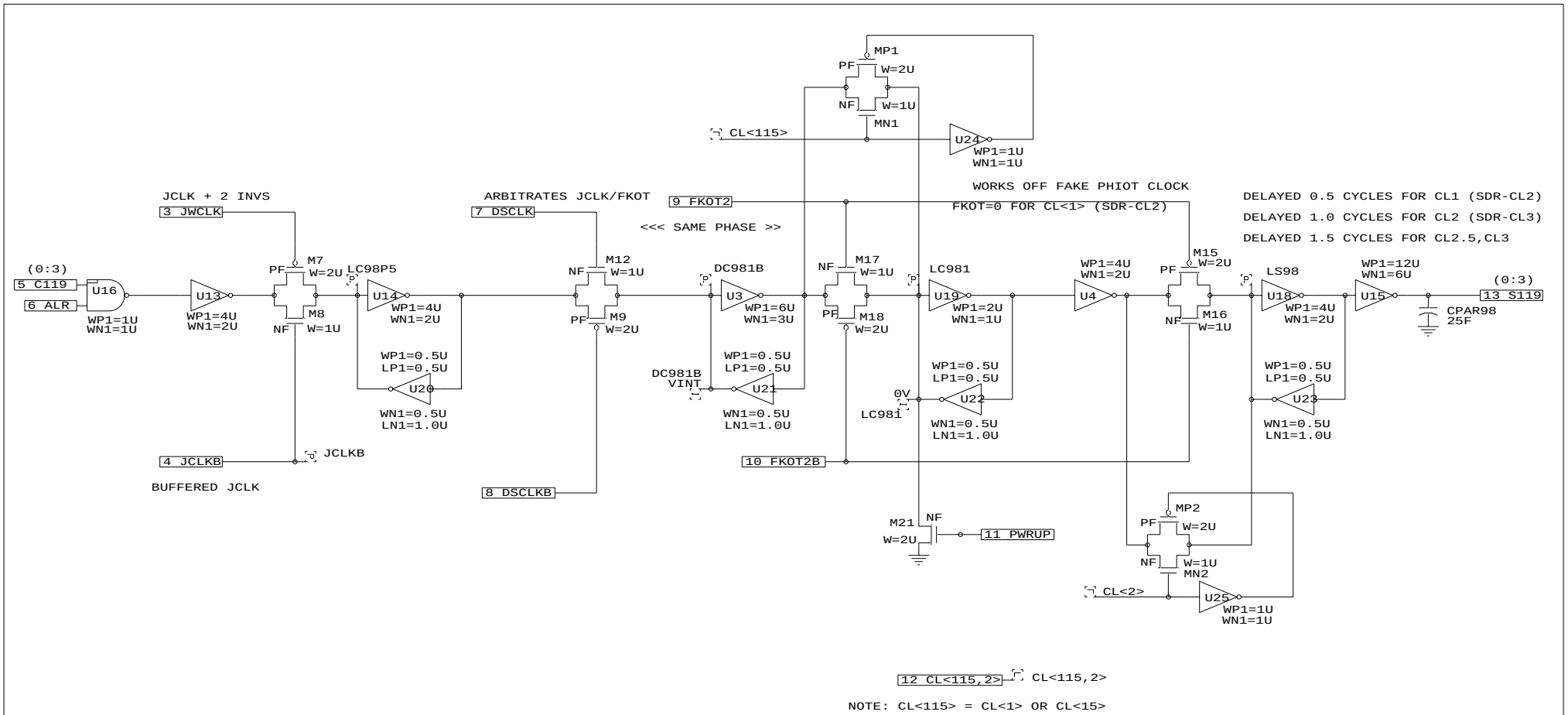
FOR CL2 - NO OFF CONTROL NEEDED

FOR CL1, HCLKEN=1 ALWAYS

United Memories, Inc.		
PROJECT: 128D14		
Title HCLK<0:3> /TCLK GENERATION		
Size B	Document Number HCLK	REV A
Date: December 10, 2001	Sheet 1 of 1	


3 CL<1:3,5>
CL<1:3,5>
CL2=SDR-CL3
CL1=SDR-CL2
CL12B
4 FKOT
CL<2>
CL<1>
U34
WP1=1U
WN1=1U
U26
WP1=1U
WN1=1U
U11
WP1=3U
WN1=1U
U9
WP1=1.5U
WN1=1U
CL<2>=1 ON PWRUP
SO LIREN=0??
M3
W=2U
PF
NF
M4
W=1U
U29
WP1=4U
WN1=2U
LIREN
U5
ICLKRENB
WP1=4U
WN1=2U
WP1=0.5U
LP1=0.5U
U30
WN1=0.5U
LN1=1.0U
M33
W=2U
9 WRITE
NF
VINT
M19
W=5U
M18
W=5U
M17
W=5U
M25
W=1.5U
M26
W=1.5U
RCLK
M20
W=7U
10 ICLKR<0:1>
ICLKR<0:1>
11 ICLKF<0:1>
ICLKF<0:1>
5 SR
M29
W=1U
M30
W=1U
MAY NOT NEED
THESE XFER GATES
U28
WP1=2U
WN1=1U
SRENB
M31
W=1U
M32
W=1U
6 SHRM5
U6
WP1=1U
WN1=1U
U10
WP1=2U
WN1=1U
U8
WP1=1.5U
WN1=1U
M7
W=2U
M8
W=1U
U33
WP1=8U
WN1=2U
CL<1>
LIFEN
U7
ICLKFENB
WP1=4U
WN1=2U
WP1=0.5U
LP1=0.5U
U31
WN1=0.5U
LN1=1.0U
7 SDRVCC
CL<3>
CL<3>=0 ON PWRUP
SO LIFEN=0??
LIFEN=0 FOR CL<1>
M23
W=5U
M22
W=5U
M21
W=5U
M27
W=1.5U
M28
W=1.5U
M24
W=7U
FCLK
CL3
CL<5>
U13
WP1=1U
WN1=1U
M9
W=1U
M10
W=1U
S0<0>
M11
W=1U
M12
W=1U
S0<1>
8 S0<0:1>
S0<0:1>
U14
WP1=3U
WN1=3U
U12
WP1=8U
WN1=4U
U1
WP1=32U
WN1=16U
ICLKR<0>
CPAR1
240F
U19
WP1=3U
WN1=3U
U18
WP1=8U
WN1=4U
U17
WP1=32U
WN1=16U
ICLKF<1>
CPAR2
240F
M13
W=1U
M14
W=1U
S0<1>
U27
WP1=1U
WN1=1U
M15
W=1U
M16
W=1U
S0<0>
U22
WP1=3U
WN1=3U
U21
WP1=8U
WN1=4U
U20
WP1=32U
WN1=16U
143Mhz
ICLKR<1>
CPAR4
240F
U25
WP1=3U
WN1=3U
U24
WP1=8U
WN1=4U
U23
WP1=32U
WN1=16U
143Mhz
ICLKF<0>
CPAR3
240F
VINT
VINT
1 VINT
VSS
2 VSS
RISING EDGE DATA SORT CLOCK
PLACED IN CONBLK
PLACED IN DCON
United Memories, Inc.
PROJECT: 128D14
Title
ICLK R AND F GENERATION
Size
B
Document Number
ICLK
REV
A
Date: December 6, 2001
Sheet 1 of 1


ARBITRATES JCLK/FKOT
3 DSCLK
4 DSCLKB
M1 W=1U
M2 W=2U
NF
PF
DC01B
U1
WP1=4U WN1=2U
WP1=0.5U LP1=0.5U
VINT
U2
DC01B
WN1=0.5U LN1=1.0U
10 CL<1,15>
CL<1,15>
MP2
PF W=2U
NF W=1U
MN2
CL<1>
U23
WP1=1U WN1=1U
FAKE PHIOT TO MATCH DATA PATH
FKOT=0 FOR CL<1>(SDR-CL2)
11 FKOT2
12 FKOT2B
M3 W=1U
M4 W=2U
DC01
U20
WP1=4U WN1=2U
WP1=0.5U LP1=0.5U
0V
DC01
U3
WN1=0.5U LN1=1.0U
M6 W=2U
M7 W=1U
DC0B1P5
U21
WP1=4U WN1=2U
WP1=0.5U LP1=0.5U
U4
WN1=0.5U LN1=1.0U
M5 W=1U
M8 W=2U
LS0
DELAYED 1.5 CYCLES FOR CL2= (CL3-SDR)
DELAYED 2 CYCLES FOR CL2.5,CL3
U5
WP1=4U WN1=2U
U7
WP1=12U WN1=6U
S0<1>
CPAR1 30F
WP1=0.5U LP1=0.5U
0V
LS0
U6
WN1=0.5U LN1=1.0U
U9
WP1=3U WN1=1.5U
U8
WP1=12U WN1=6U
S0<0>
CPAR2 30F
TO ICLK GENERATION
MP3
PF W=2U
NF W=1U
MN3
CL<15>
U25
WP1=1U WN1=1U
MP1
PF W=2U
NF W=1U
MN1
13 CL<2>
U22
WP1=1U WN1=1U
S0<0:1>
14 S0<0:1>
5 JWCLK
FROM BCCON
6 DDRC0
U16
WP1=1U WN1=1U
U18
WP1=4U WN1=4U
7 SDRVCC
U17
WP1=1U WN1=1U
U19
WP1=1U WN1=1U
8 CA<0>
M13 W=2U
M14 W=1U
LC0P5
U24
WP1=6U WN1=3U
WP1=0.5U LP1=0.5U
U10
WN1=0.5U LN1=1.0U
M9 W=1U
M10 W=2U
LC0B1
U11
WP1=4U WN1=2U
WP1=0.5U LP1=0.5U
0V
LC01
U12
WN1=0.5U LN1=1.0U
M11 W=2U
M12 W=1U
LC01P5
U15
WP1=4U WN1=2U
WP1=0.5U LP1=0.5U
U14
WN1=0.5U LN1=1.0U
WP1=12U WN1=6U
U13
15 WDDRC0
CPAR3 30F
DDRC0 SHIFTED 1.5 CYCLE FOR DDR WRITE MUX CONTROL
9 JCLKB
PLACED IN CONBLK
PLACED IN DCON
1 VINT
VINT
2 VSS
VSS
United Memories, Inc.
PROJECT: 128D14
Title
S0 (ODD-EVEN) SHIFTER
Size B
Document Number S0SHFT
REV A
Date: December 6, 2001
Sheet 1 of 1



ALR=AT LEAST ONE BANK IS READING

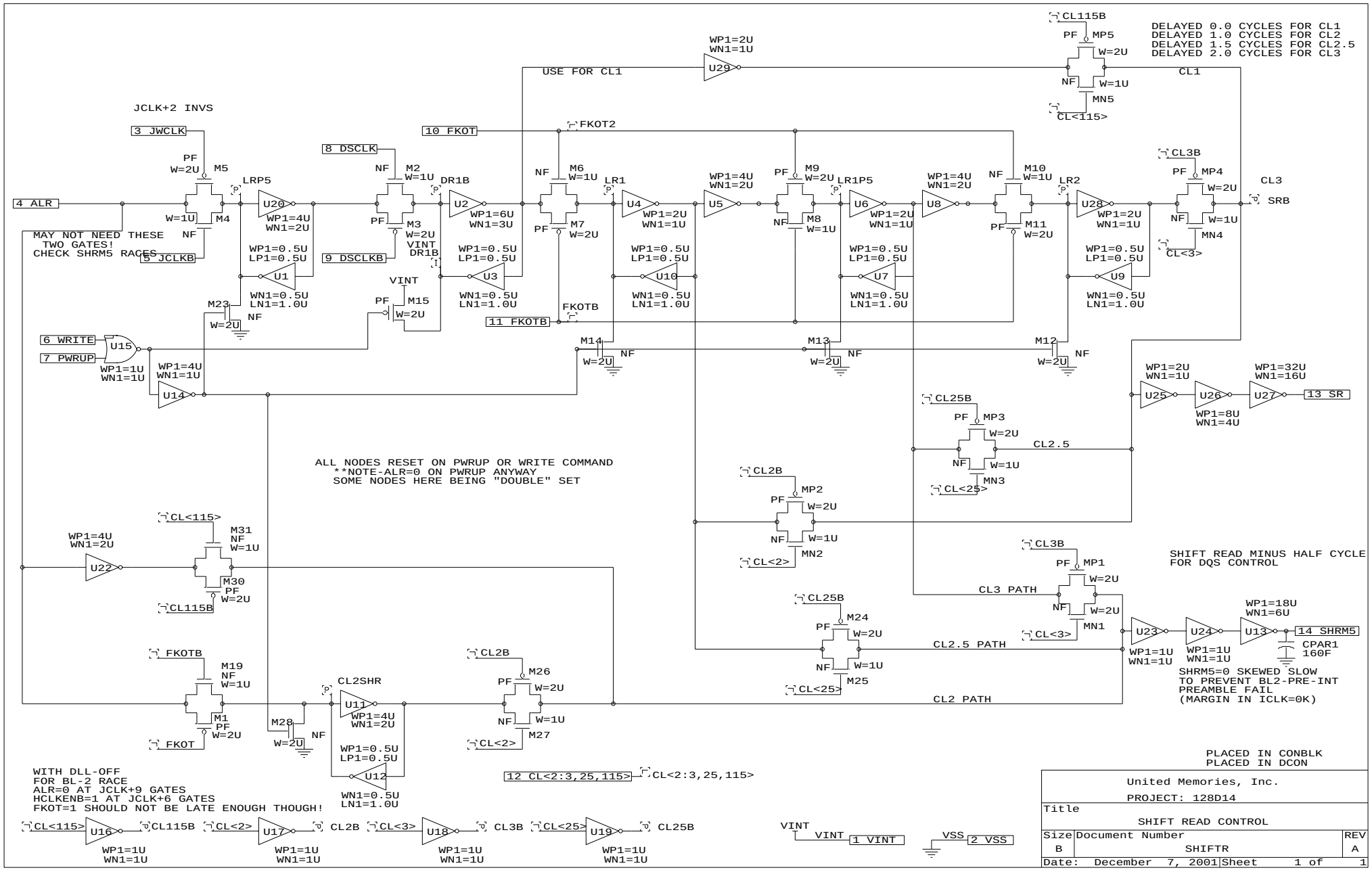
FOR USE IN CONTROLLING HCLKS
(X4/X8/X16) MUXING STAGE OF THE PIPELINE

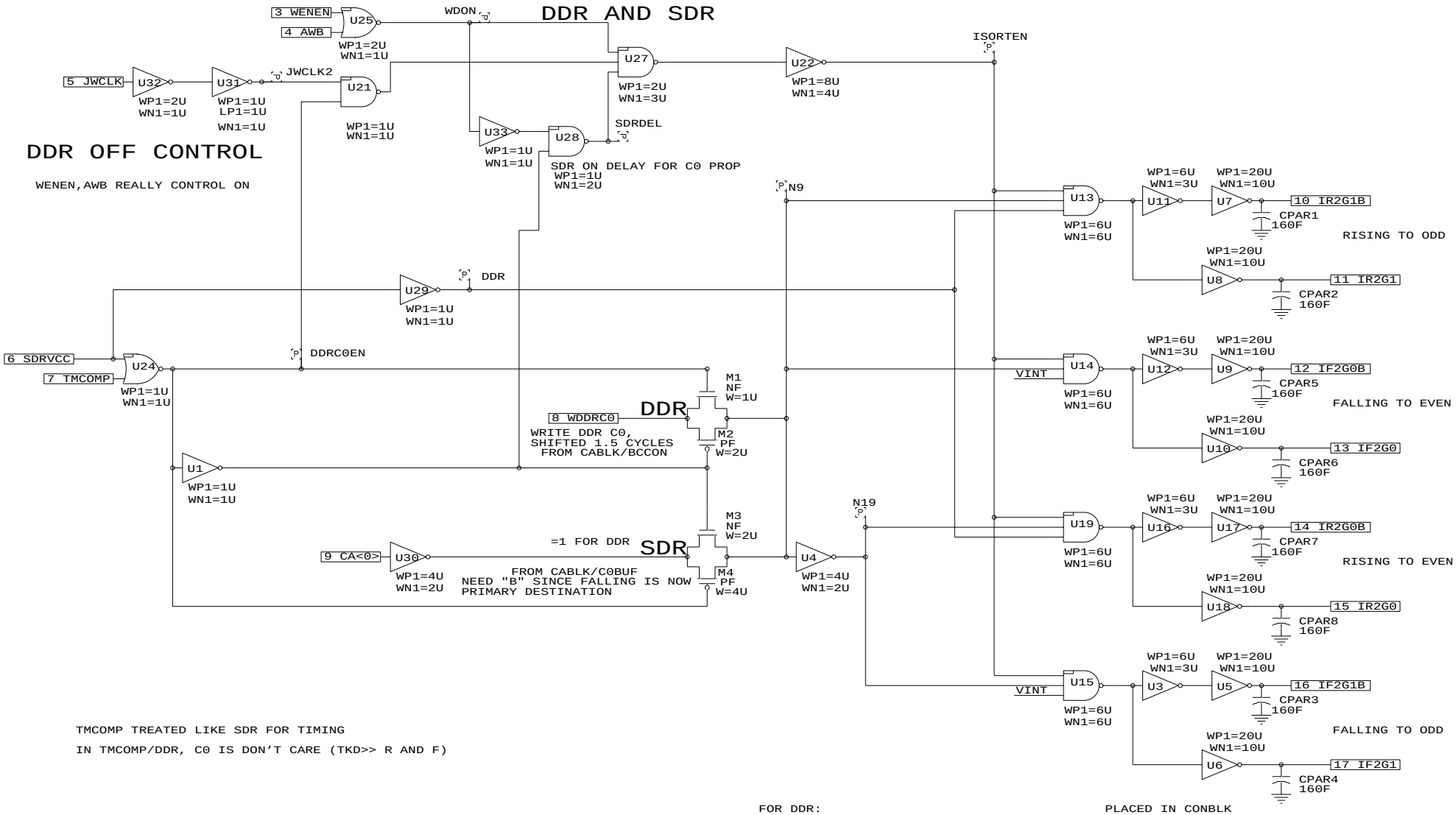
LREAD INFORMATION
IS EMBEDDED INSIDE S119

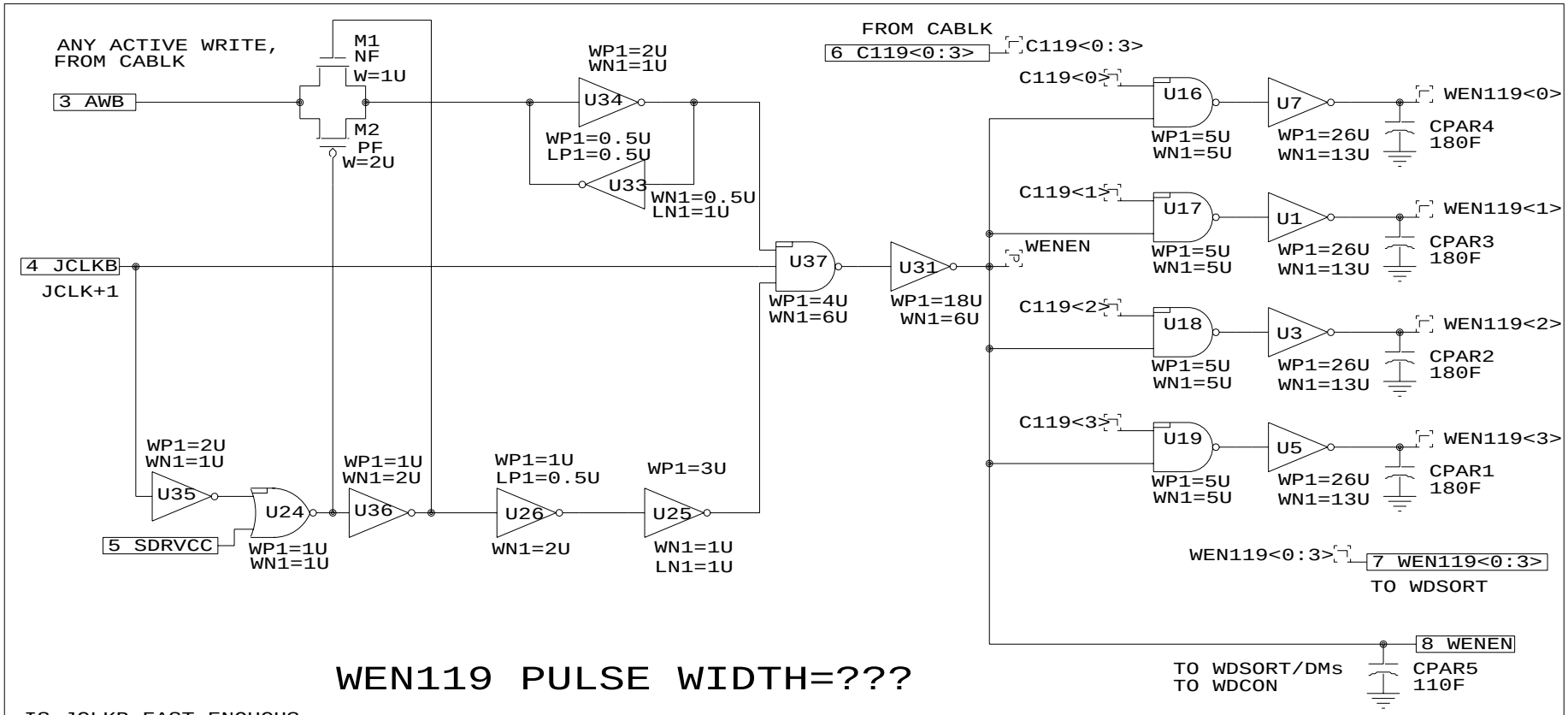
VINT
VINT
1 VINT
VSS
2 VSS

PLACED IN DCON

United Memories, Inc.		
PROJECT: 128D14		
Title C11 C9 SHIFTER (4X) <0:3>		
Size B	Document Number S119	REV A
Date: December 6, 2001	Sheet 1 of 1	


DELAYED 0.0 CYCLES FOR CL1
DELAYED 1.0 CYCLES FOR CL2
DELAYED 1.5 CYCLES FOR CL2.5
DELAYED 2.0 CYCLES FOR CL3
JCLK+2 INVS
USE FOR CL1
MAY NOT NEED THESE TWO GATES! CHECK SHRM5 RACES
ALL NODES RESET ON PWRUP OR WRITE COMMAND
**NOTE-ALR=0 ON PWRUP ANYWAY
SOME NODES HERE BEING "DOUBLE" SET
SHIFT READ MINUS HALF CYCLE FOR DQS CONTROL
CL3 PATH
CL2.5 PATH
CL2 PATH
SHRM5=0 SKEWED SLOW TO PREVENT BL2-PRE-INT PREAMBLE FAIL (MARGIN IN ICLK=0K)
WITH DLL-OFF FOR BL-2 RACE
ALR=0 AT JCLK+9 GATES
HCLKENB=1 AT JCLK+6 GATES
FKOT=1 SHOULD NOT BE LATE ENOUGH THOUGH!
PLACED IN CONBLK
PLACED IN DCON
United Memories, Inc.
PROJECT: 128D14
Title
SHIFT READ CONTROL
Size B
Document Number SHIFTR
REV A
Date: December 7, 2001
Sheet 1 of 1


DDR AND SDR
DDR OFF CONTROL
WENEN,AWB REALLY CONTROL ON
3 WENEN
4 AWB
5 JWCLK
6 SDRVCC
7 TMCOMP
8 WDDRC0
9 CA<0>
10 IR2G1B
11 IR2G1
12 IF2G0B
13 IF2G0
14 IR2G0B
15 IR2G0
16 IF2G1B
17 IF2G1
WDON
JWCLK2
DDRC0EN
DDR
SDRDEL
ISORTEN
N9
N19
VINT
U25 WP1=2U WN1=1U
U32 WP1=2U WN1=1U
U31 WP1=1U LP1=1U WN1=1U
U21 WP1=1U WN1=1U
U33 WP1=1U WN1=1U
U28 WP1=1U WN1=2U
SDR ON DELAY FOR C0 PROP
U27 WP1=2U WN1=3U
U22 WP1=8U WN1=4U
U29 WP1=1U WN1=1U
U24 WP1=1U WN1=1U
U1 WP1=1U WN1=1U
U30 WP1=4U WN1=2U
U4 WP1=4U WN1=2U
M1 NF W=1U
M2 PF W=2U
M3 NF W=2U
M4 PF W=4U
DDR
WRITE DDR C0, SHIFTED 1.5 CYCLES FROM CABLK/BCCON
SDR
=1 FOR DDR
FROM CABLK/C0BUF
NEED "B" SINCE FALLING IS NOW PRIMARY DESTINATION
U13 WP1=6U WN1=6U
U14 WP1=6U WN1=6U
U19 WP1=6U WN1=6U
U15 WP1=6U WN1=6U
U11 WP1=6U WN1=3U
U12 WP1=6U WN1=3U
U16 WP1=6U WN1=3U
U3 WP1=6U WN1=3U
U7 WP1=20U WN1=10U
U8 WP1=20U WN1=10U
U9 WP1=20U WN1=10U
U10 WP1=20U WN1=10U
U17 WP1=20U WN1=10U
U18 WP1=20U WN1=10U
U5 WP1=20U WN1=10U
U6 WP1=20U WN1=10U
CPAR1 160F
CPAR2 160F
CPAR5 160F
CPAR6 160F
CPAR7 160F
CPAR8 160F
CPAR3 160F
CPAR4 160F
RISING TO ODD
FALLING TO EVEN
RISING TO EVEN
FALLING TO ODD
TMCOMP TREATED LIKE SDR FOR TIMING
IN TMCOMP/DDR, C0 IS DON'T CARE (TKD>> R AND F)
VINT
1 VINT
VSS
2 VSS
RISING PATH DISABLED FOR SDR
SINCE DQS HAS BEEN REMOVED FROM SORT TIMING, UPPER AND LOWER CAN BE COMBINED
FOR DDR:
ENABLE SORT IFF,
JCLK=0 AND WENEN=0
(LOOK AT DDRC0 SHIFTED 1.5)
(SHOULD BE FAST OFF,SLOW ON)
FOR SDR: (OR TMCOMP)
ENABLE SORT IFF,
JCLK=1 ++ (ALLOW C0 TO CHANGE)
(LOOK AT C0 STRAIGHT FROM C0BUF)
(SHOULD BE SLOW OFF,SLOW ON)
PLACED IN CONBLK
PLACED IN DCON
United Memories, Inc.
PROJECT: 128D14
Title
WRITE DATA CONTROL (C0 SORTING)
Size B
Document Number WDCON
REV A
Date: December 21, 2001
Sheet 1 of 1



WEN119 PULSE WIDTH=???

IS JCLKB FAST ENOUGH?

JCLK-JCLKW=1
JCLKB-WENEN=2
WENEN-DM=3
DM-DMB=1
========
JCLK-DMB=7

JCLK-YCLK=3
YCLK-YCLKW=8
YCLKW-YW119=2
=======
JCLK-YW119=13

JCLK-GDATA=9

x= 119 for 128m
98 for 64m

BASED C11 AND C9 INFORMATION (9,8 for 64m)

FOR X16, ALL ACTIVE
FOR X8, TWO ARE ACTIVE(0,2 OR 1,3)
FOR X4, ONE IS ACTIVE

PLACED IN CONBLK
PLACED IN DCON

VINT
VINT — 1 VINT
VSS — 2 VSS

United Memories, Inc. PROJECT: 128D14		
Title WEN119<0:3> GENERATION		
Size A	Document Number WEN119	REV A
Date: October 16, 2001	Sheet 1 of 1	

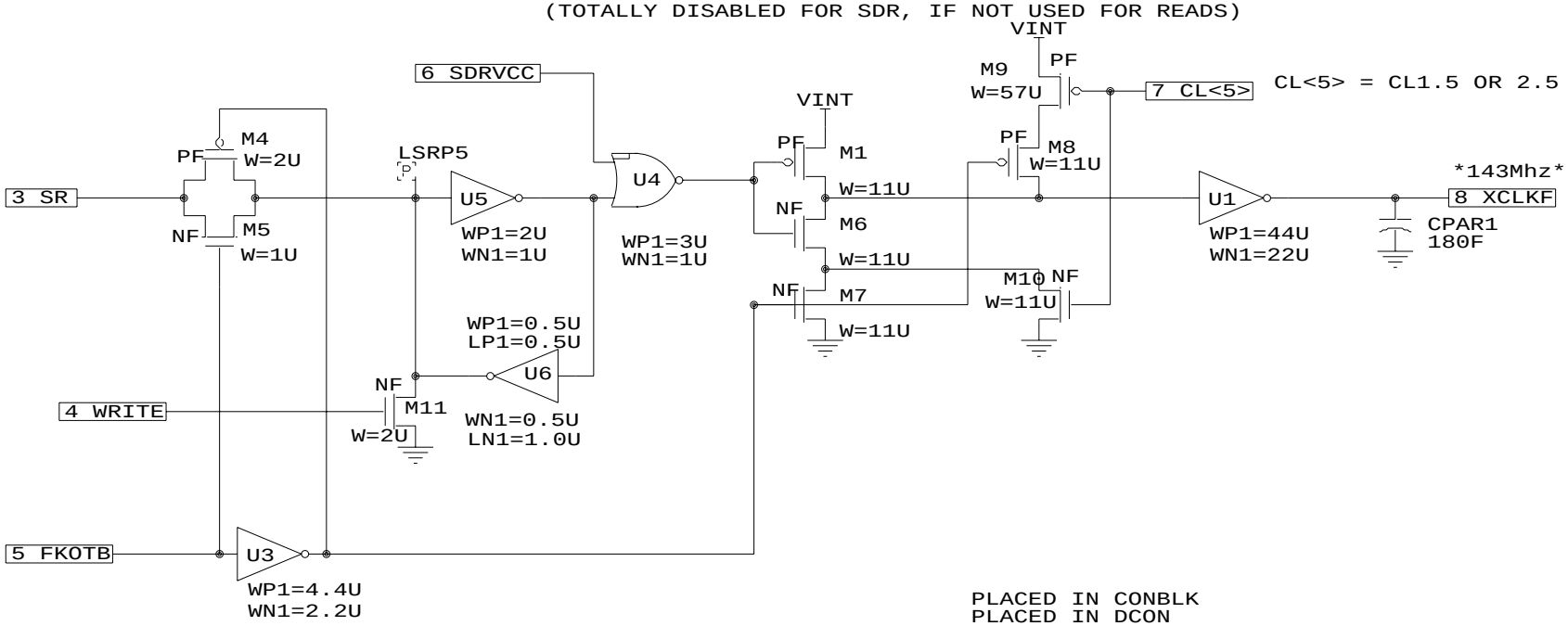
ACTIVE HIGH

EXTRA CLOCK IN FALLING PATH FOR CL3 AND CL2

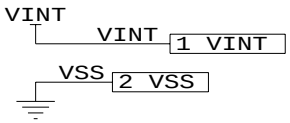
=DC-ON FOR CL2.5

THIS CLOCK ALWAYS TOGGLES, READS/WRITES/IDLE

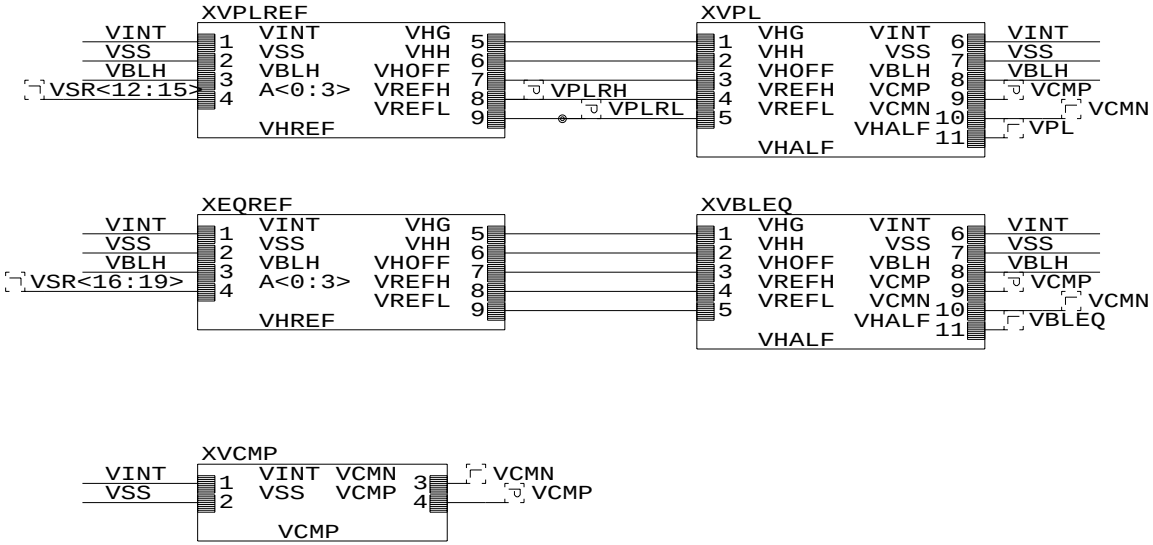
(TOTALLY DISABLED FOR SDR, IF NOT USED FOR READS)



PLACED IN CONBLK
PLACED IN DCON



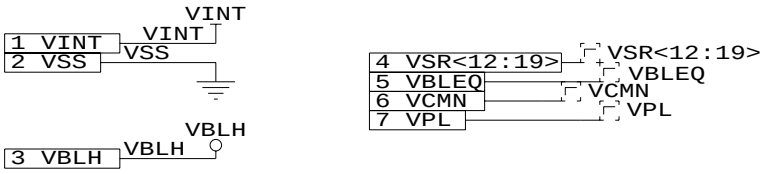
United Memories, Inc. PROJECT: 128D14		
Title XCLKF GENERATION		
Size A	Document Number XCLKF	REV A
Date: December 7, 2001	Sheet 1 of 1	



SEE TEST MODE DOCUMENTATION FOR VPL VS VSR<12:15>
SEE TEST MODE DOCUMENTATION FOR VBLEQ VS VSR<16:19>

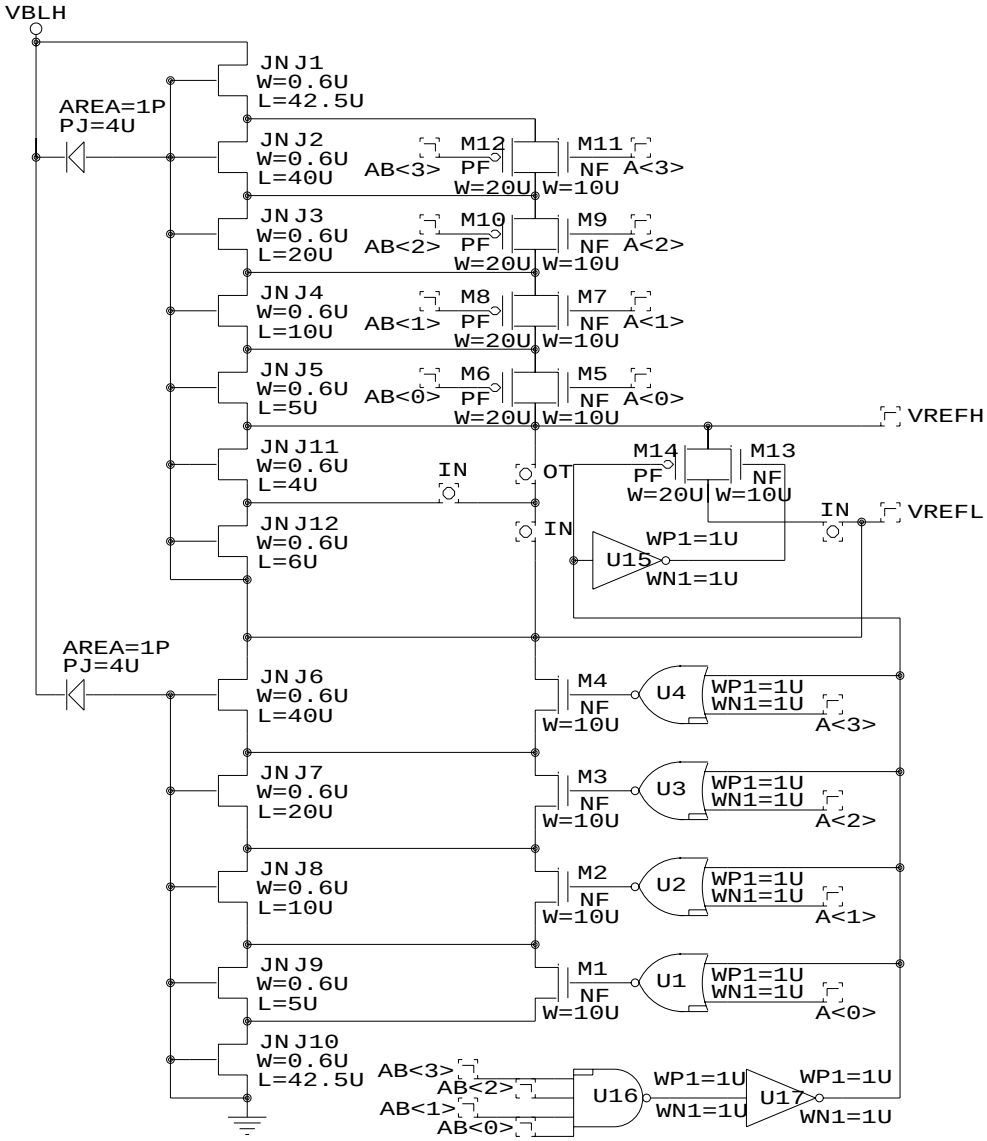
Inputs: VSR<12:19> (Voltage Set Registers 3 and 4)
VCMN (Voltage Current Mirror N-type from VREFBG)

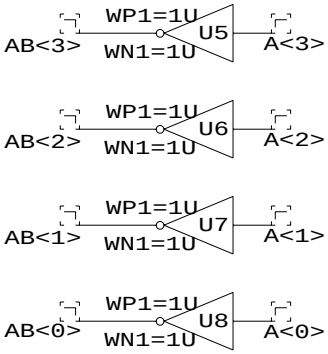
Outputs: VPL (Voltage PLate to memory cell array)
VBLEQ (Voltage to the BitLine precharge node.)

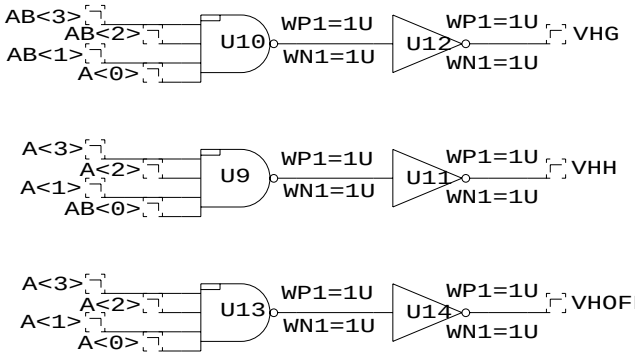


PLACED IN LMISC

United Memories Inc.		Confidential
Project: 128D14		
Title HALF VBLH GENERATORS FOR VBLEQ/VPL		
Size A	Document Number VHBLH	REV A
Date: September 4, 2001	Sheet 1 of 1	





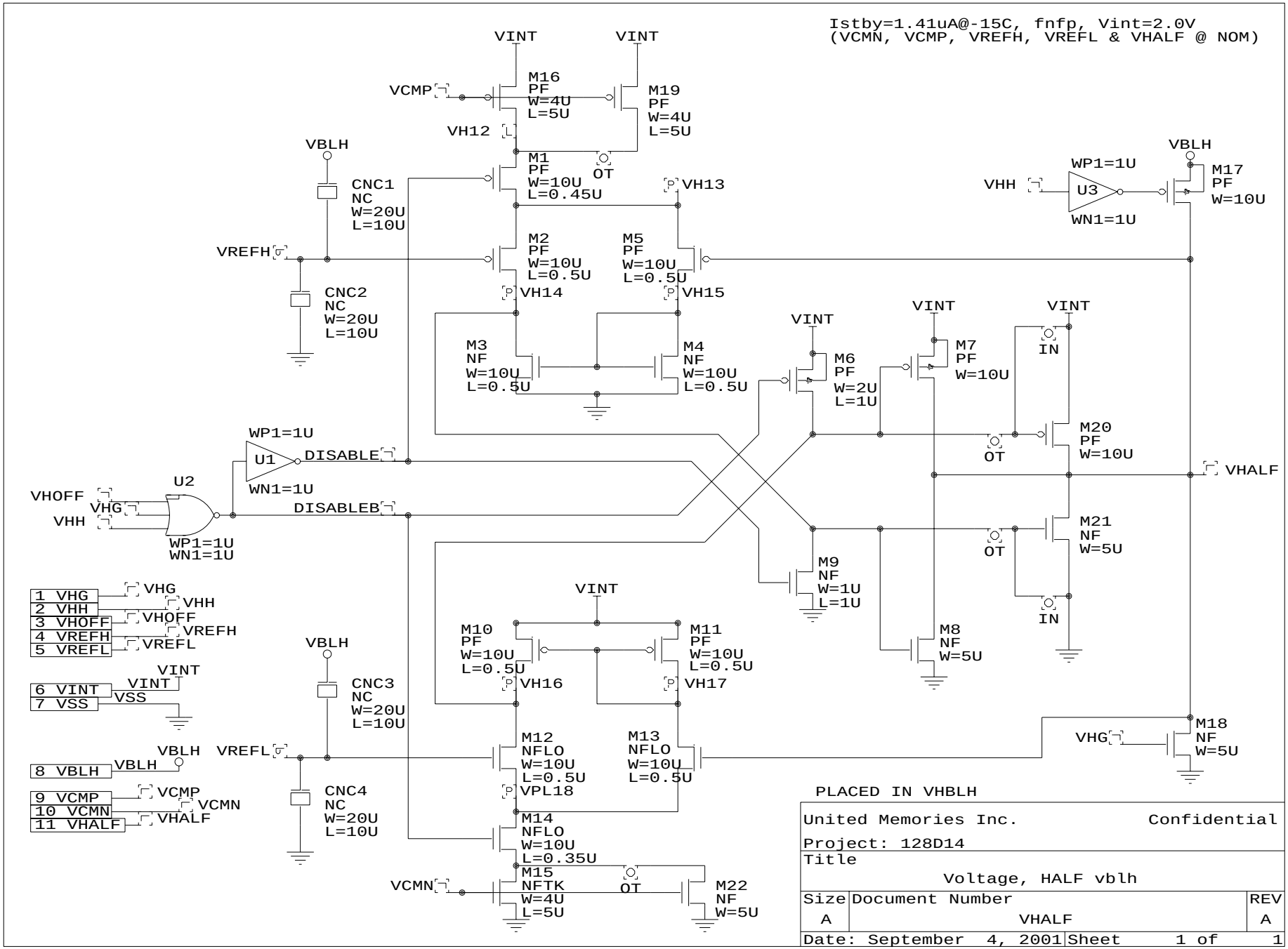


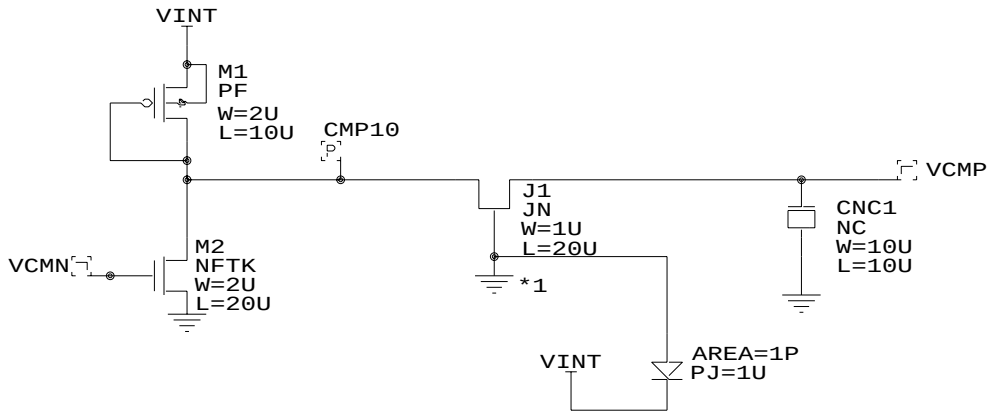
Istby=1.74uA @ 105C, VBLH=1.6V
Istby=1.64uA @ -15C, VBLH=1.6V

When using the VBLEQ test modes to write weak ones or zeros into the cell, a background pattern of 50% ones and 50% zeros should be written beforehand to prevent excessive VBLEQ current spikes.

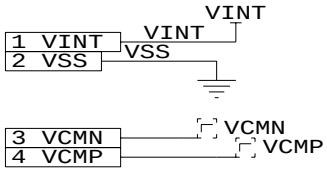
PLACED IN VHBLH

United Memories Inc.		Confidential
Project: 128D14		
Title	Voltage, Half vblh REFerence	
Size A	Document Number VHREF	REV A
Date: September 4, 2001	Sheet 1 of 1	


Istby=1.41uA@-15C, fnfp, Vint=2.0V
(VCMN, VCMP, VREFH, VREFL & VHALF @ NOM)
VINT
VINT
VCMP
M16
PF
W=4U
L=5U
M19
PF
W=4U
L=5U
VH12
VBLH
M1
PF
W=10U
L=0.45U
OT
CNC1
NC
W=20U
L=10U
VH13
VREFH
M2
PF
W=10U
L=0.5U
M5
PF
W=10U
L=0.5U
VH14
VH15
CNC2
NC
W=20U
L=10U
M3
NF
W=10U
L=0.5U
M4
NF
W=10U
L=0.5U
VINT
M6
PF
W=2U
L=1U
VINT
M7
PF
W=10U
VINT
IN
M20
PF
W=10U
OT
VHALF
VBLH
WP1=1U
VHH
U3
WN1=1U
M17
PF
W=10U
WP1=1U
U1
DISABLE
WN1=1U
U2
VHOFF
VHG
VHH
DISABLEB
WP1=1U
WN1=1U
M21
NF
W=5U
OT
M9
NF
W=1U
L=1U
IN
M8
NF
W=5U
1 VHG
2 VHH
3 VHOFF
4 VREFH
5 VREFL
VHG
VHH
VHOFF
VREFH
VREFL
VINT
M10
PF
W=10U
L=0.5U
M11
PF
W=10U
L=0.5U
VH16
VH17
VINT
6 VINT
7 VSS
VINT
VSS
VBLH
CNC3
NC
W=20U
L=10U
M18
NF
W=5U
VHG
VBLH
8 VBLH
VBLH
VREFL
M12
NFLO
W=10U
L=0.5U
M13
NFLO
W=10U
L=0.5U
VPL18
9 VCMP
10 VCMN
11 VHALF
VCMP
VCMN
VHALF
CNC4
NC
W=20U
L=10U
M14
NFLO
W=10U
L=0.35U
M15
NFTK
W=4U
L=5U
OT
VCMN
M22
NF
W=5U
PLACED IN VHBLH
United Memories Inc.
Confidential
Project: 128D14
Title
Voltage, HALF vblh
Size
A
Document Number
VHALF
REV
A
Date: September 4, 2001
Sheet 1 of 1



VCMP=1.1651V & I=0.19uA @ 105C, fnfp, VCMN=0.9063V
VCMP=1.1112V & I=0.13uA @ -15C, fnfp, VCMN=0.9587V
(The VCMN above is as simulated for that condition)

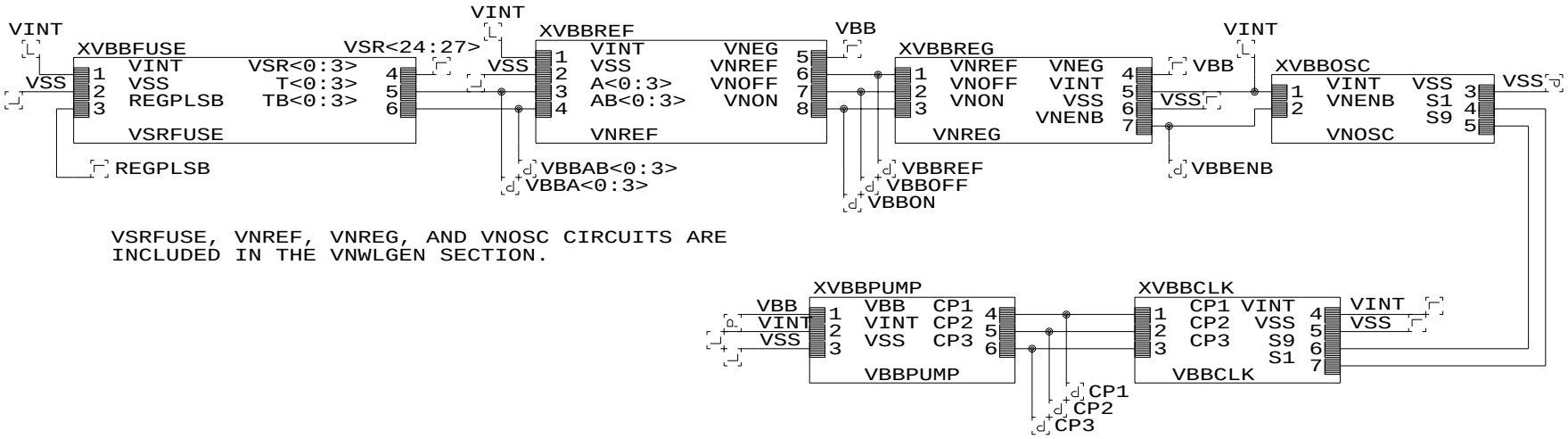


PLACED IN VHBLH

United Memories Inc.		Confidential
Project: 128D14		
Title	Voltage Current Mirror P-type	
Size A	Document Number VCMP	REV A
Date: September 4, 2001	Sheet 1 of 1	

Description: This circuit generates a bias voltage for a PF transistor to provide a load current of less than 1uA.

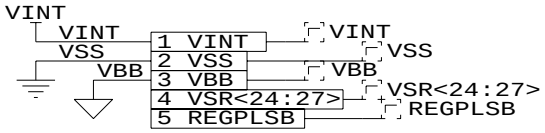
Inputs: VCMN (Voltage Current Mirror N-type from VREFBG)
Outputs: VCMP (Voltage Current Mirror P-type from VPL)



VSRFUSE, VNREF, VNREG, AND VNOSC CIRCUITS ARE
INCLUDED IN THE VNWLGEN SECTION.

SEE TEST MODE DOCUMENTATION FOR VBB VS VSR<0:3>.

VNREF, VNREG, VNOSC
SHEETS ARE IN VNWLGEN SECTION

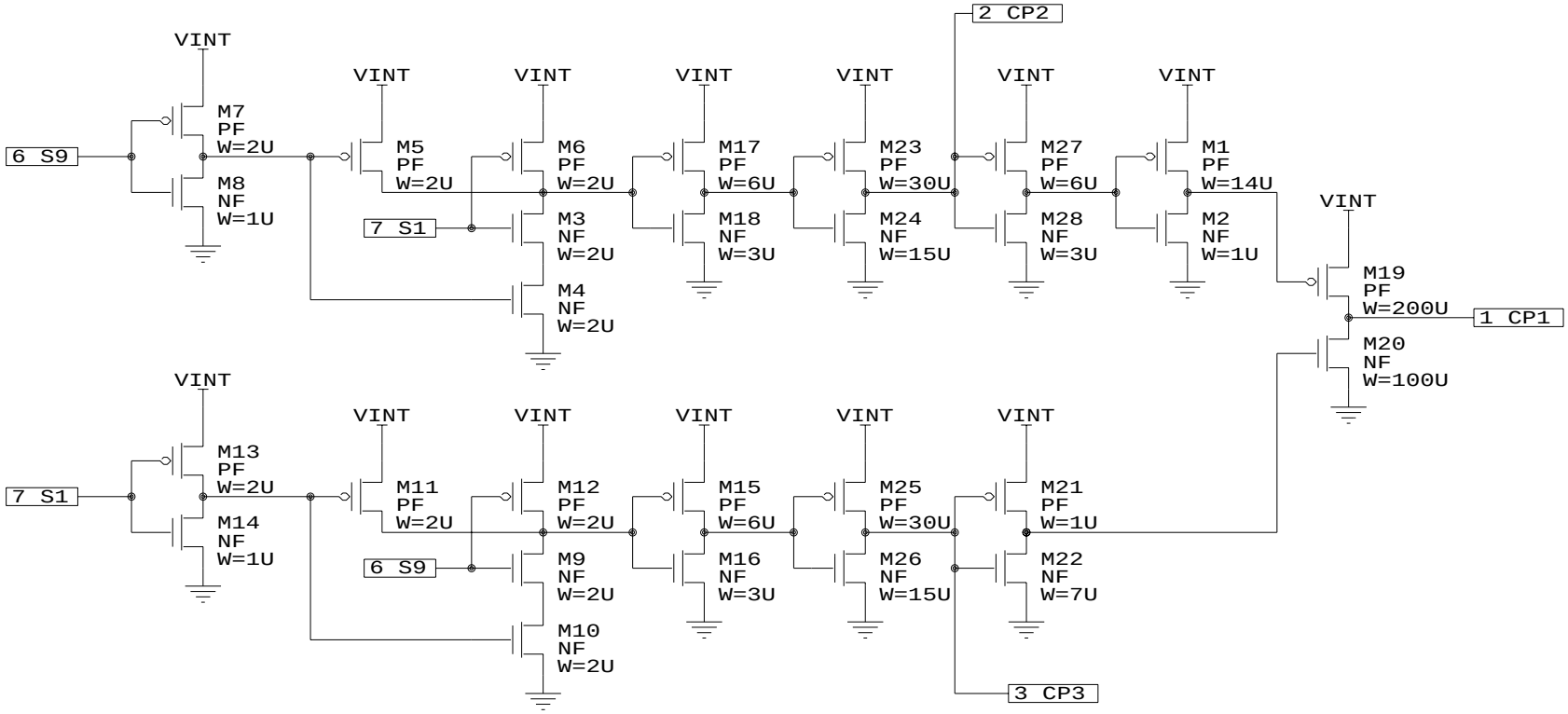


*Values are before parasitics have been added.

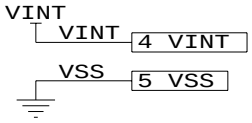
VBB Voltage	-0.3
Models	SlowSlow
Temperature	105
VCC Voltage	2.0
VBB Current	1.2mA*

PLACED IN RMISC

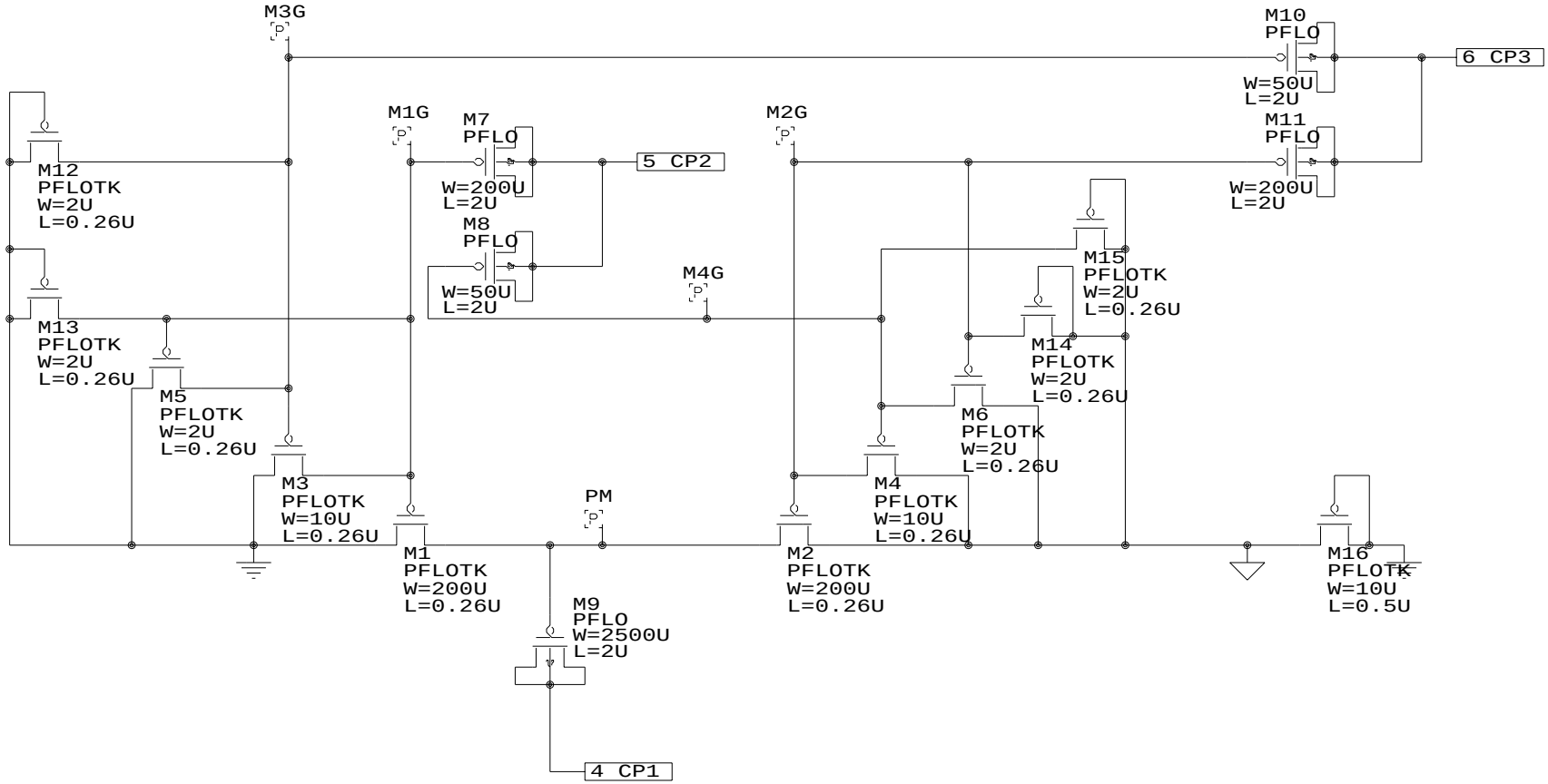
UNITED MEMORIES INC.		Confidential
PROJECT: 128D14		
Title	VBB GENERATOR	
Size A	Document Number VBBGEN	REV A
Date: September 4, 2001	Sheet 1 of 1	

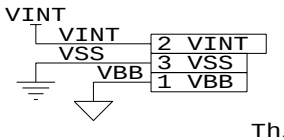


PLACED IN VBBGEN



UNITED MEMORIES INC.		Confidential
PROJECT: 128D14		
Title	VBB Pump Clocks	
Size A	Document Number VBBCLK	REV A
Date: September 4, 2001	Sheet 1 of 1	



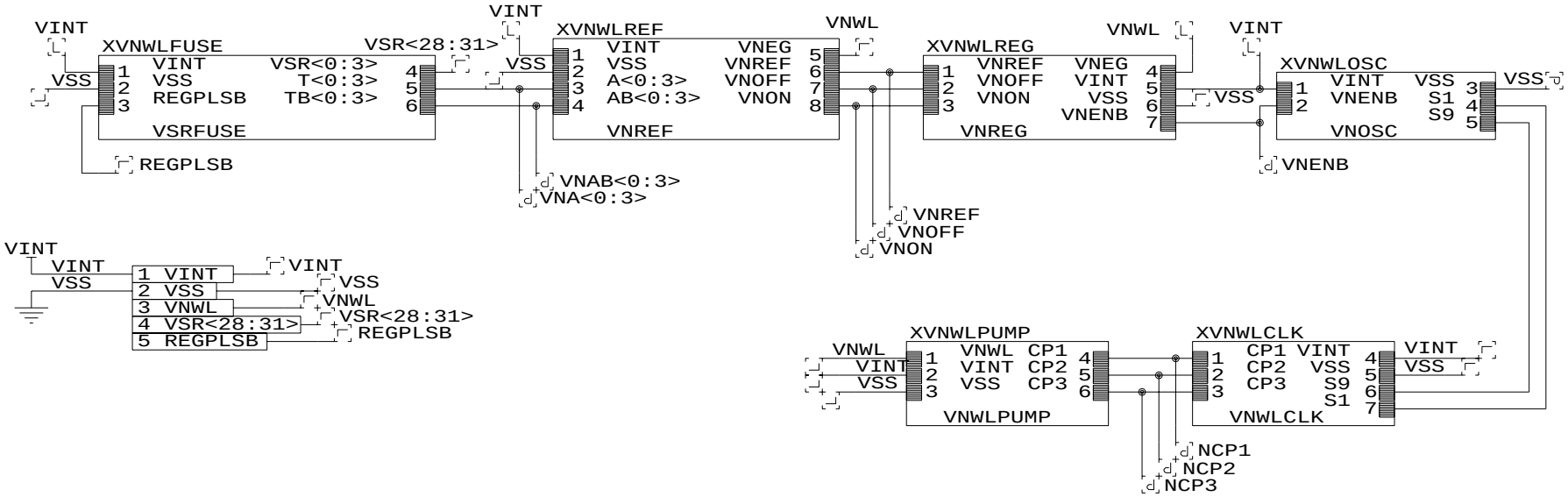


This pump is stopped with CP1 floating.
This pump is stopped with CP2 and CP3 high.

PLACED IN VBBGEN

UNITED MEMORIES INC.		Confidential
PROJECT: 128D14		
Title	Pump for Vbb Generator	
Size A	Document Number VBBPUMP	REV A
Date: September 7, 2001	Sheet 1 of 1	

SEE TEST MODE DOCUMENT FOR VBB VS VSR<4:7>



*Values are before parasitics have been added.

VNWLL Voltage -0.3

Models SlowSlow

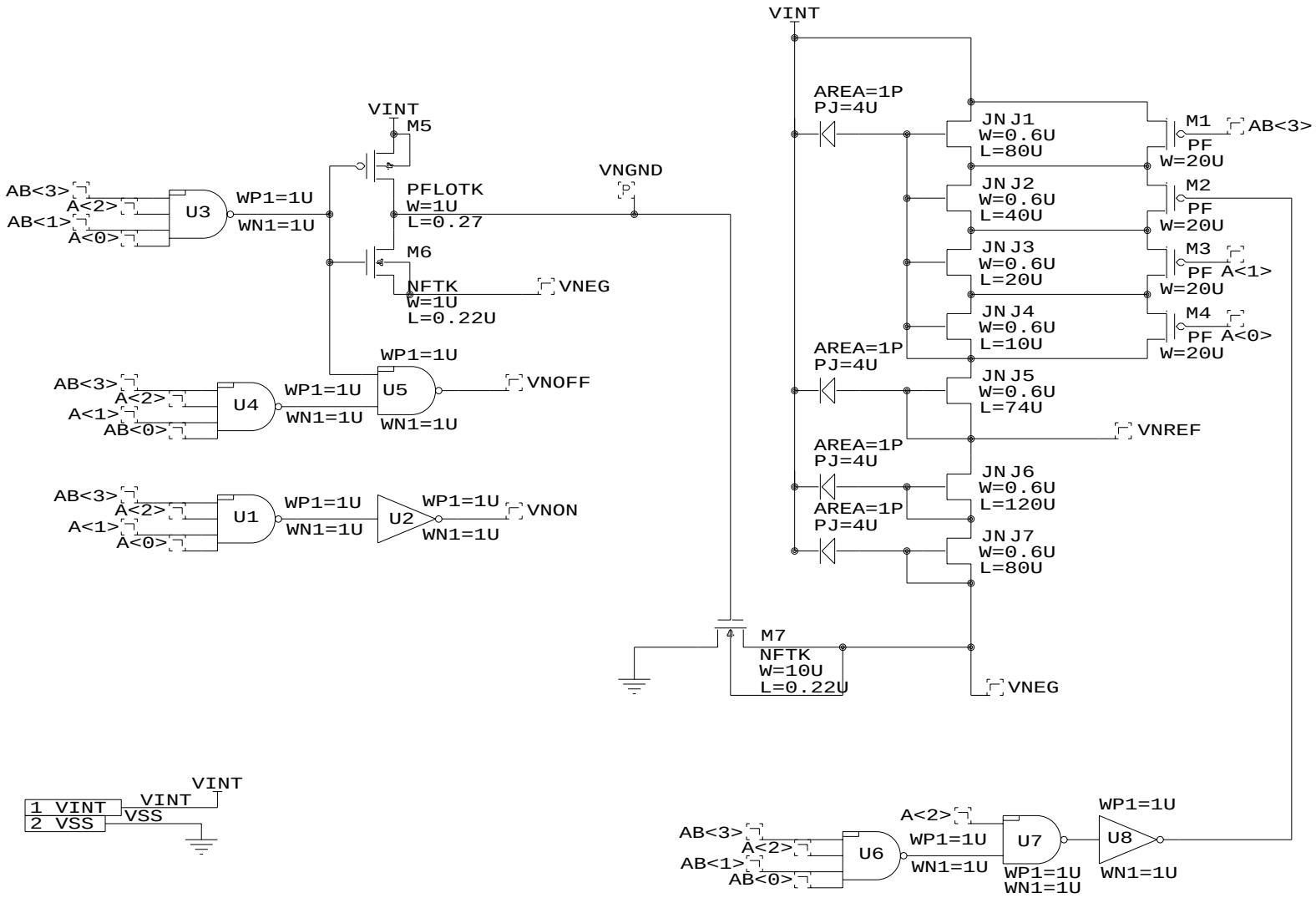
Temperature 105

VCC Voltage 2.0

VNWL Current 2.4mA*

PLACED IN LMISC

UNITED MEMORIES INC. Confidential		
PROJECT: 128D14		
Title VNWL GENERATOR		
Size A	Document Number VNWLGEN	REV A
Date: September 4, 2001	Sheet 1 of 1	

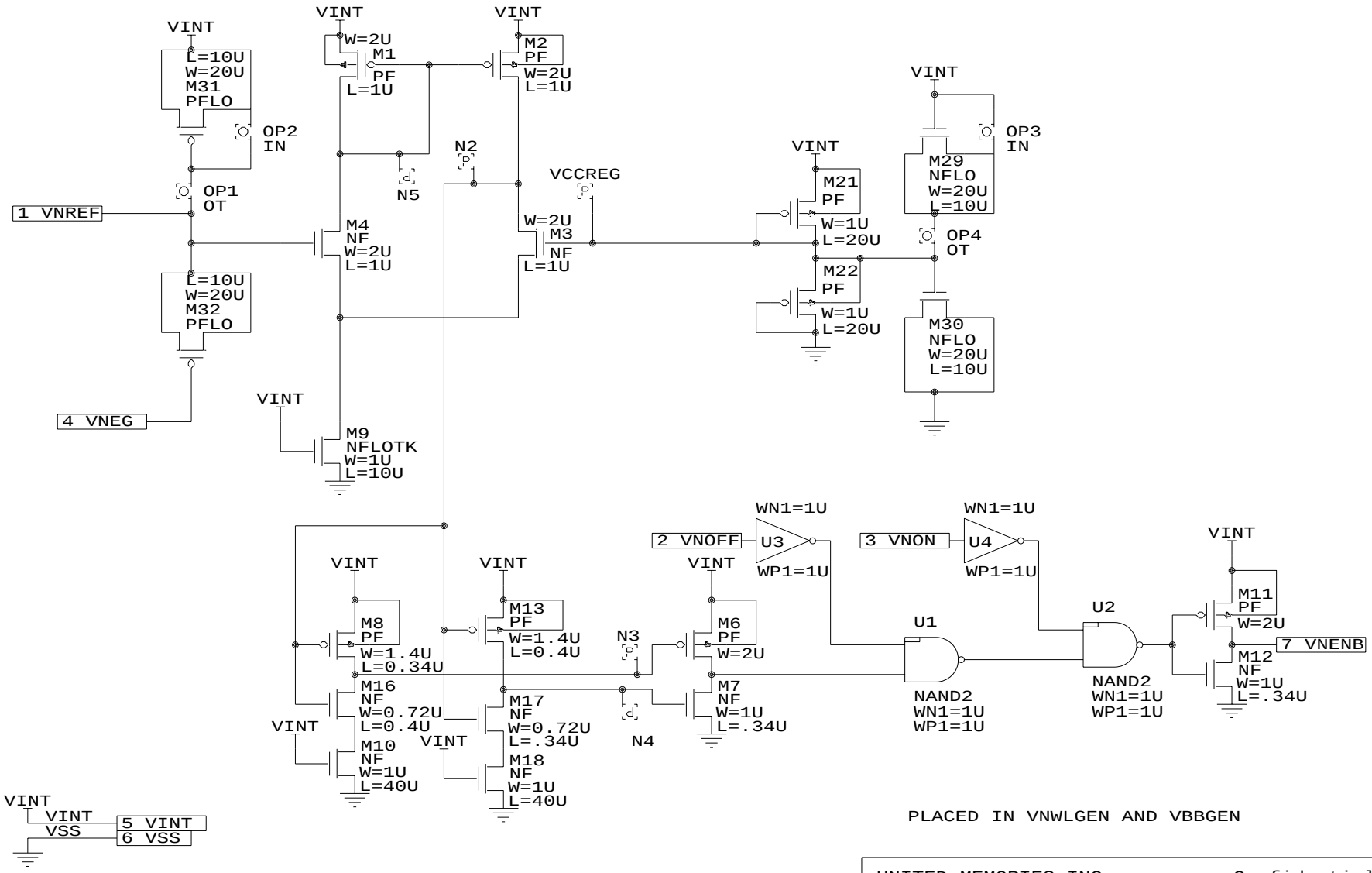


PLACED IN VBBGEN AND VNWLGEN

Istby=1.6uA @ Vint=2.0V, -15C, fnfp models
Istby=1.7uA @ Vint=2.0V, 105C, snsp models

A<3>, AB<2> NOT USED

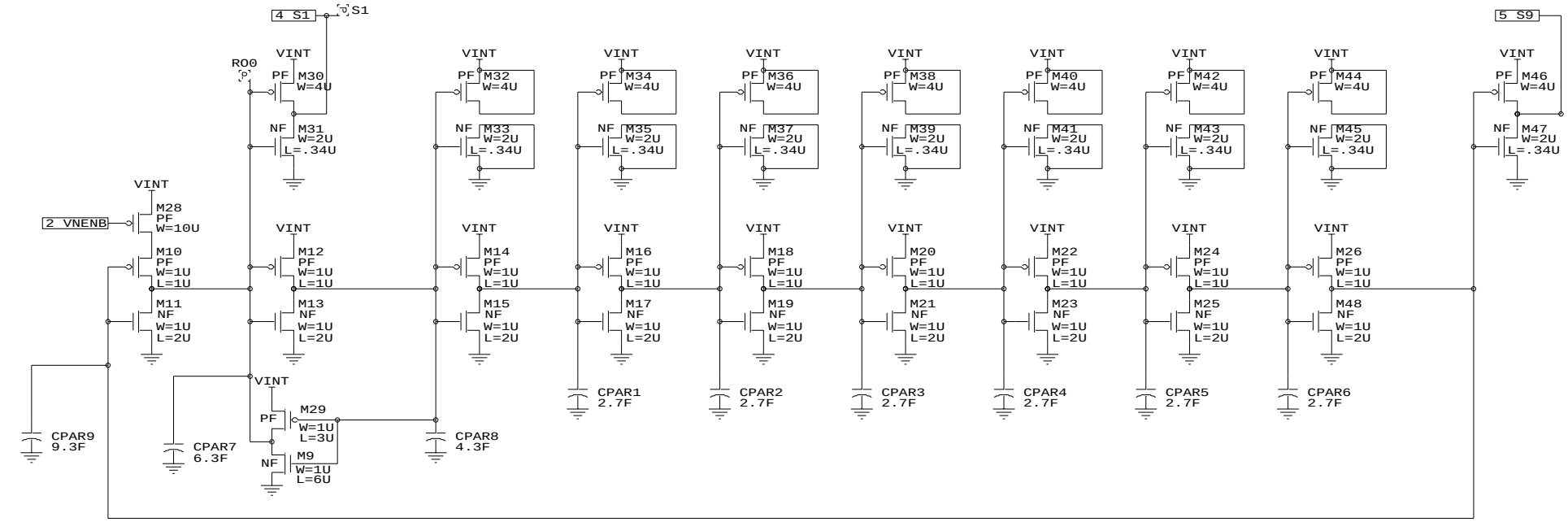
United Memories Inc.		Confidential
Project: 128D14		
Title	Voltage, Negative REFerence	
Size A	Document Number VNREF	REV A
Date: September 4, 2001	Sheet 1 of 1	



PLACED IN VNWLGEN AND VBBGEN

Istby=3.76uA @ Vint=2.0V, 105C, fnfp, vnref=0.99V
Istby=6.70uA @ Vint=2.0V, 105C, fnfp, vnref=1.00V
Istby=3.90uA @ Vint=2.0V, 105C, fnfp, vnref=1.01V
Istby=4.40uA @ Vint=2.0V, -15C, fnfp, vnref=1.01V

UNITED MEMORIES INC.		Confidential
PROJECT: 128D14		
Title		
Regulator for Negative Voltage Generator		
Size A	Document Number VNREG	REV A
Date: September 4, 2001	Sheet 1 of 1	

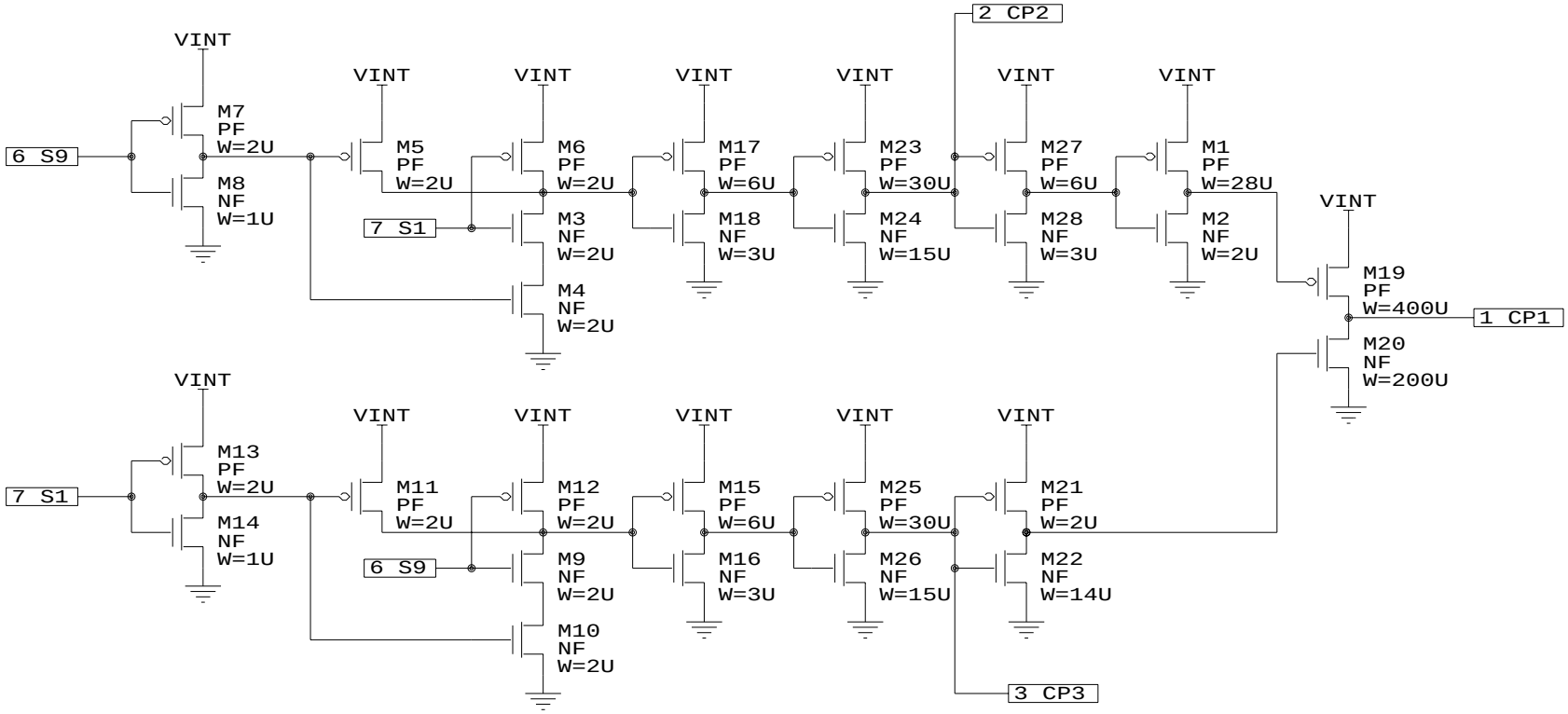


VINT
VINT 1 VINT
VSS 3 VSS

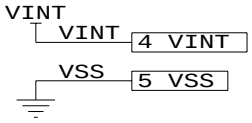
Oscillator Period @ 105C, 2.0 Vcc, Slow Models = ??nS
Oscillator Period @ -15C, 2.4 Vcc, Fast Models = ??nS

PLACED IN VNWLGEN AND VBBGEN

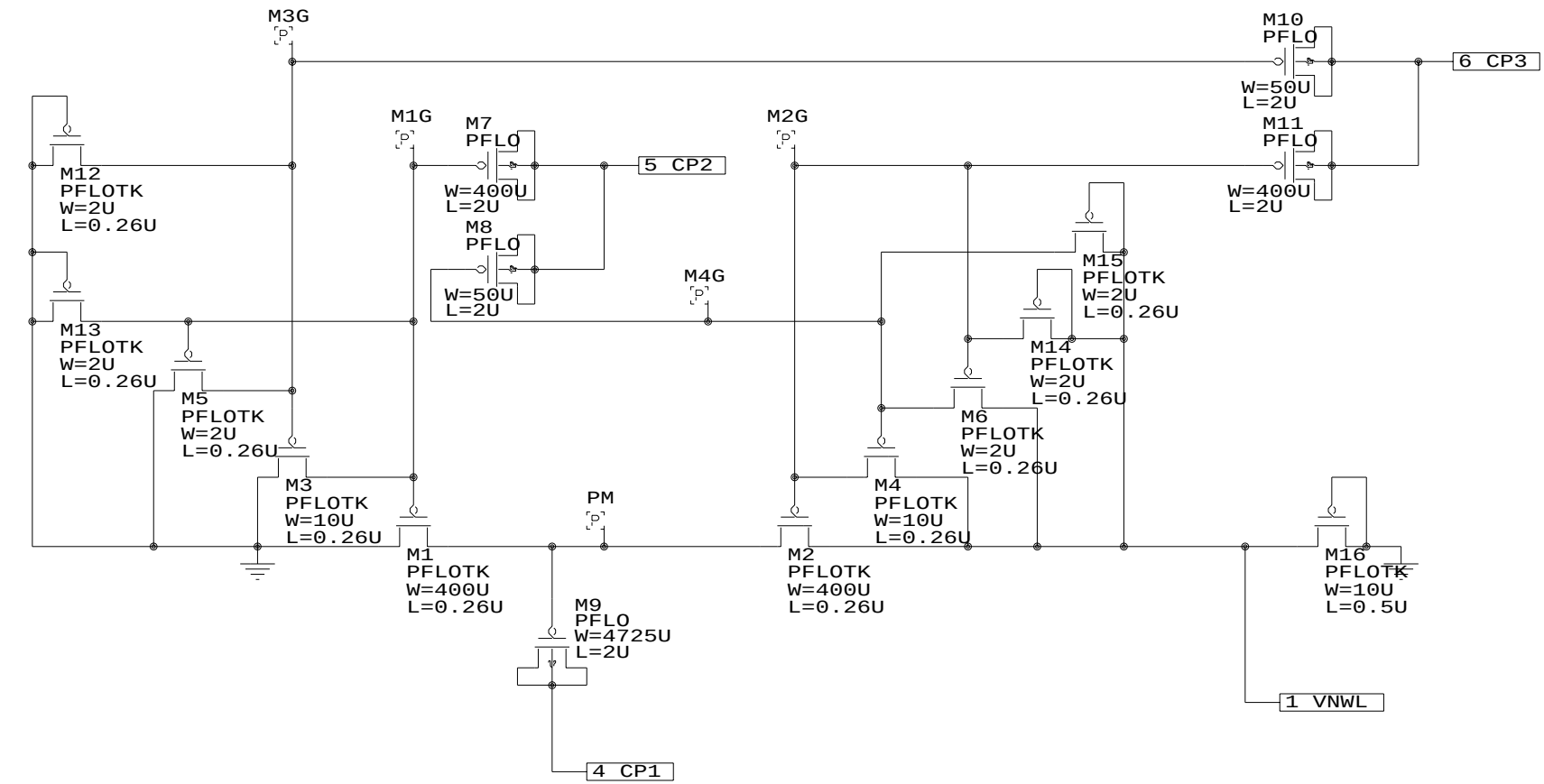
UNITED MEMORIES INC.		Confidential
PROJECT: 128D14		
Title	Negative Voltage Gen Oscillator	
Size B	Document Number VNOSC	REV A
Date: September 4, 2001	Sheet 1 of 1	

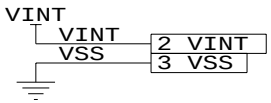


PLACED IN VNWLGEN



UNITED MEMORIES INC. Confidential PROJECT: 128D14		
Title VNWLL Pump Clocks		
Size A	Document Number VNWLCLK	REV A
Date: September 4, 2001	Sheet 1 of 1	

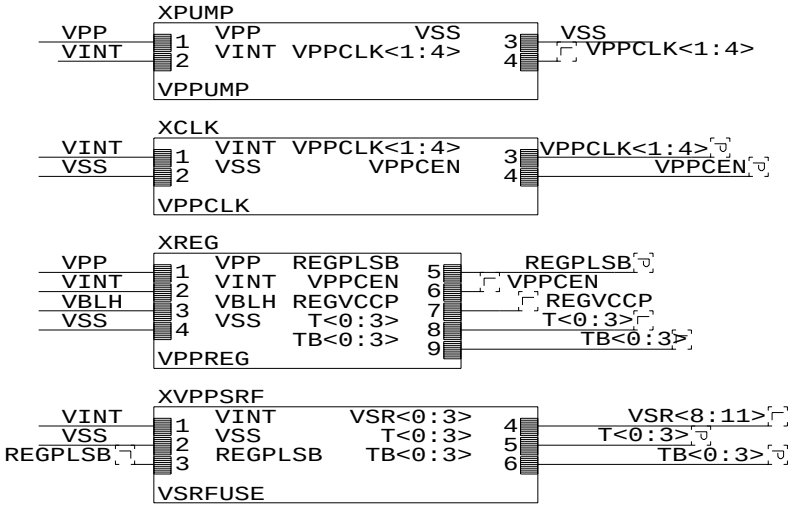




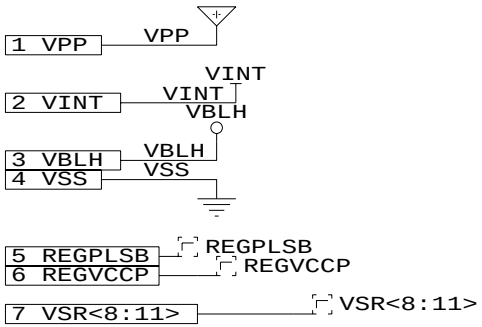
This pump is stopped with CP1 floating.
This pump is stopped with CP2 and CP3 high.

PLACED IN VNWLGEN

UNITED MEMORIES INC.		Confidential
PROJECT: 128D14		
Title	Pump for VNWLL Generator	
Size A	Document Number VNWLPUMP	REV A
Date: October 24, 2001	Sheet 1 of 1	



NOTE: VSRFUSE SCHEMATIC LOCATED IN COUNTER/VSRFUSE SECTION



PLACED IN LMISC - "REGV" ACTIVATED

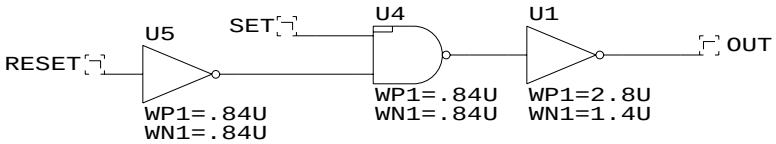
PLACED IN RMISC - "NOBANKB" ACTIVATED

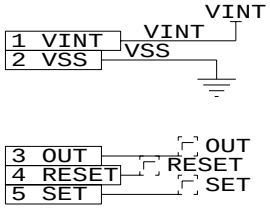
Note: IPP MUST BE MULTIPLIED BY 3 FOR PUMP EFFICIENCY
WHEN CALCULATING TOTAL IPP CURRENT.

Standby Current (Nom Models, T=-15, Vint=2.2): ICC = 9.7e-8
IPP = 1.4e-6
IVBLH = 3.8e-8

SOURCABLE CURRENT (IPP) = 5.03 mA (MIN).

United Memories Inc.		Confidential
Project: 128D14		
Title		
Voltage Positive Pump		
Size A	Document Number VPP	REV A
Date: October 30, 2001	Sheet 1 of 1	





PLACED IN: VPP/VPPCLK

United Memories Inc.		Confidential
Project: 128D14		
Title		
Voltage Positive Pump Clock Decode		
Size	Document Number	REV
A	VPCKDEC	A
Date: September 4, 2001	Sheet 1 of 1	

Edge Delays

NOTE:THE GATES OF ALL OPTION CAPS
MUST HAVE A DIODE CONNECTION TO GROUND

Notes

VPPMCLK causes VPPCLK<1> to go low and VPPCYCLE to go high.

Delay from VPPCLK<1> falling to VPPCLK<2> rising.

Delay from VPPCLK<2> rising to VPPCLK<3> rising.

Delay from VPPCLK<3> rising to VPPCLK<4> rising.

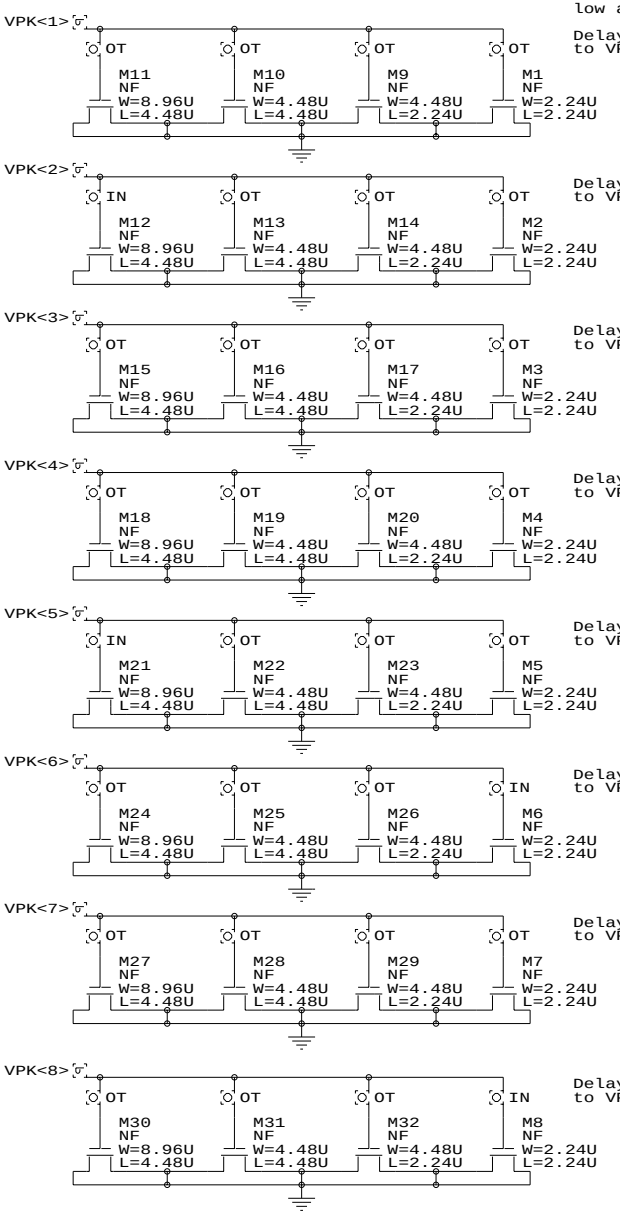
Delay from VPPCLK<4> rising to VPPCLK<3> falling.

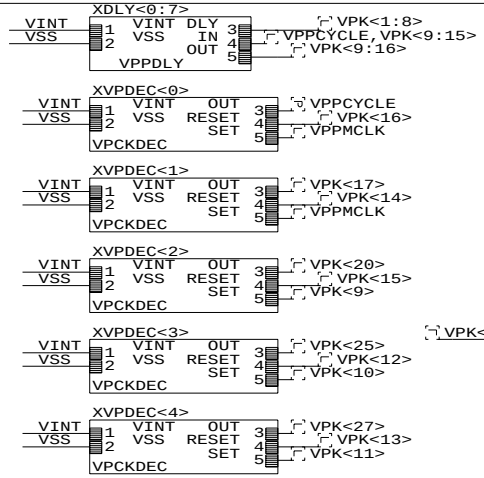
Delay from VPPCLK<3> falling to VPPCLK<4> falling.

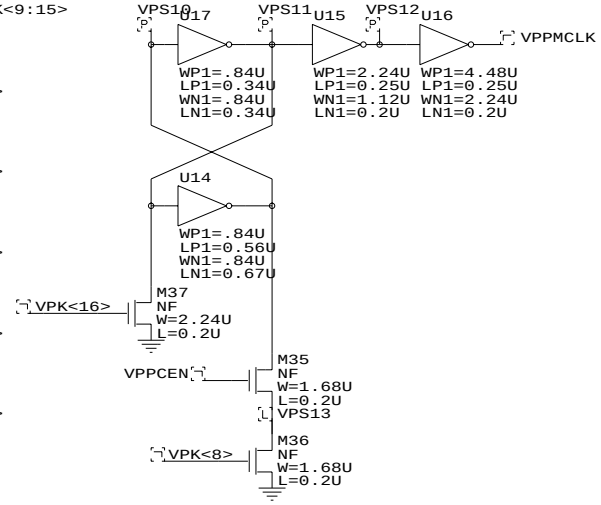
Delay from VPPCLK<4> falling to VPPCLK<1> rising.

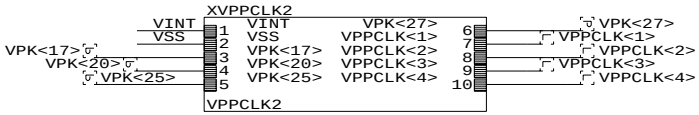
Delay from VPPCLK<1> rising to VPPCLK<2> falling.

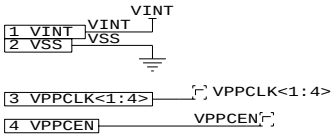
Delay from VPPCLK<2> falling. to VPPCYCLE falling.





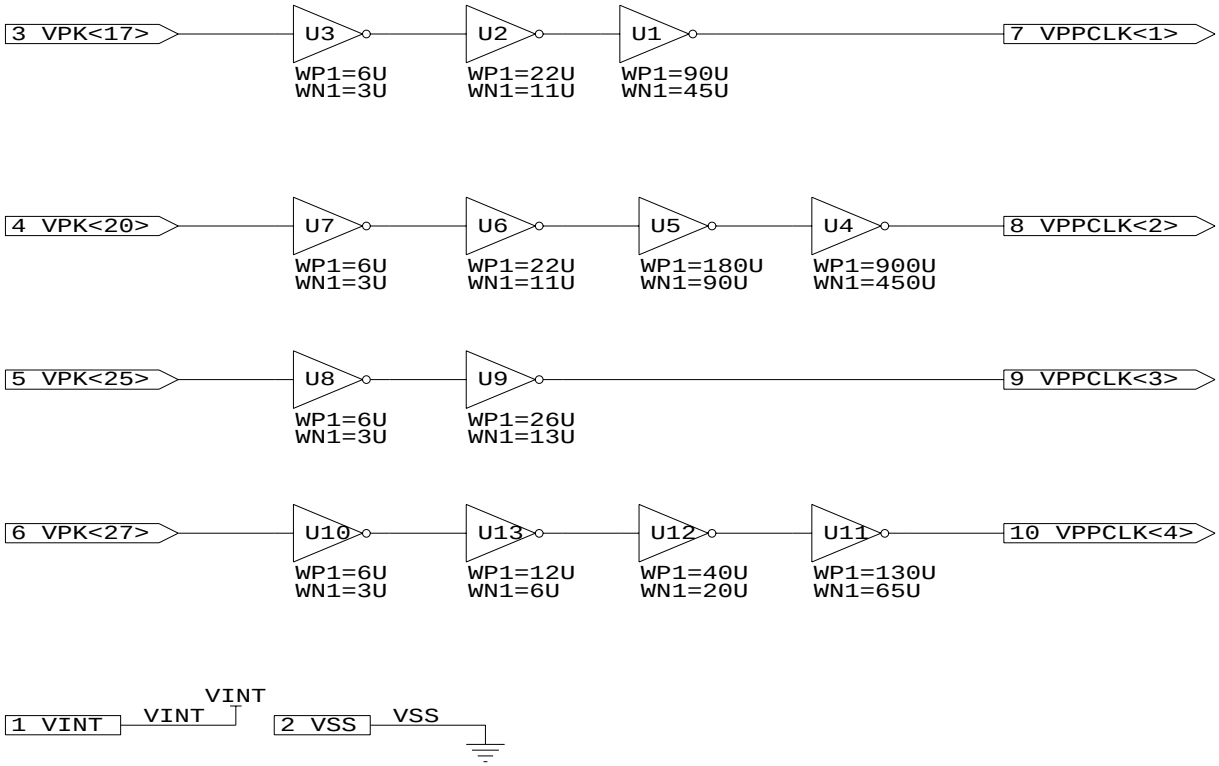






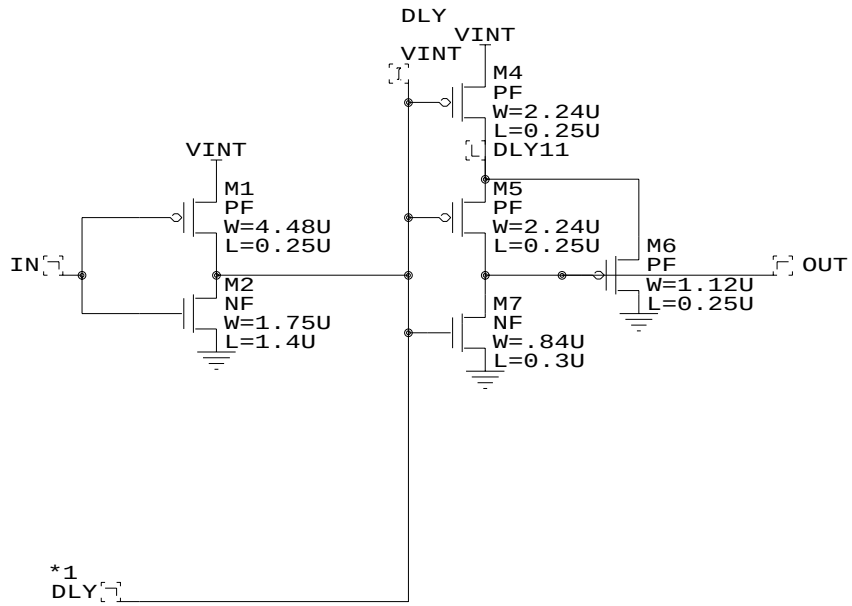
PLACED IN: VPP

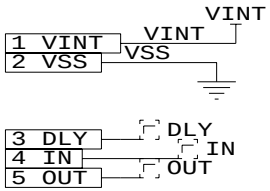
United Memories Inc.		Confidential
Project: 128D14		
Title	Voltage Positive Pump CLocK	
Size B	Document Number VPPCLK	REV A
Date: October 30, 2001	Sheet 1 of 1	



PLACED IN: VPPCLK

United Memories Inc.		Confidential
Project: 128D14		
Title		
Voltage Positive Pump CLocK #2		
Size A	Document Number VPPCLK2	REV A
Date: July 20, 2001	Sheet 1 of 1	

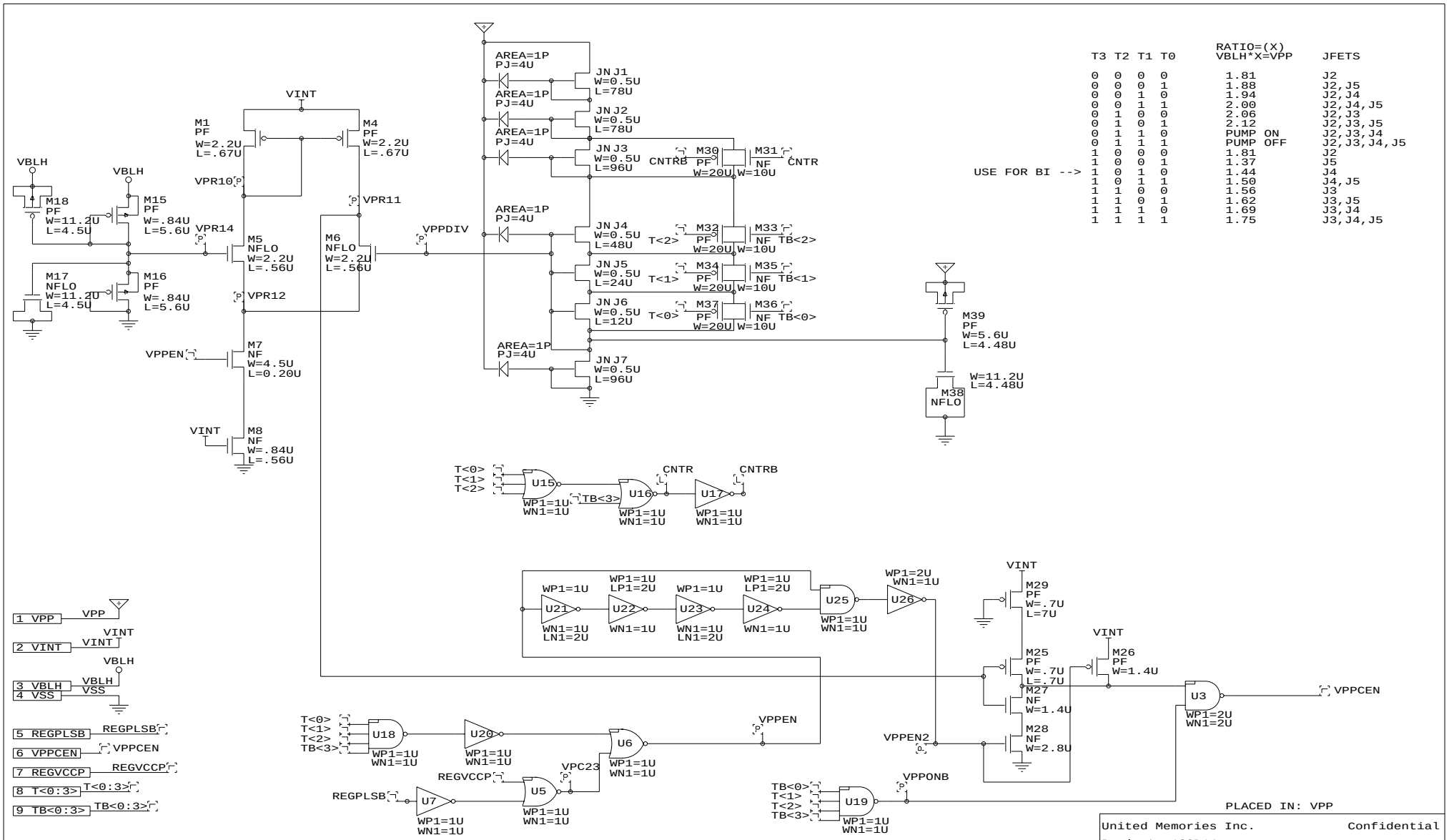




Note 1: Node DLY is connected to load capacitors at the VPPCLK circuit level.

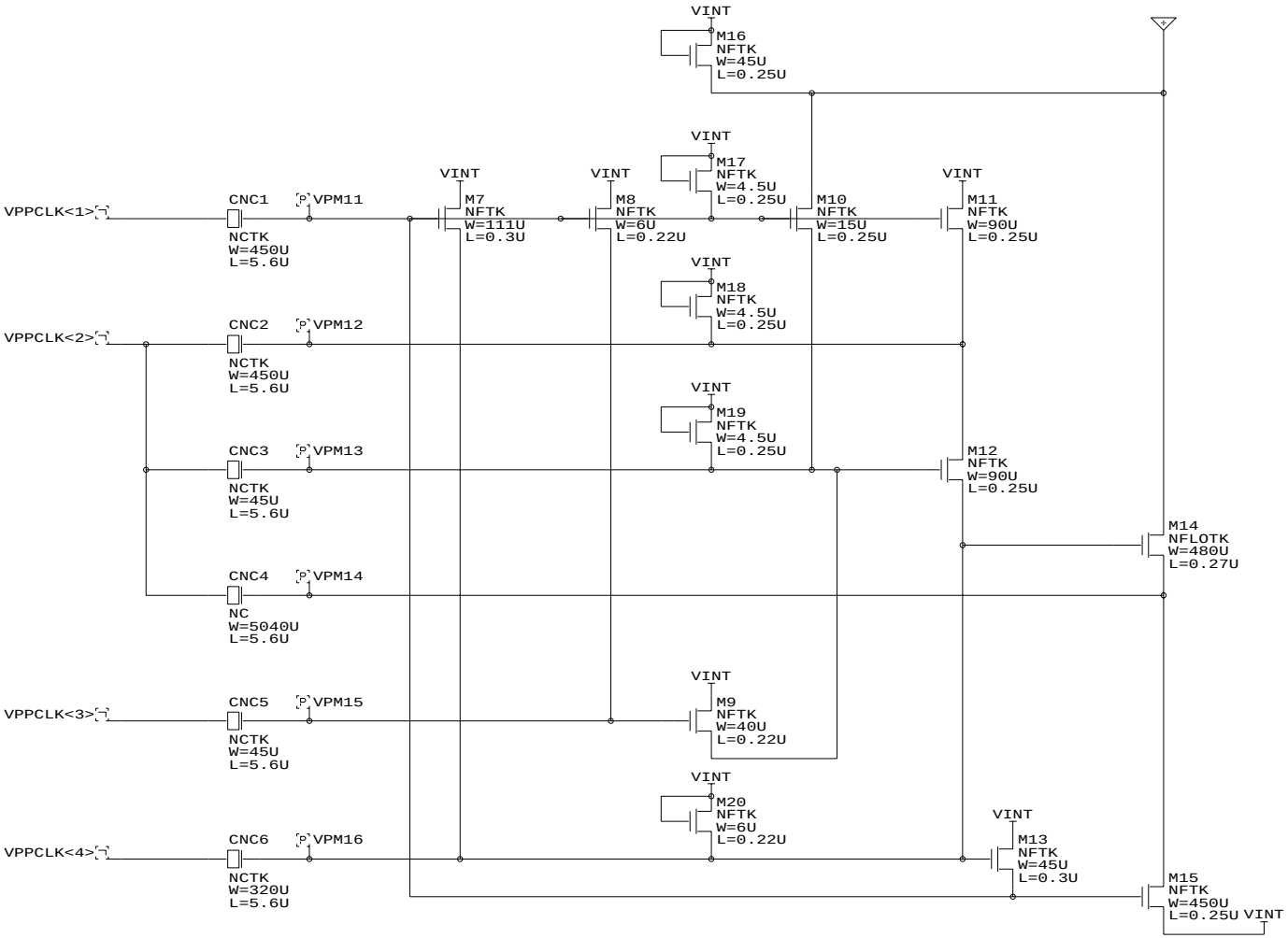
PLACED IN: VPPCLK

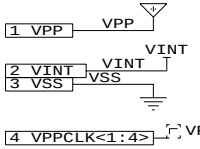
United Memories Inc.		Confidential
Project: 128D14		
Title		
Voltage Positive Pump DeLaY		
Size	Document Number	REV
A	VPPDLY	A
Date: June 25, 2001	Sheet 1 of 1	



USE FOR BI -->

T3	T2	T1	T0	RATIO=(X) VBLH*X=VPP	JFETS
0	0	0	0	1.81	J2
0	0	0	1	1.88	J2,J5
0	0	1	0	1.94	J2,J4
0	0	1	1	2.00	J2,J4,J5
0	1	0	0	2.06	J2,J3
0	1	0	1	2.12	J2,J3,J5
0	1	1	0	PUMP ON	J2,J3,J4
0	1	1	1	PUMP OFF	J2,J3,J4,J5
1	0	0	0	1.81	J2
1	0	0	1	1.37	J5
1	0	1	0	1.44	J4
1	0	1	1	1.50	J4,J5
1	1	0	0	1.56	J3
1	1	0	1	1.62	J3,J5
1	1	1	0	1.69	J3,J4
1	1	1	1	1.75	J3,J4,J5



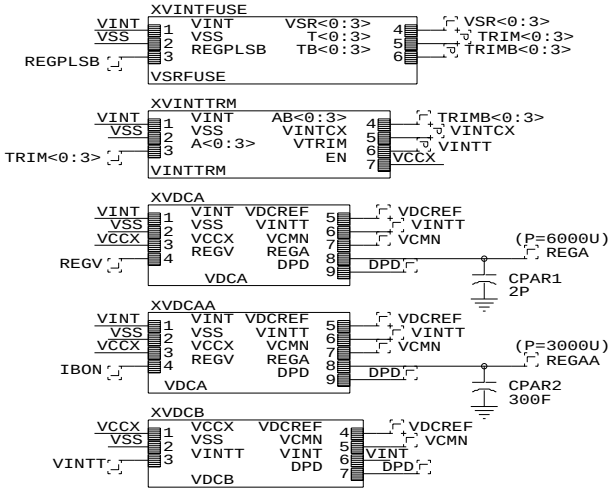


PLACED IN VPP

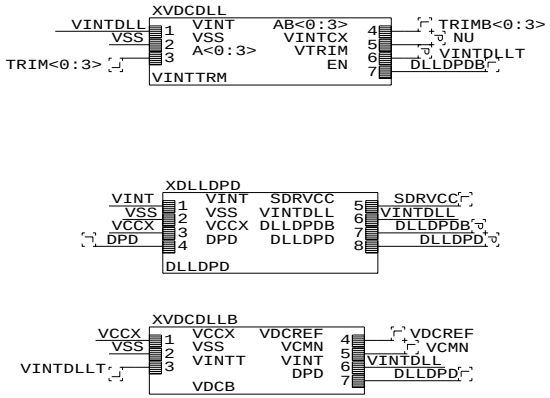
Description: This is the charge pump used for the word lines.
Meta-Level: VPP
Inputs: VPPCLK<1:4> (Voltage Positive Pump CLocK 1 to 4 from ???)
Outputs: VCCP (Voltage Common Collector Pumped to ???)

United Memories Inc.		Confidential
Project: 128D14		
Title	Voltage Positive PUMP	
Size B	Document Number VPPUMP	REV A
Date: October 30, 2001	Sheet 1 of 1	

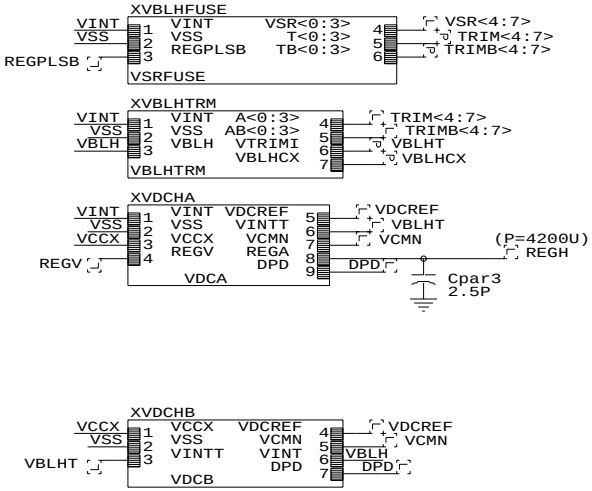
VINT



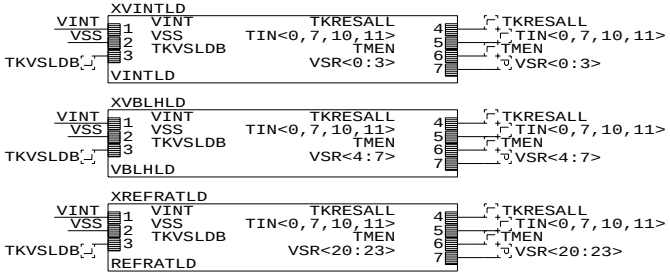
VINTDLL



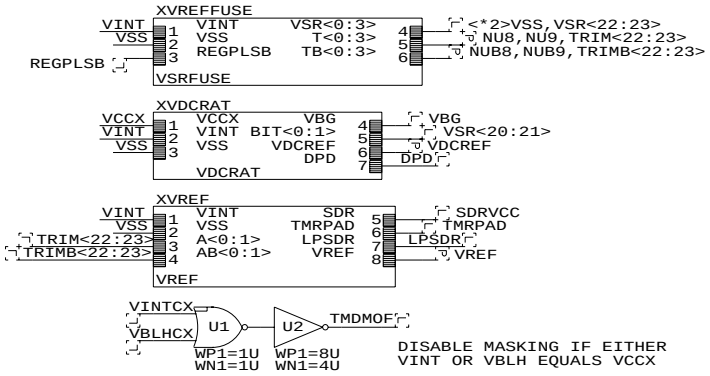
VBLH



VSR LOADING



CONTROL



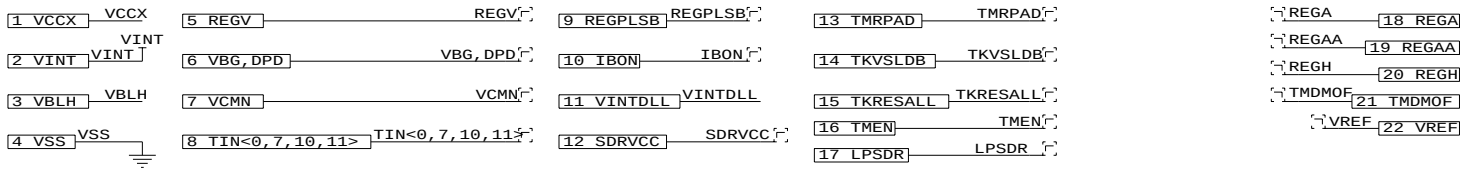
REGAA - Intermediate Strength VINT Generator (P=3000U)
- Use VDCPASS On Left End

REGA - Full Strength VINT Generator (P=6000U)
- Use VDCPASS On Center And Right

REGH - Full Strength VBLH Generator (P=4200U)
- Use VDCPASS On Left, Center, And Right

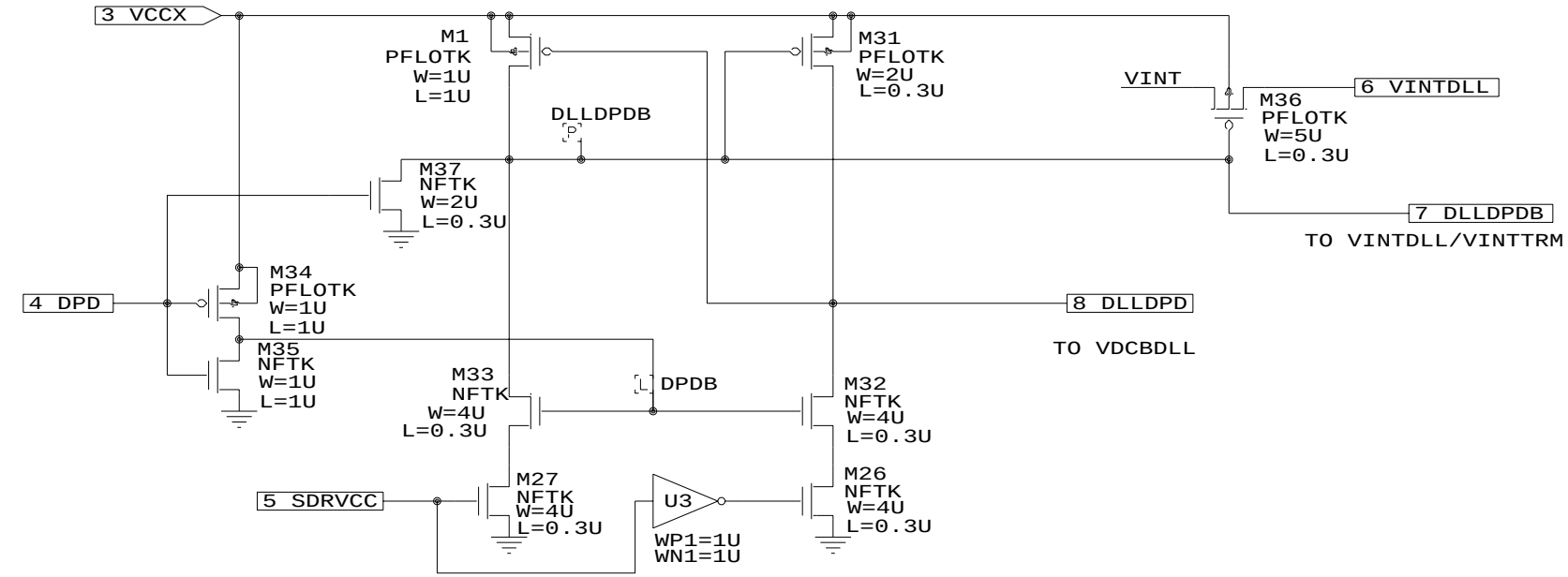
Total Power

- Standby (8.8uA)
- IBON = 1 (657uA)
- IBON = 1 And REGV = 1 (1.95mA)



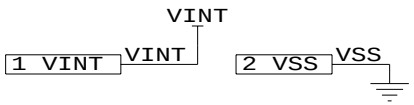
PLACED IN LMISC

UNITED MEMORIES INC.		
PROJECT: 128D14		
Title VBLH/VINT VOLTAGE DOWN CONVERTERS		
Size B	Document Number VDC	REV A
Date: November 21, 2001	Sheet 1 of 1	



FOR ALL SDR PARTS, KILL VDCBDLL AND SHORT VINTDLL=VINT

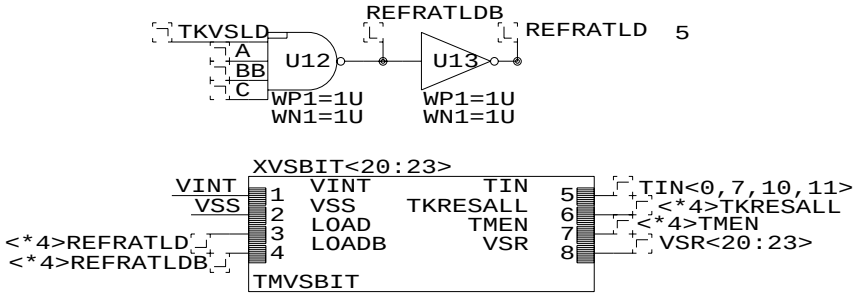
MAINTAIN FOR DPD=1 CONDITION



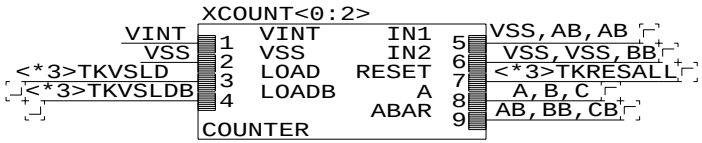
PLACED IN IOBLK

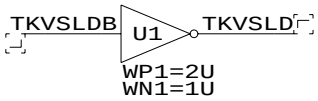
United Memories Inc. PROJECT: 128D14		
Title SPECIAL POWER DOWN FOR VINT-DLL		
Size A	Document Number DLLDPD	REV A
Date: November 1, 2001	Sheet 1 of 1	

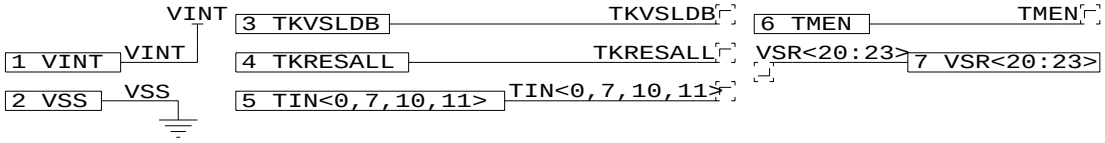
REF/RAT (LOAD 5)



COUNTER



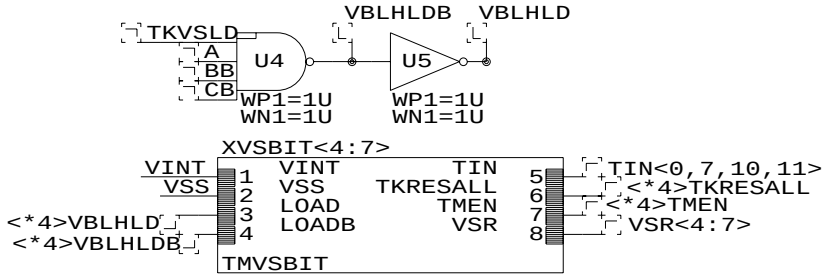




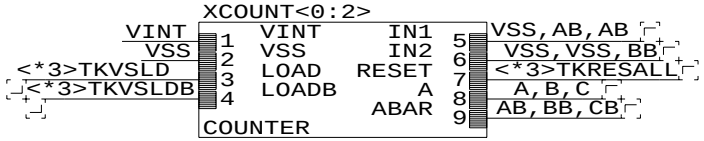
PLACED IN VDC

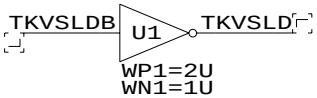
UNITED MEMORIES INC. PROJECT: 128D14		
Title REF/RAT LOAD CONTROL W/ COUNTER		
Size A	Document Number REFRATLD	REV A
Date: September 4, 2001	Sheet 1 of 1	

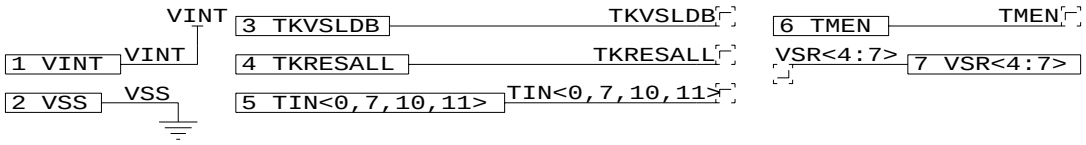
VBLH (LOAD 1)



COUNTER

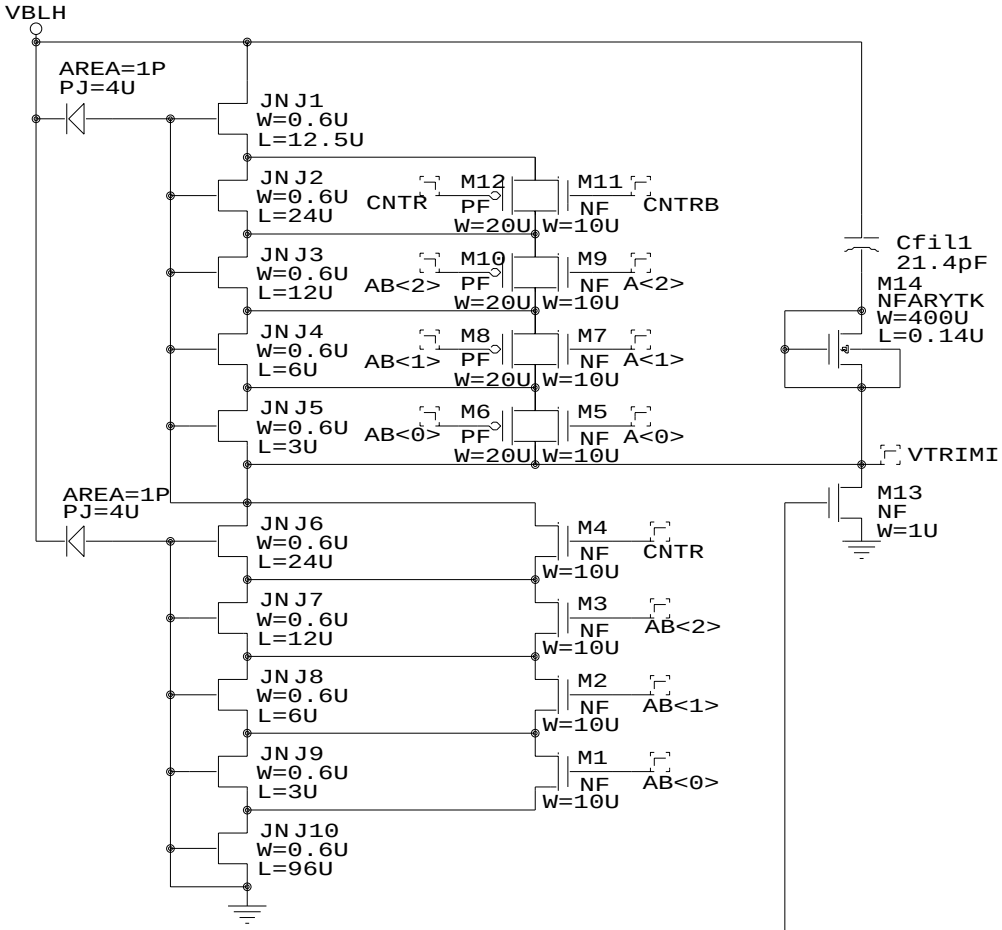


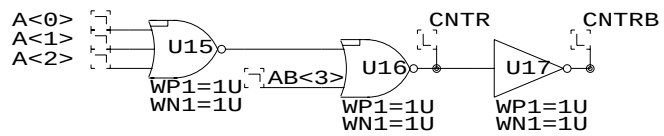


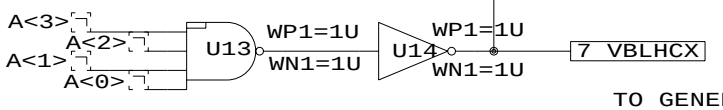


PLACED IN VDC

UNITED MEMORIES INC. PROJECT: 128D14		
Title VBLH LOAD CONTROL W/ COUNTER		
Size A	Document Number VBLHLD	REV A
Date: September 4, 2001	Sheet 1 of 1	



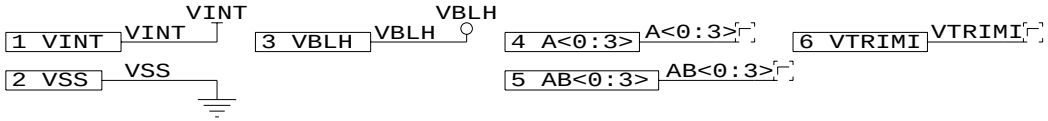




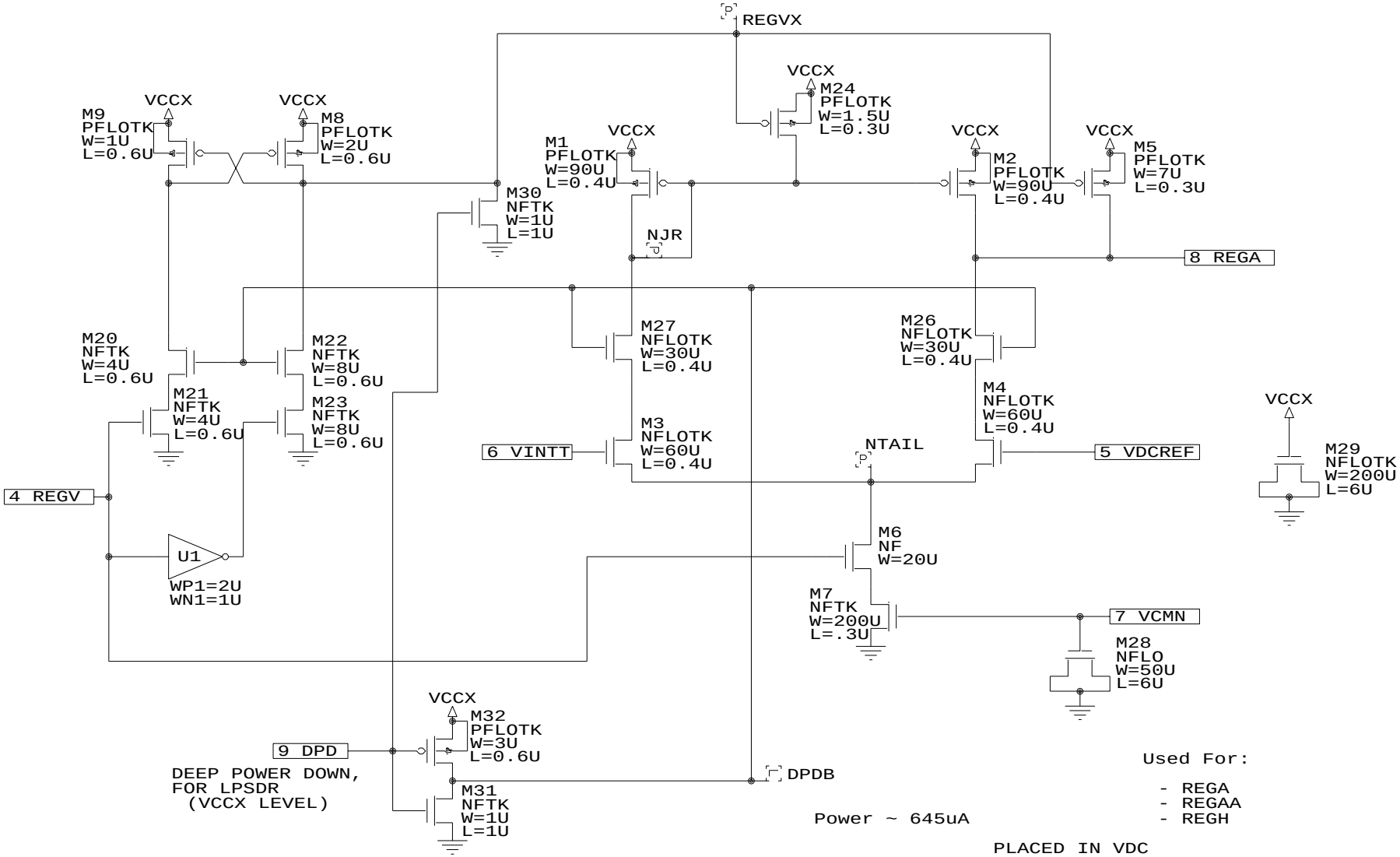
TO GENERATE TMDMOF

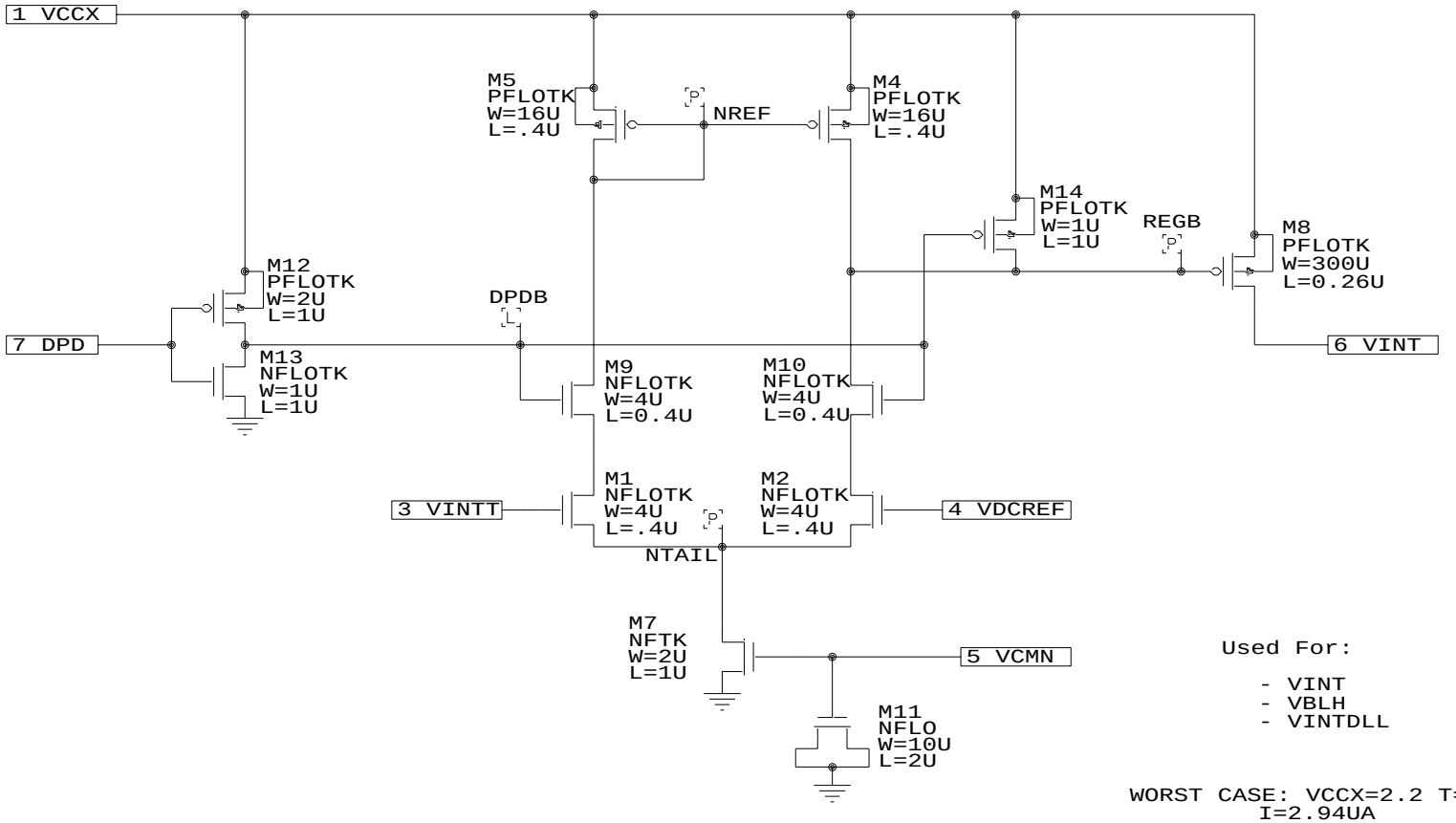
VINT=1.6 T=105 NOM
Ltotal always = 153.5U
R=2.9K/SQ ->
I=1.6/[(153.5/.6)*(2900)]
I=2.16uA

PLACED IN VDC



United Memories Inc.		Confidential
Project: 128D14		
Title	VBLH TRIM	
Size A	Document Number VBLHTRM	REV A
Date: September 4, 2001	Sheet 1 of 1	


REGVX
VCCX
M24
PFLOTK
W=1.5U
L=0.3U
M9
PFLOTK
W=1U
L=0.6U
M8
PFLOTK
W=2U
L=0.6U
M1
PFLOTK
W=90U
L=0.4U
M2
PFLOTK
W=90U
L=0.4U
M5
PFLOTK
W=7U
L=0.3U
M30
NFTK
W=1U
L=1U
NJR
8 REGA
M20
NFTK
W=4U
L=0.6U
M22
NFTK
W=8U
L=0.6U
M21
NFTK
W=4U
L=0.6U
M23
NFTK
W=8U
L=0.6U
M27
NFLOTK
W=30U
L=0.4U
M26
NFLOTK
W=30U
L=0.4U
M4
NFLOTK
W=60U
L=0.4U
M3
NFLOTK
W=60U
L=0.4U
6 VINTT
NTAIL
5 VDCREF
M29
NFLOTK
W=200U
L=6U
4 REGV
U1
WP1=2U
WN1=1U
M6
NF
W=20U
M7
NFTK
W=200U
L=.3U
7 VCMN
M28
NFLO
W=50U
L=6U
M32
PFLOTK
W=3U
L=0.6U
9 DPD
DEEP POWER DOWN,
FOR LPSDR
(VCCX LEVEL)
DPDB
M31
NFTK
W=1U
L=1U
Power ~ 645uA
Used For:
- REGA
- REGAA
- REGH
PLACED IN VDC
VINT
1 VINT
2 VSS
VSS
3 VCCX
UNITED MEMORIES INC.
PROJECT: 128D14
Title
ACTIVE VINT/VBLH REG
Size
A
Document Number
VDCA
REV
A
Date: October 29, 2001
Sheet 1 of 1



Used For:

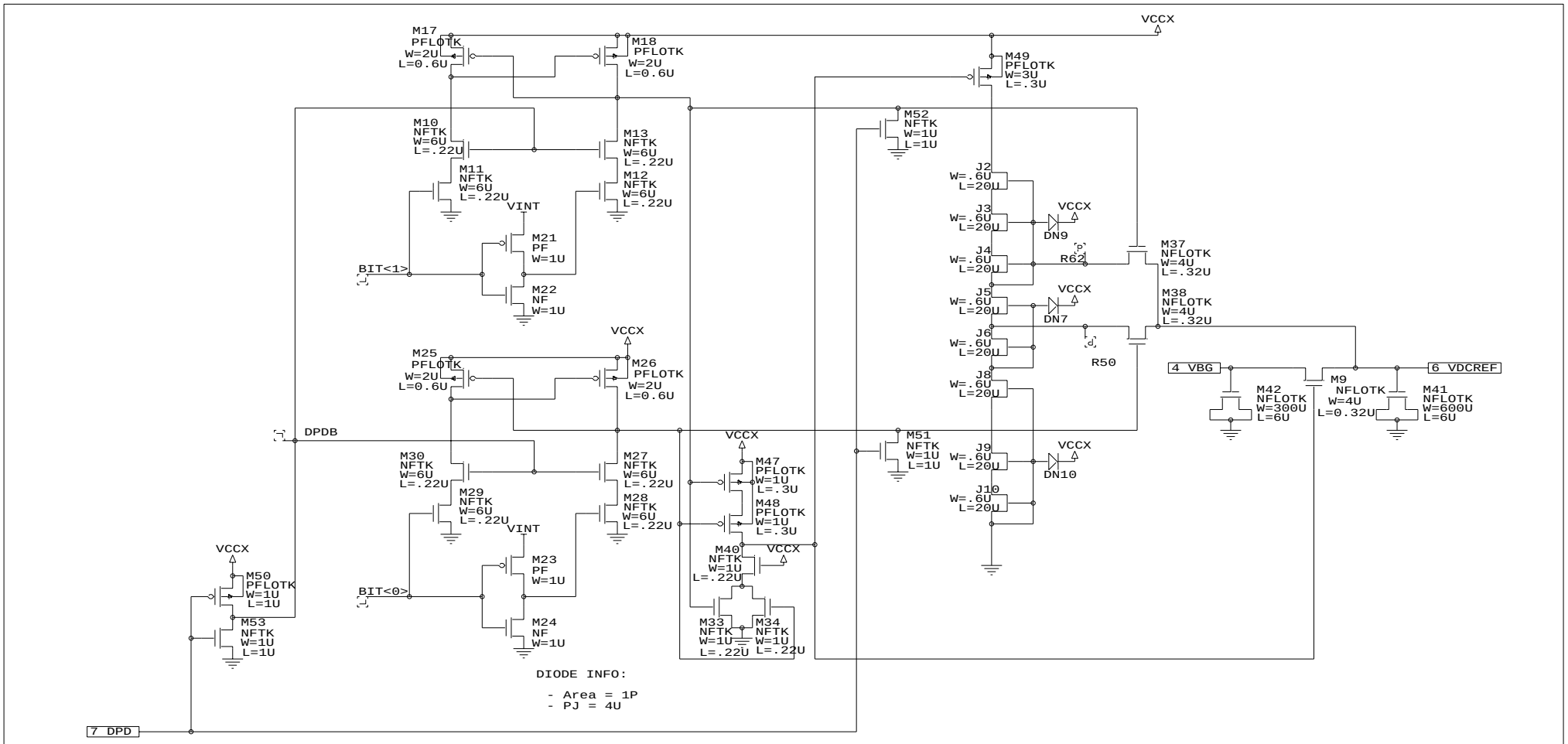
- VINT
- VBLH
- VINTDLL

WORST CASE: VCCX=2.2 T=105
I=2.94UA

PLACED IN VDC

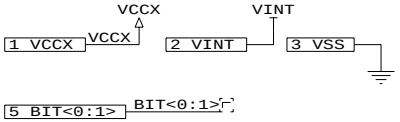
2 VSS

UNITED MEMORIES INC. PROJECT: 128DDR		
Title STANDBY VINT/VBLH REG		
Size A	Document Number VDCB	REV A
Date: October 29, 2001	Sheet 1 of 1	



VBLH=1.29*VDCREF
VINT=1.61*VDCREF

PLACED IN VDC



BIT 1	BIT 0		CURRENT (VCCX=3.0)
0	0	VDCREF=VBG	90nA
0	1	VDCREF=.5*VCCX	3.85UA
1	0	VDCREF=.62*VCCX (BURN-IN)	3.85UA
1	1	VDCREF=.57*VCCX	4.36UA

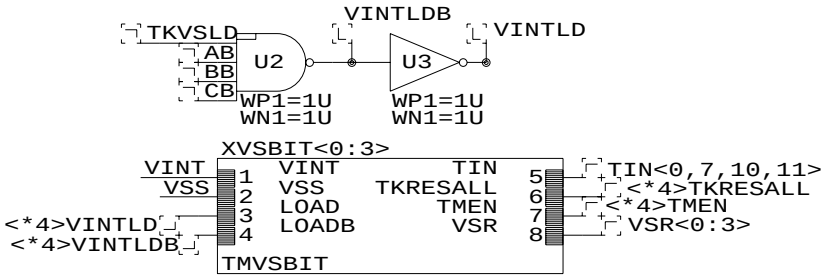
UNITED MEMORIES INC.
PROJECT: 128DDR

Title: VDC RATIO CIRCUIT

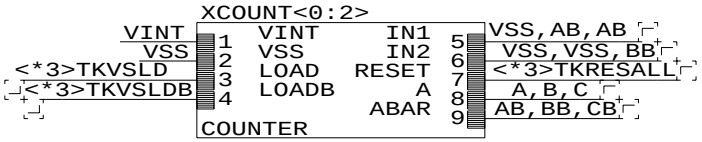
Size	Document Number	REV
B	VDCRAT	A

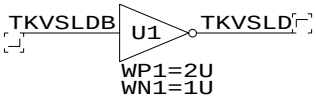
Date: October 29, 2001 | Sheet 1 of 1

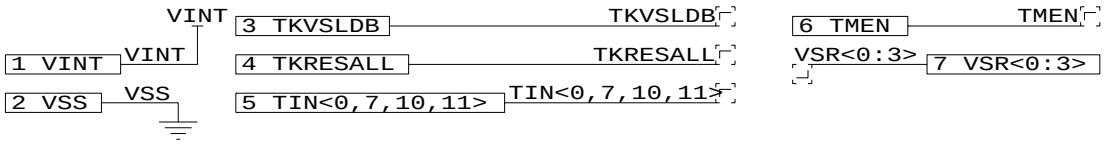
VINT (LOAD 0)



COUNTER

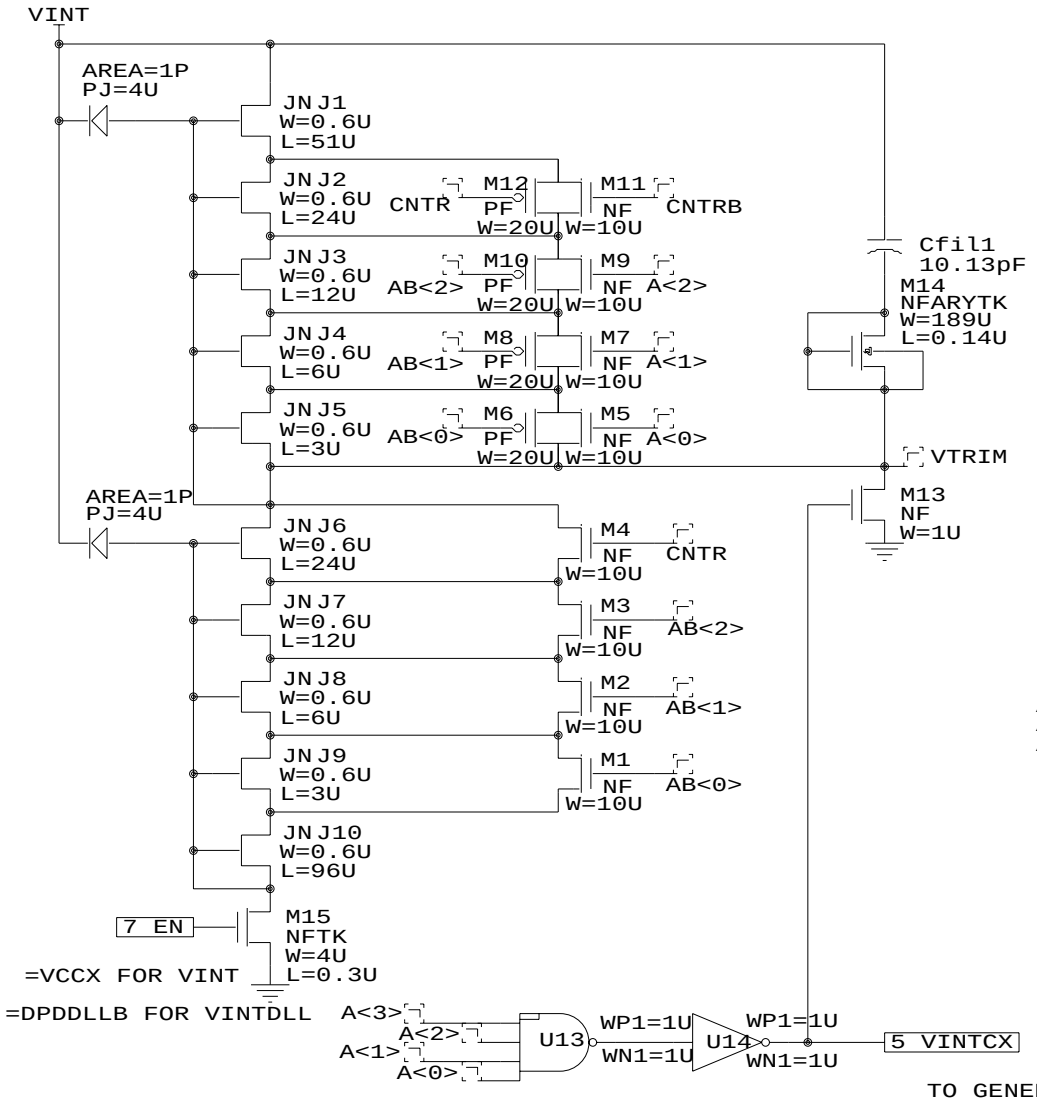




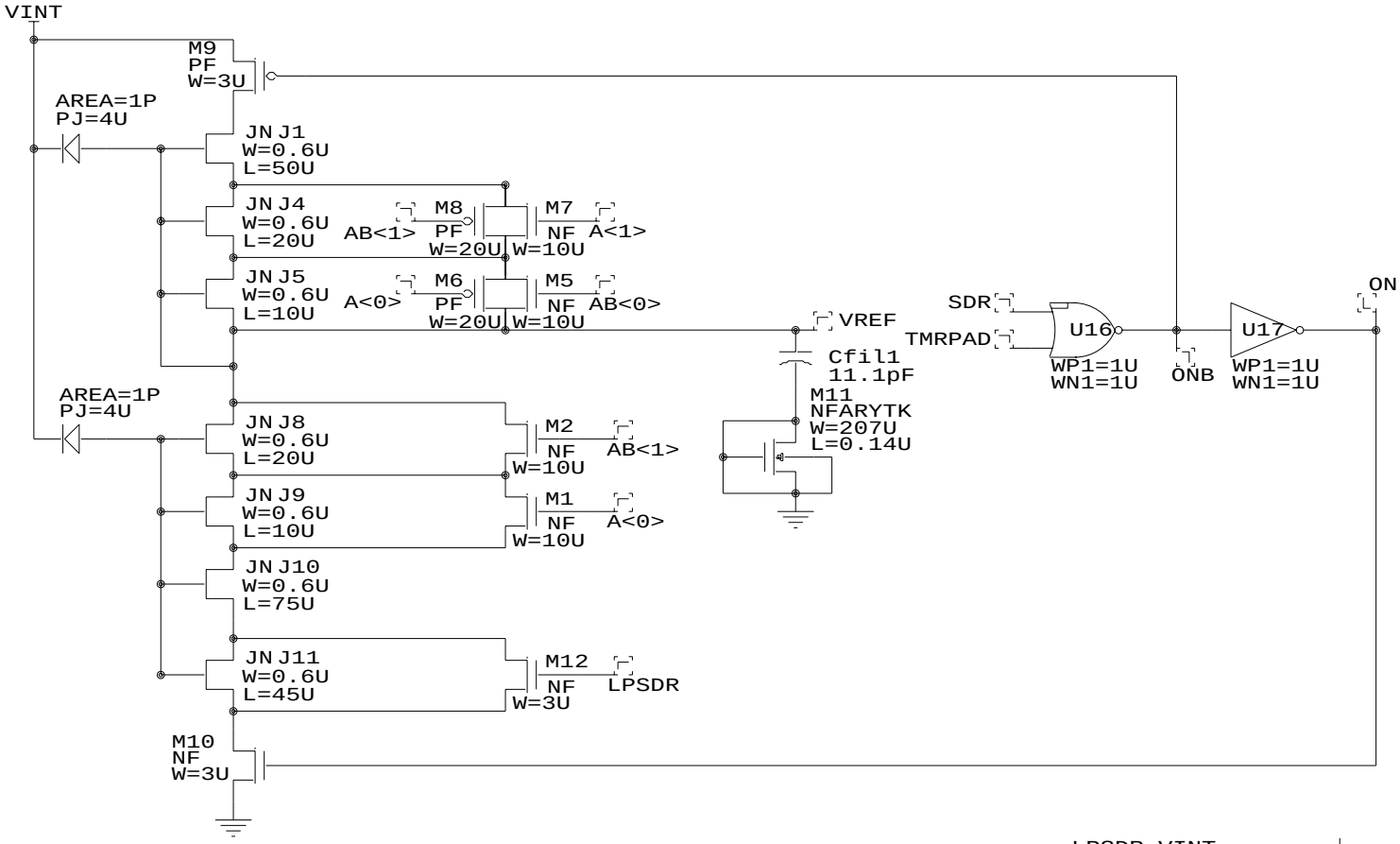


PLACED IN VDC

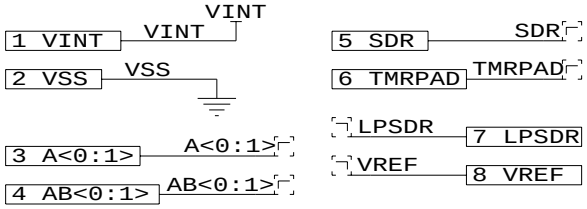
UNITED MEMORIES INC. PROJECT: 128D14		
Title VINT LOAD CONTROL W/ COUNTER		
Size A	Document Number VINTLD	REV A
Date: September 4, 2001	Sheet 1 of 1	



United Memories Inc.		Confidential
Project: 128D14		
Title	VINT TRIM	
Size A	Document Number VINTTRM	REV A
Date: November 1, 2001	Sheet 1 of 1	



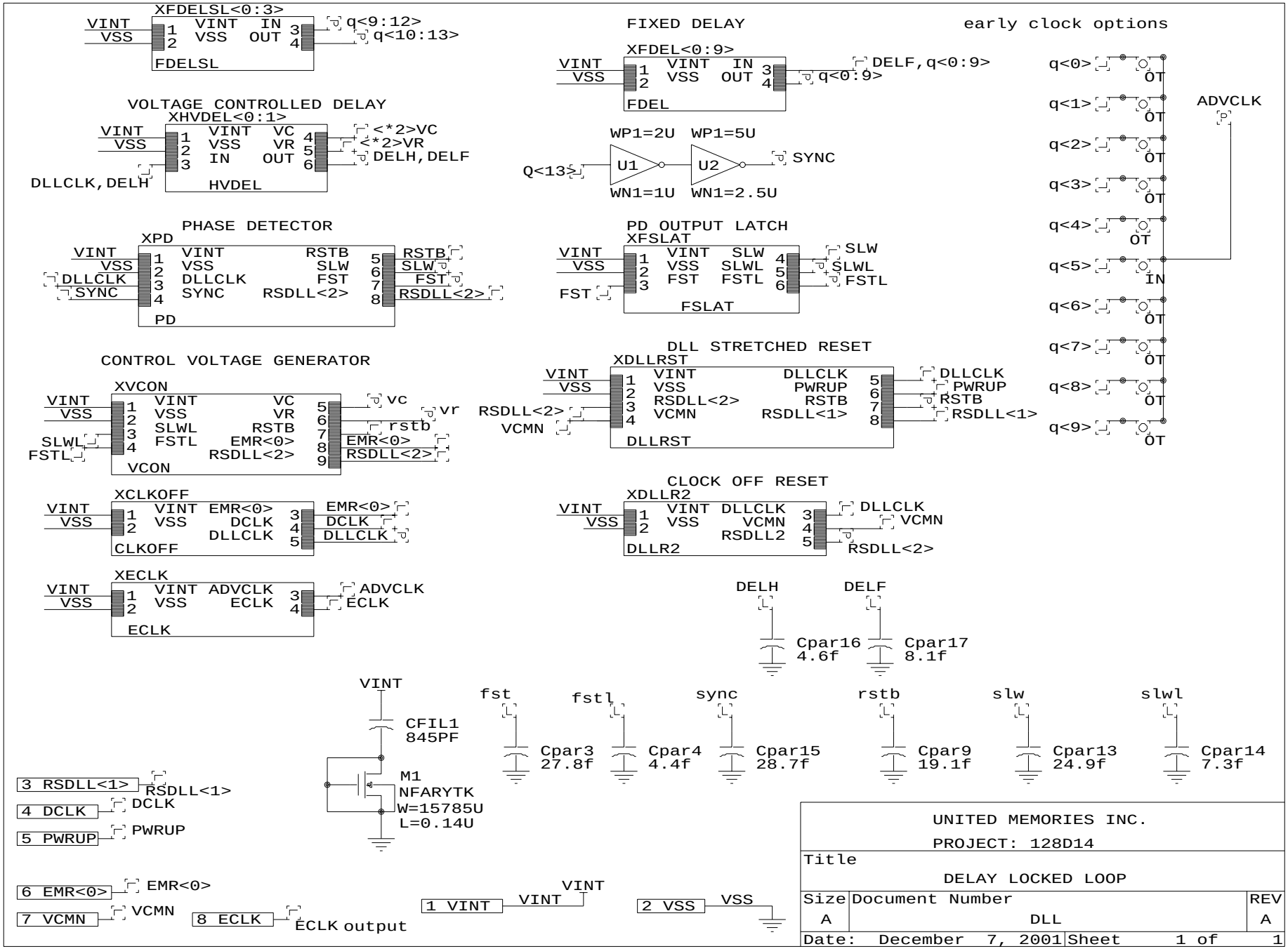
LPSDR=VINT			LPSDR=VSS		
A<1>	A<0>	VREF	A<1>	A<0>	VREF
0	0	.55*VINT	0	0	.65*VINT
0	1	.485*VINT	0	1	.60*VINT
1	0	.675*VINT	1	0	.75*VINT
1	1	.61*VINT	1	1	.70*VINT

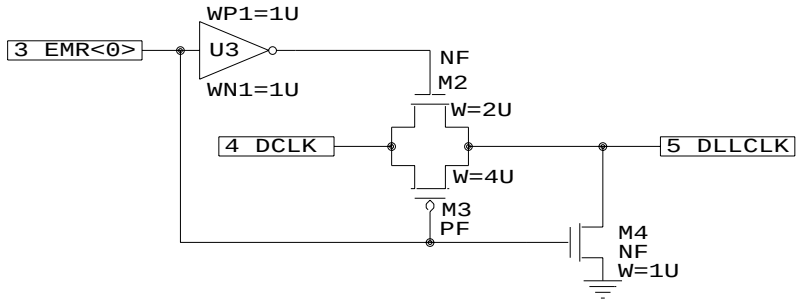


PLACED IN VDC

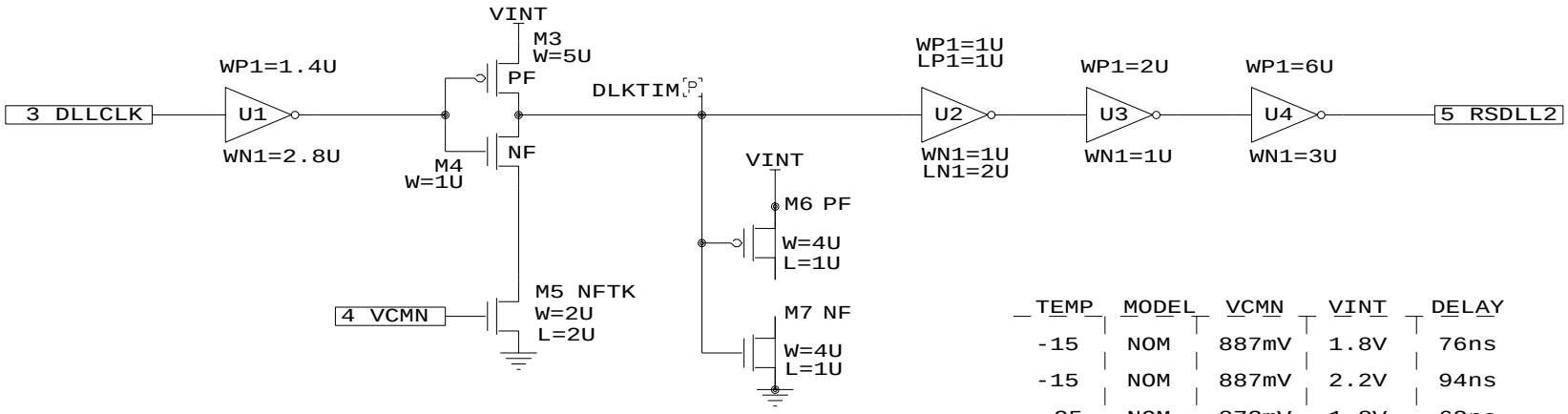
R=2.9K/SQ
I~2.07uA

United Memories Inc.		Confidential
Project: 128D14		
Title	VREF GENERATOR	
Size A	Document Number VREF	REV A
Date: December 3, 2001	Sheet 1 of 1	

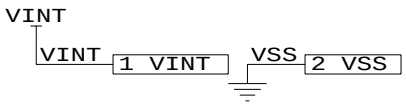

XFDELSL<0:3>
VINT
VSS
VINT IN
VSS OUT
q<9:12>
q<10:13>
FDELSL
FIXED DELAY
XFDEL<0:9>
DELF,q<0:9>
q<0:9>
FDEL
early clock options
q<0>
q<1>
q<2>
q<3>
q<4>
q<5>
q<6>
q<7>
q<8>
q<9>
OT
IN
ADVCLK
VOLTAGE CONTROLLED DELAY
XHVDEL<0:1>
VC
VR
<*2>VC
<*2>VR
DELH,DELF
DLLCLK,DELH
HVDEL
WP1=2U
WP1=5U
Q<13>
U1
U2
SYNC
WN1=1U
WN1=2.5U
PHASE DETECTOR
XPD
RSTB
SLW
FST
RSDLL<2>
DLLCLK
SYNC
PD
PD OUTPUT LATCH
XFSLAT
SLWL
FSTL
FSLAT
CONTROL VOLTAGE GENERATOR
XVCON
vc
vr
rstb
EMR<0>
SLWL
FSTL
VCON
DLL STRETCHED RESET
XDLLRST
DLLCLK
PWRUP
RSDLL<1>
VCMN
DLLRST
XCLKOFF
CLKOFF
CLOCK OFF RESET
XDLLR2
RSDLL2
DLLR2
XECLK
ADVCLK
ECLK
DELH
DELF
Cpar16
4.6f
Cpar17
8.1f
fst
fstl
sync
rstb
slw
slwl
Cpar3
27.8f
Cpar4
4.4f
Cpar15
28.7f
Cpar9
19.1f
Cpar13
24.9f
Cpar14
7.3f
CFIL1
845PF
M1
NFARYTK
W=15785U
L=0.14U
3 RSDLL<1>
4 DCLK
5 PWRUP
6 EMR<0>
7 VCMN
8 ECLK
ECLK output
1 VINT
2 VSS
UNITED MEMORIES INC.
PROJECT: 128D14
Title
DELAY LOCKED LOOP
Size
A
Document Number
DLL
REV
A
Date: December 7, 2001
Sheet 1 of 1



UNITED MEMORIES INC. PROJECT: 128D14		
Title DLLCLK OFF		
Size A	Document Number CLKOFF	REV A
Date: December 3, 2001	Sheet 1 of 1	



TEMP	MODEL	VCMN	VINT	DELAY
-15	NOM	887mV	1.8V	76ns
-15	NOM	887mV	2.2V	94ns
25	NOM	872mV	1.8V	63ns
25	NOM	872mV	2.2V	77ns
105	NOM	841mV	1.8V	51ns
105	NOM	841mV	2.2V	62ns
-15	SNFP	942mV	1.8V	69ns
-15	SNFP	942mV	2.2V	85ns
105	SNFP	900mV	1.8V	45ns
105	SNFP	900mV	2.2V	55ns
-15	FNFP	847mV	1.8V	77ns
-15	FNFP	847mV	2.2V	95ns
105	FNFP	777mV	1.8V	64ns
105	FNFP	777mV	2.2V	79ns



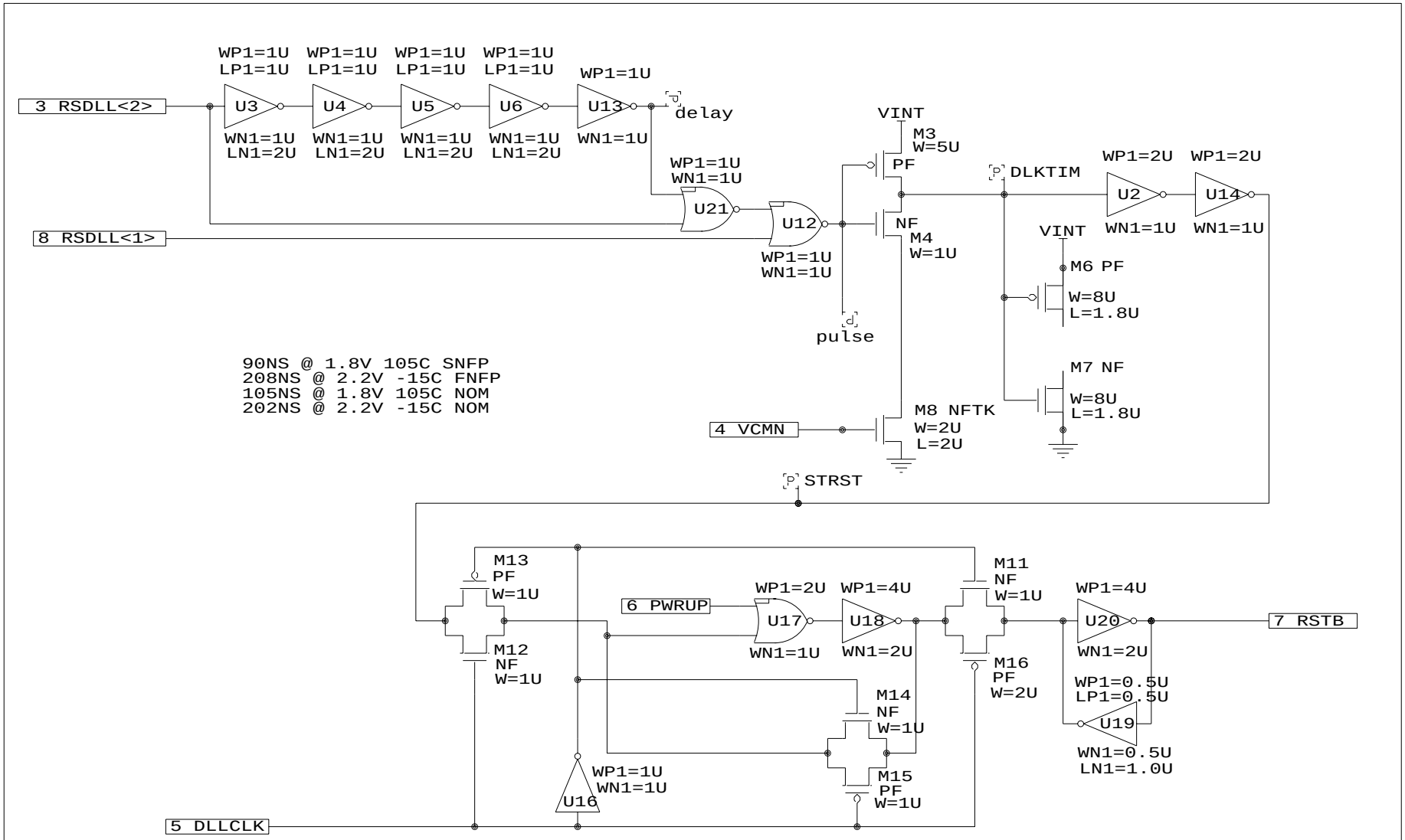
UNITED MEMORIES INC.

PROJECT: 128D14

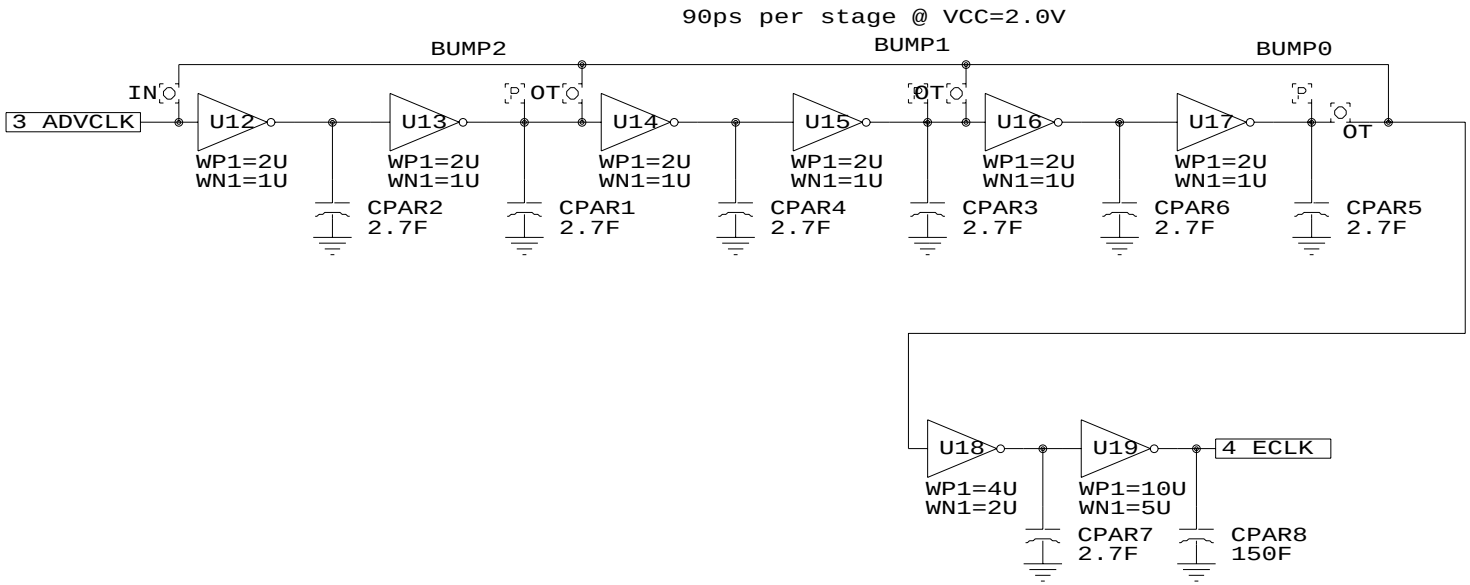
Title: DLL RESET2

Size	Document Number	REV
A	DLLR2	A

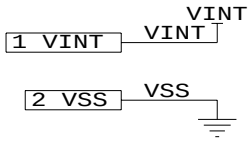
Date: November 29, 2001 Sheet 1 of 1



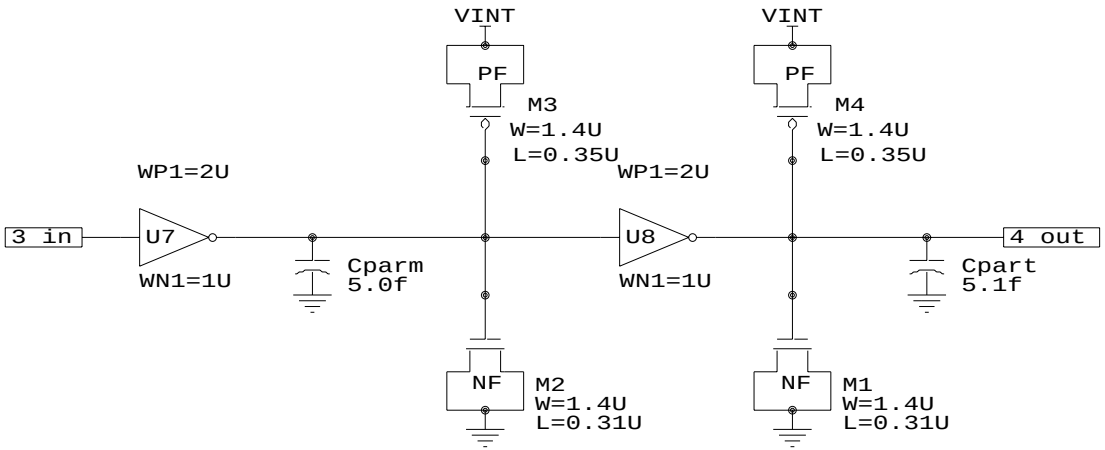
UNITED MEMORIES INC.		
PROJECT: 128D14		
Title		
DLL RESET		
Size A	Document Number DLLRST	REV A
Date: December 3, 2001	Sheet 1 of 1	



PLACED IN LMISC
PLACED IN DLL

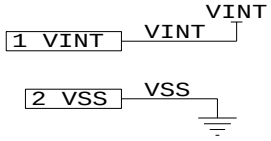


United Memories, Inc. Project: 128D14		
Title EARLY CLOCK		
Size A	Document Number ECLK	REV A
Date: November 21, 2001	Sheet 1 of 1	

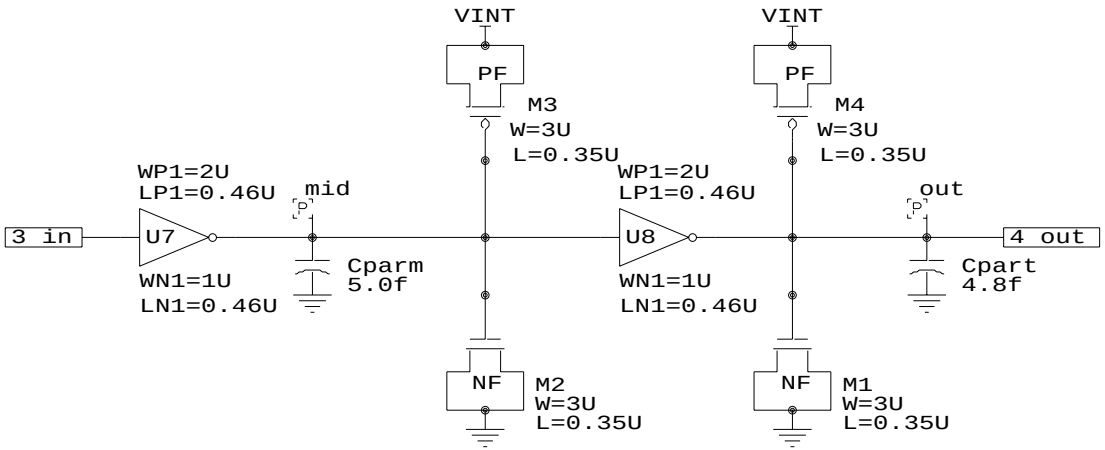


175 ps per stage @ VINT=2.0V 45C

PLACED IN DLL

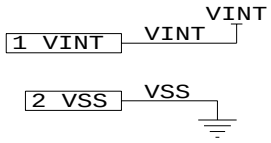


United Memories, Inc. Project: 128D14		
Title Fixed Delay Line		
Size A	Document Number FDEL	REV A
Date: December 6, 2001	Sheet 1 of 1	

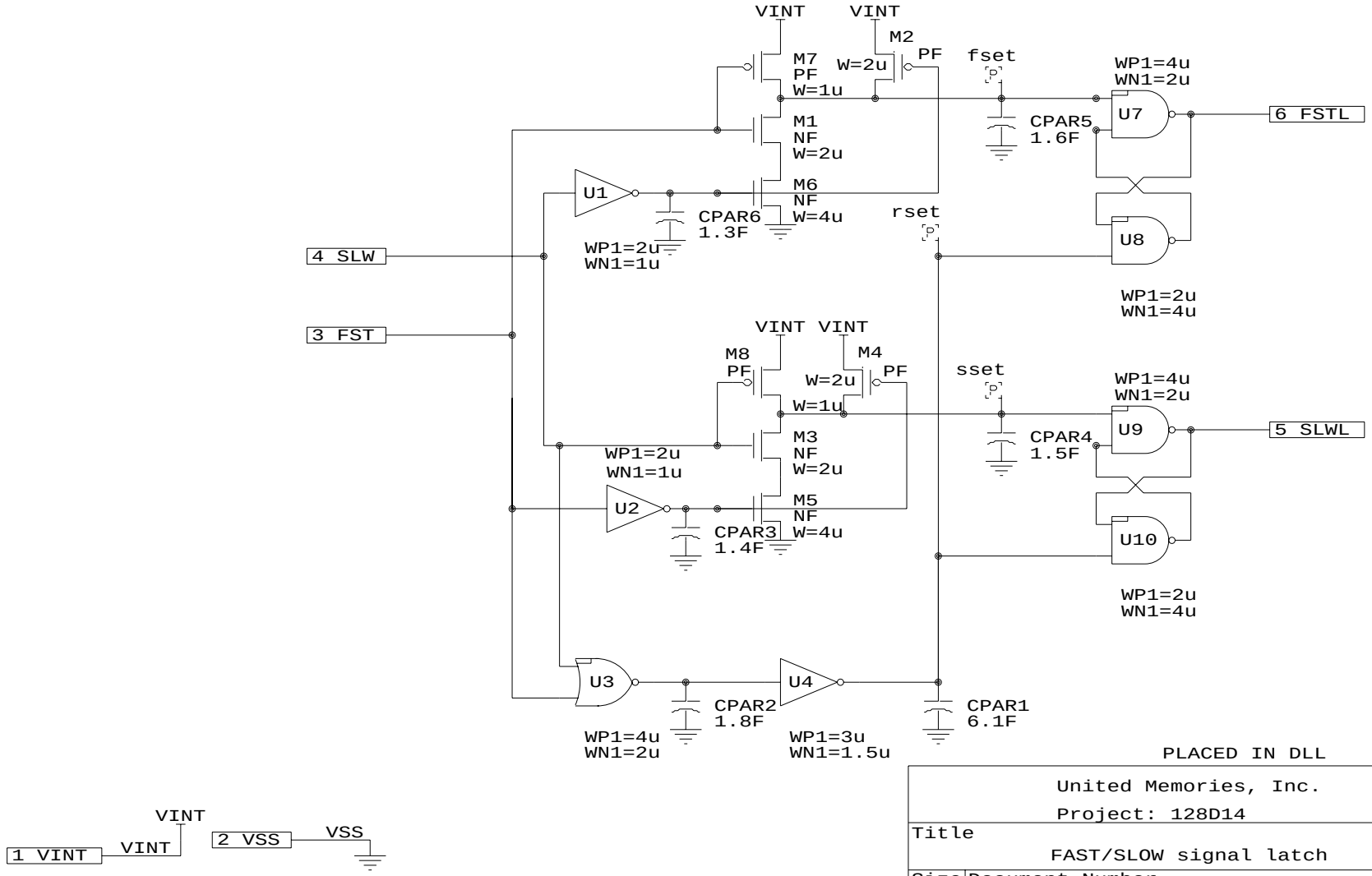


600 ps per pair @ VINT=2.0V 45C

PLACED IN DLL

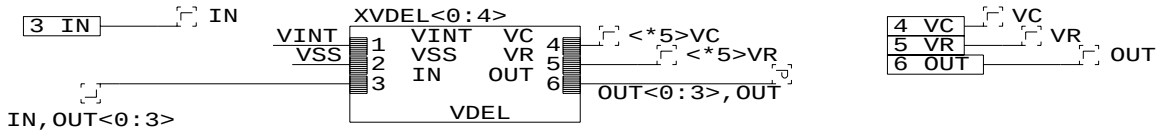


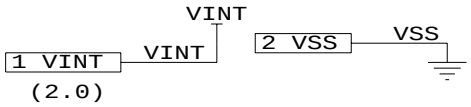
United Memories, Inc. Project: 128D14		
Title Slow Fixed Delay Line		
Size A	Document Number FDELSL	REV A
Date: December 6, 2001	Sheet 1 of 1	



PLACED IN DLL

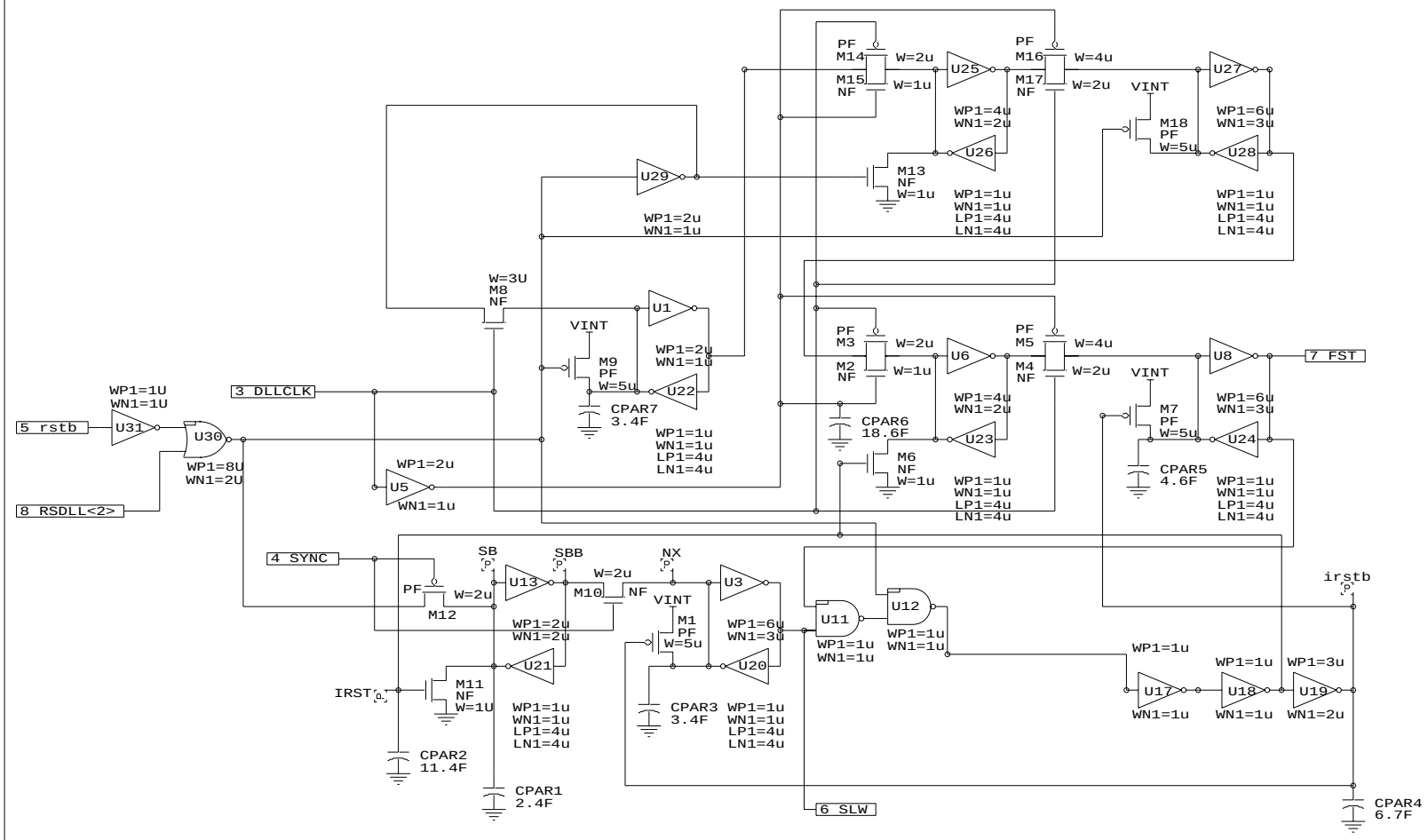
United Memories, Inc. Project: 128D14		
Title FAST/SLOW signal latch		
Size A	Document Number fslat	REV A
Date: September 4, 2001	Sheet 1 of 1	





PLACED IN DLL

United Memories, Inc. Project: 128D14 TopBlock: DLL		
Title ONE-HALF VOLTAGE CONTROLLED DELAY LINE		
Size A	Document Number HVDEL	REV A
Date: September 4, 2001	Sheet 1 of 1	



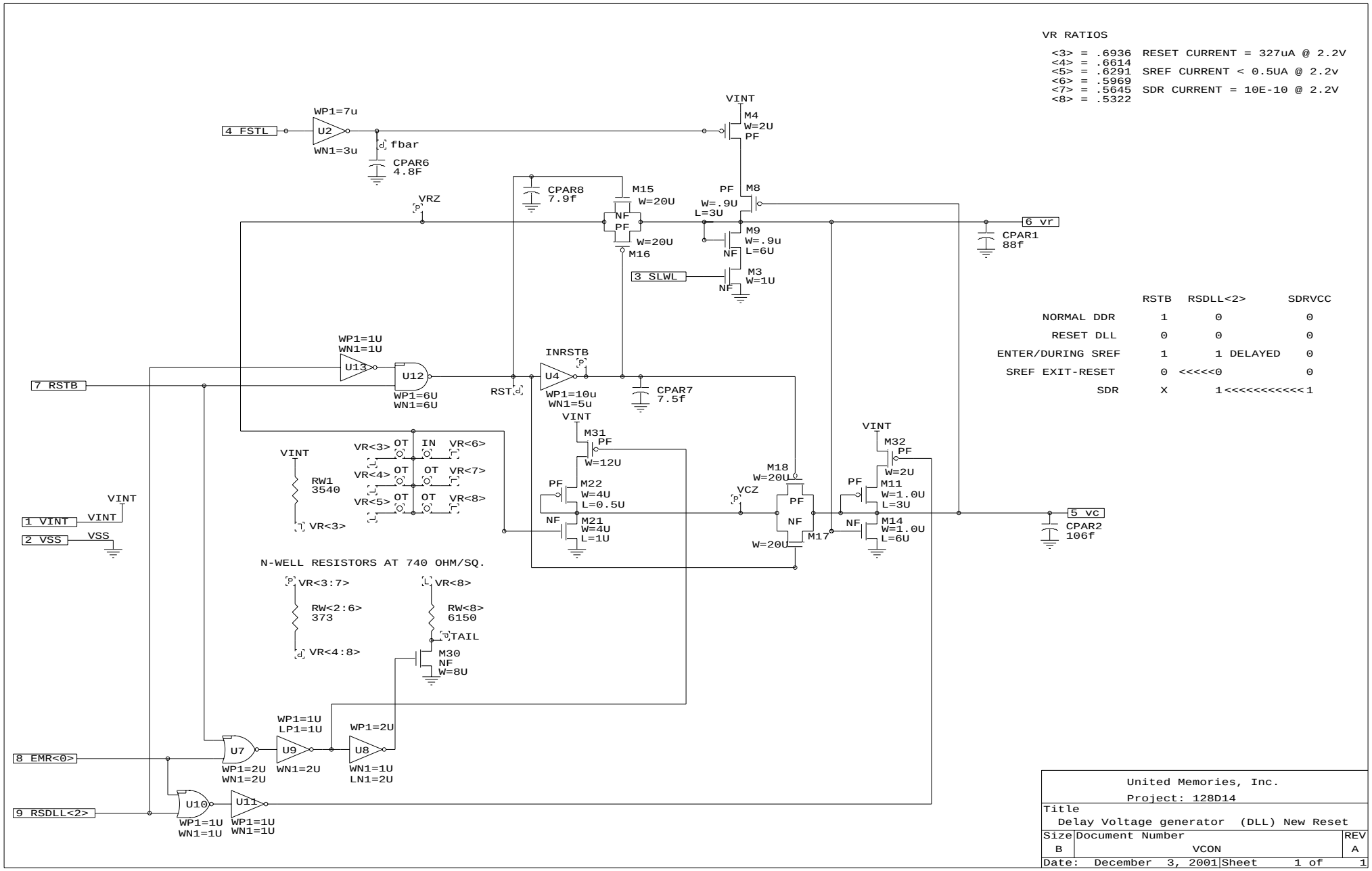
United Memories Inc.

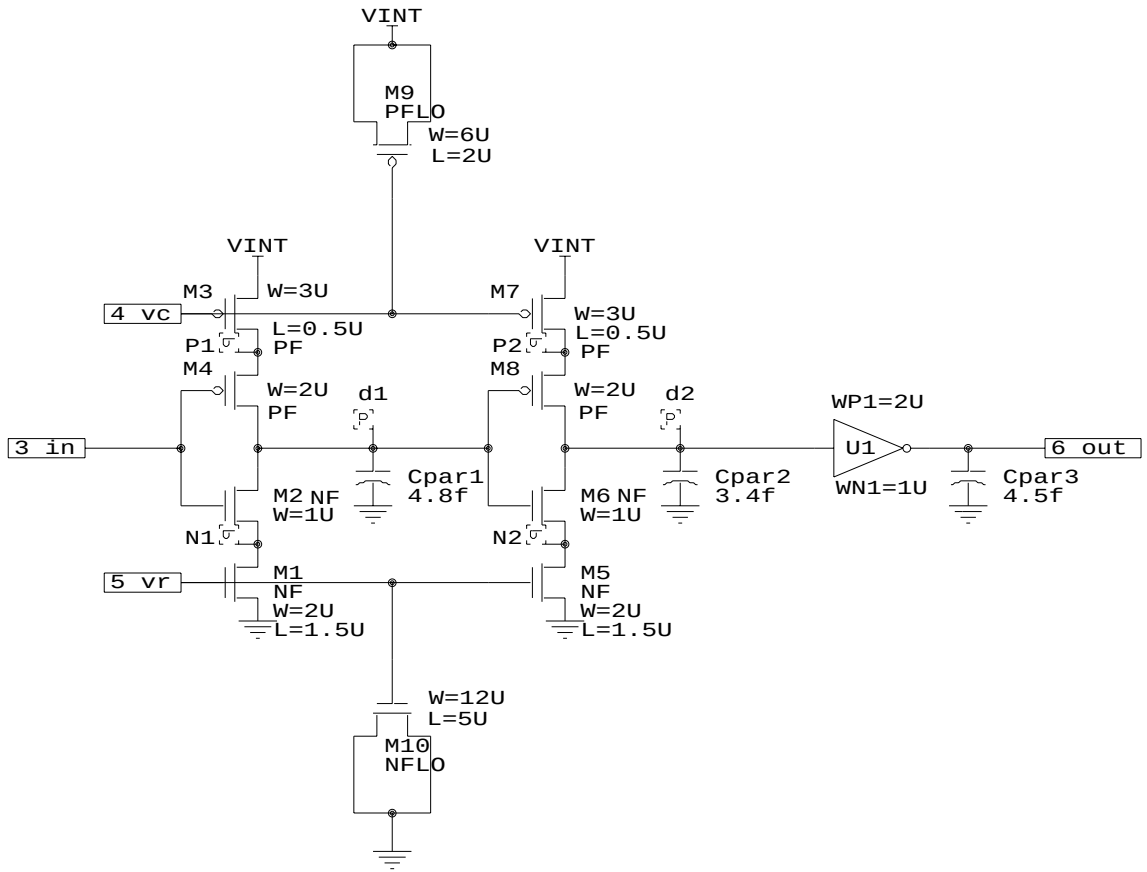
Project: 128D14
TopBlock: DLL

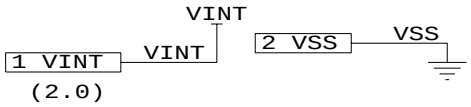
Title
Phase Detector

Size	Document Number	REV
B	PD	A

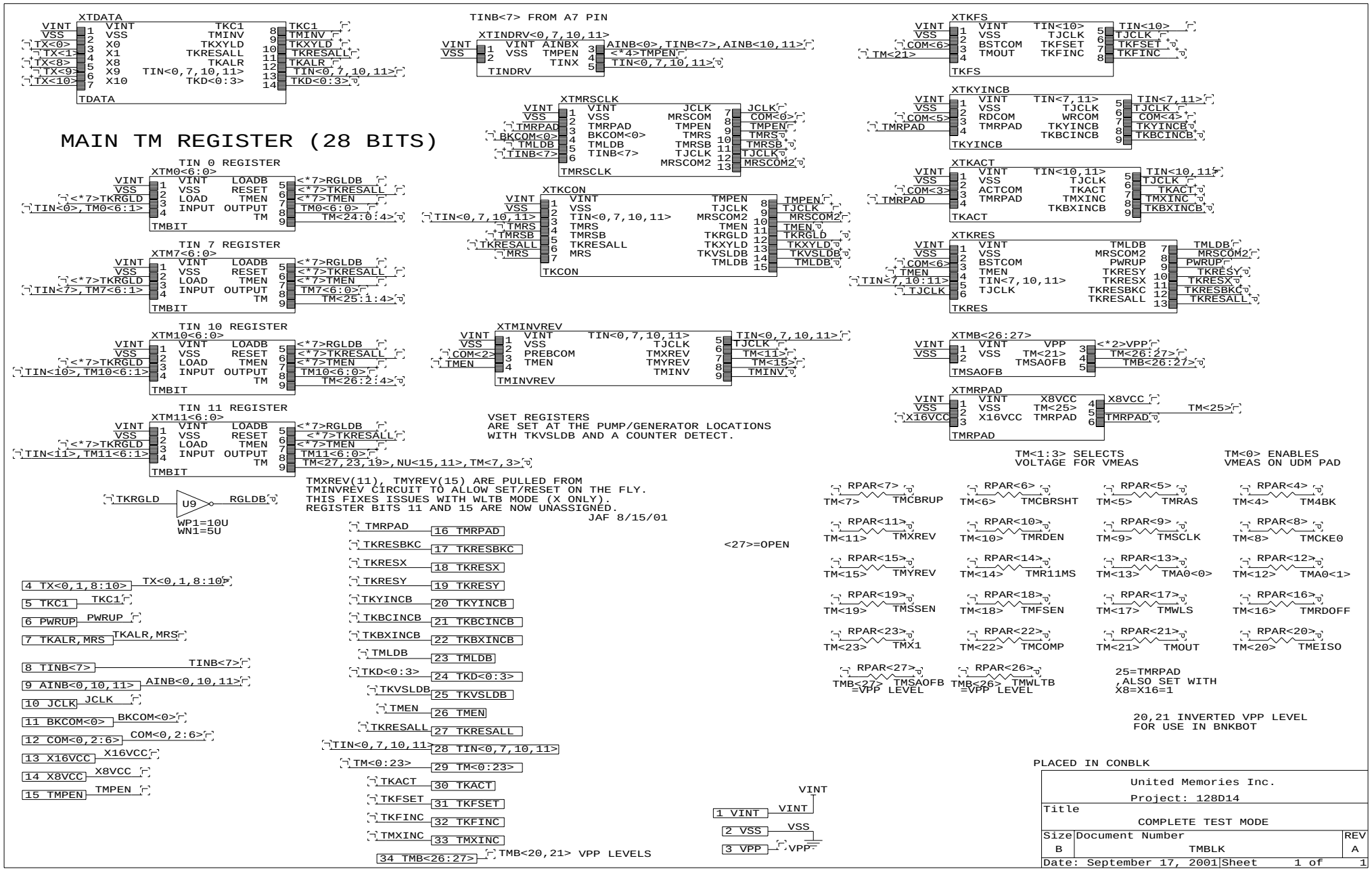
Date: December 3, 2001 | Sheet 1 of 1

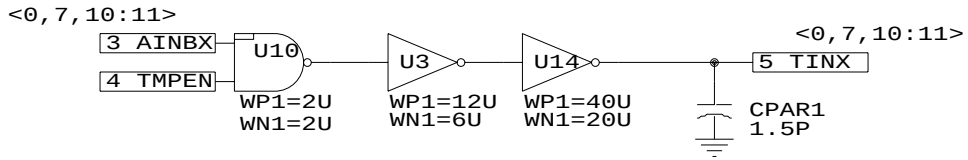

VR RATIOS
<3> = .6936 RESET CURRENT = 327uA @ 2.2V
<4> = .6614
<5> = .6291 SREF CURRENT < 0.5UA @ 2.2v
<6> = .5969
<7> = .5645 SDR CURRENT = 10E-10 @ 2.2V
<8> = .5322
RSTB RSDLL<2> SDRVCC
NORMAL DDR 1 0 0
RESET DLL 0 0 0
ENTER/DURING SREF 1 1 DELAYED 0
SREF EXIT-RESET 0 <<<<<0 0
SDR X 1<<<<<<<<<<<1
4 FSTL
U2
WP1=7u
WN1=3u
fbar
CPAR6
4.8F
VINT
M4
W=2U
PF
CPAR8
7.9f
M15
W=20U
NF
PF
W=20U
M16
VRZ
PF
M8
W=.9U
L=3U
M9
W=.9u
L=6U
NF
3 SLWL
M3
W=1U
NF
6 vr
CPAR1
88f
WP1=1U
WN1=1U
U13
U12
WP1=6U
WN1=6U
7 RSTB
RST
INRSTB
U4
WP1=10u
WN1=5u
CPAR7
7.5f
VINT
M31
PF
W=12U
PF
M22
W=4U
L=0.5U
NF
M21
W=4U
L=1U
VINT
RW1
3540
VR<3>
VR<3> OT IN VR<6>
VR<4> OT OT VR<7>
VR<5> OT OT VR<8>
VINT
1 VINT
VINT
2 VSS
VSS
M18
W=20U
VCZ
PF
NF
M17
W=20U
VINT
M32
PF
W=2U
PF
M11
W=1.0U
L=3U
NF
M14
W=1.0U
L=6U
5 vc
CPAR2
106f
N-WELL RESISTORS AT 740 OHM/SQ.
VR<3:7>
RW<2:6>
373
VR<4:8>
VR<8>
RW<8>
6150
TAIL
M30
NF
W=8U
WP1=1U
LP1=1U
WP1=2U
8 EMR<0>
U7
WP1=2U
WN1=2U
U9
WN1=2U
U8
WN1=1U
LN1=2U
9 RSDLL<2>
U10
WP1=1U
WN1=1U
U11
WP1=1U
WN1=1U
United Memories, Inc.
Project: 128D14
Title
Delay Voltage generator (DLL) New Reset
Size B
Document Number
VCON
REV A
Date: December 3, 2001
Sheet 1 of 1

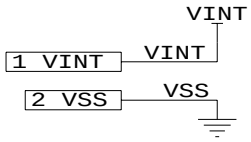




United Memories, Inc. Project: 128D14 TopBlock: DLL		
Title Voltage Controlled Delay Element		
Size A	Document Number vdel	REV A
Date: December 4, 2001	Sheet 1 of 1	


XTDATA
TDATA
VINT VSS TX<0> TX<1> TX<8> TX<9> TX<10>
VINT VSS X0 X1 X8 X9 X10
TKC1 TMINV TKXYLD TKRESALL TKALR TIN<0,7,10,11> TKD<0:3>
TKC1 TMINV TKXYLD TKRESALL TKALR TIN<0,7,10,11> TKD<0:3>
TINB<7> FROM A7 PIN
XTINDRV<0,7,10,11>
VINT VSS
VINT VSS AINBX TMPEN TINX
AINB<0>,TINB<7>,AINB<10,11>
<*4>TMPEN
TIN<0,7,10,11>
TINDRV
XTKFS
VINT VSS COM<6> TM<21>
VINT VSS BSTCOM TMOUT
TIN<10> TJCLK TKFSET TKFINC
TIN<10> TJCLK TKFSET TKFINC
TKFS
XTKYINCB
VINT VSS COM<5> TMRPAD
VINT VSS RDCOM TMRPAD
TIN<7,11> TJCLK WRCOM TKYINCB TKBCINCB
TIN<7,11> TJCLK COM<4> TKYINCB TKBCINCB
TKYINCB
MAIN TM REGISTER (28 BITS)
TIN 0 REGISTER
XTM0<6:0>
VINT VSS <*7>TKRGLD TIN<0>,TM0<6:1>
VINT VSS LOAD INPUT
LOADB RESET TMEN OUTPUT TM
<*7>RGLDB <*7>TKRESALL <*7>TMEN TM0<6:0> TM<24:0:4>
TMBIT
XTMRSCLK
VINT VSS TMRPAD BKCOM<0> TMLDB TINB<7>
VINT VSS TMRPAD BKCOM<0> TMLDB TINB<7>
JCLK MRSCOM TMPEN TMRS TMRSB TJCLK MRSCOM2
JCLK COM<0> TMPEN TMRS TMRSB TJCLK MRSCOM2
TMRSCLK
XTKCON
VINT VSS TIN<0,7,10,11> TMRS TMRSB TKRESALL MRS
VINT VSS TIN<0,7,10,11> TMRS TMRSB TKRESALL MRS
TMPEN TJCLK MRSCOM2 TMEN TKRGLD TKXYLD TKVSLDB TMLDB
TMPEN TJCLK MRSCOM2 TMEN TKRGLD TKXYLD TKVSLDB TMLDB
TKCON
XTKACT
VINT VSS COM<3> TMRPAD
VINT VSS ACTCOM TMRPAD
TIN<10,11> TJCLK TKACT TMXINC TKBXINCB
TIN<10,11> TJCLK TKACT TMXINC TKBXINCB
TKACT
TIN 7 REGISTER
XTM7<6:0>
VINT VSS <*7>TKRGLD TIN<7>,TM7<6:1>
VINT VSS LOAD INPUT
LOADB RESET TMEN OUTPUT TM
<*7>RGLDB <*7>TKRESALL <*7>TMEN TM7<6:0> TM<25:1:4>
TMBIT
XTKRES
VINT VSS COM<6> TMEN TIN<7,10:11> TJCLK
VINT VSS BSTCOM TMEN TIN<7,10,11> TJCLK
TMLDB MRSCOM2 PWRUP TKRESY TKRESX TKRESBKC TKRESALL
TMLDB MRSCOM2 PWRUP TKRESY TKRESX TKRESBKC TKRESALL
TKRES
TIN 10 REGISTER
XTM10<6:0>
VINT VSS <*7>TKRGLD TIN<10>,TM10<6:1>
VINT VSS LOAD INPUT
LOADB RESET TMEN OUTPUT TM
<*7>RGLDB <*7>TKRESALL <*7>TMEN TM10<6:0> TM<26:2:4>
TMBIT
XTMINVREV
VINT VSS COM<2> TMEN
VINT VSS PREBCOM TMEN
TIN<0,7,10,11> TJCLK TMXREV TMYREV TMINV
TIN<0,7,10,11> TJCLK TM<11> TM<15> TMINV
TMINVREV
XTMB<26:27>
VINT VSS
VINT VSS
VPP TM<21> TMSAOFB
<*2>VPP TM<26:27> TMB<26:27>
TMSAOFB
TIN 11 REGISTER
XTM11<6:0>
VINT VSS <*7>TKRGLD TIN<11>,TM11<6:1>
VINT VSS LOAD INPUT
LOADB RESET TMEN OUTPUT TM
<*7>RGLDB <*7>TKRESALL <*7>TMEN TM11<6:0> TM<27,23,19>,NU<15,11>,TM<7,3>
TMBIT
VSET REGISTERS
ARE SET AT THE PUMP/GENERATOR LOCATIONS
WITH TKVSLDB AND A COUNTER DETECT.
XTMRPAD
VINT VSS X16VCC
VINT VSS X16VCC
X8VCC TM<25> TMRPAD
X8VCC TM<25> TMRPAD
TMRPAD
TM<1:3> SELECTS
VOLTAGE FOR VMEAS
TM<0> ENABLES
VMEAS ON UDM PAD
TMXREV(11), TMYREV(15) ARE PULLED FROM
TMINVREV CIRCUIT TO ALLOW SET/RESET ON THE FLY.
THIS FIXES ISSUES WITH WLTB MODE (X ONLY).
REGISTER BITS 11 AND 15 ARE NOW UNASSIGNED.
JAF 8/15/01
TKRGLD U9 RGLDB
WP1=10U
WN1=5U
RPAR<7> TM<7> TMCBRUP
RPAR<6> TM<6> TMCBRSHT
RPAR<5> TM<5> TMRAS
RPAR<4> TM<4> TM4BK
RPAR<11> TM<11> TMXREV
RPAR<10> TM<10> TMRDEN
RPAR<9> TM<9> TMSCLK
RPAR<8> TM<8> TMCKE0
RPAR<15> TM<15> TMYREV
RPAR<14> TM<14> TMR11MS
RPAR<13> TM<13> TMA0<0>
RPAR<12> TM<12> TMA0<1>
RPAR<19> TM<19> TMSSEN
RPAR<18> TM<18> TMFSEN
RPAR<17> TM<17> TMWLS
RPAR<16> TM<16> TMRDOFF
RPAR<23> TM<23> TMX1
RPAR<22> TM<22> TMCOMP
RPAR<21> TM<21> TMOUT
RPAR<20> TM<20> TMEISO
RPAR<27> TMB<27> TMSAOFB =VPP LEVEL
RPAR<26> TMB<26> TMWLTB =VPP LEVEL
25=TMRPAD
,ALSO SET WITH
X8=X16=1
20,21 INVERTED VPP LEVEL
FOR USE IN BNKBOT
<27>=OPEN
4 TX<0,1,8:10> TX<0,1,8:10>
5 TKC1 TKC1
6 PWRUP PWRUP
7 TKALR,MRS TKALR,MRS
8 TINB<7> TINB<7>
9 AINB<0,10,11> AINB<0,10,11>
10 JCLK JCLK
11 BKCOM<0> BKCOM<0>
12 COM<0,2:6> COM<0,2:6>
13 X16VCC X16VCC
14 X8VCC X8VCC
15 TMPEN TMPEN
TMRPAD 16 TMRPAD
TKRESBKC 17 TKRESBKC
TKRESX 18 TKRESX
TKRESY 19 TKRESY
TKYINCB 20 TKYINCB
TKBCINCB 21 TKBCINCB
TKBXINCB 22 TKBXINCB
TMLDB 23 TMLDB
TKD<0:3> 24 TKD<0:3>
TKVSLDB 25 TKVSLDB
TMEN 26 TMEN
TKRESALL 27 TKRESALL
TIN<0,7,10,11> 28 TIN<0,7,10,11>
TM<0:23> 29 TM<0:23>
TKACT 30 TKACT
TKFSET 31 TKFSET
TKFINC 32 TKFINC
TMXINC 33 TMXINC
34 TMB<26:27> TMB<20,21> VPP LEVELS
VINT
1 VINT VINT
2 VSS VSS
3 VPP VPP
PLACED IN CONBLK
United Memories Inc.
Project: 128D14
Title
COMPLETE TEST MODE
Size B
Document Number TMBLK
REV A
Date: September 17, 2001
Sheet 1 of 1

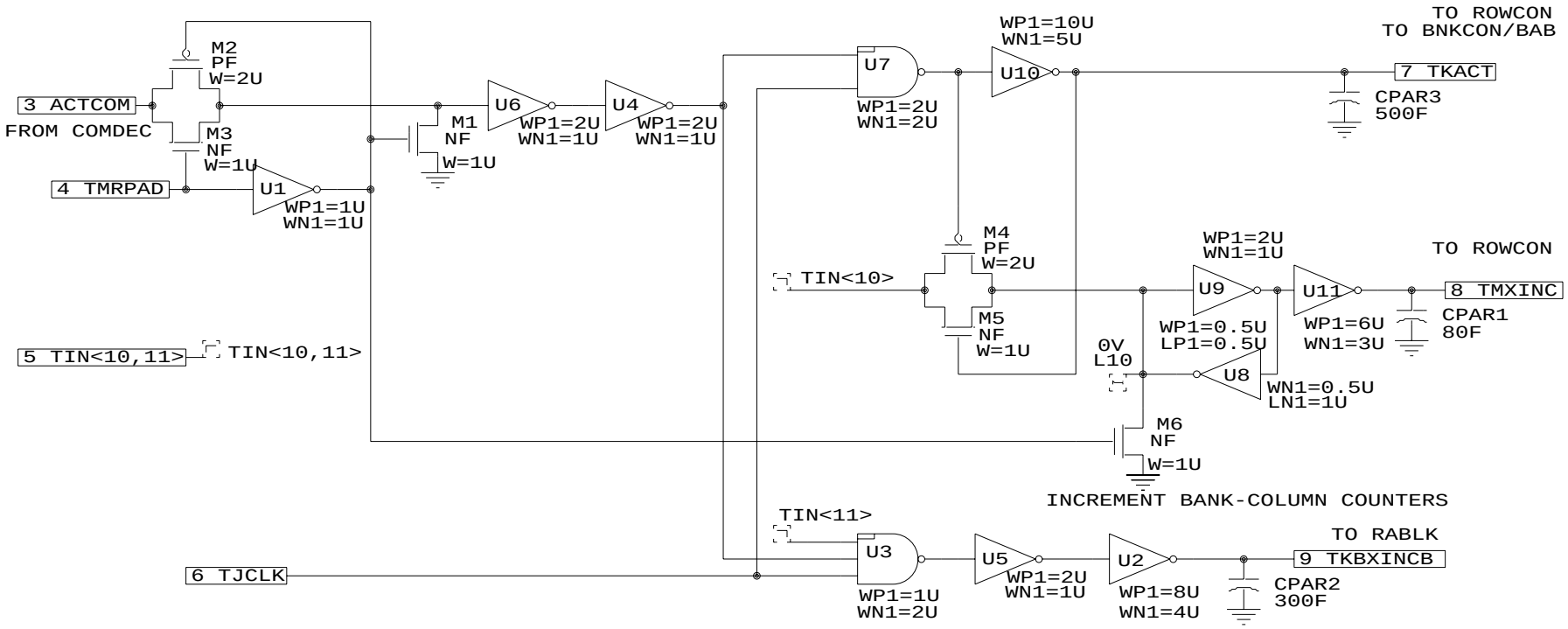




TIN SIGNALS POWER GATED WITH
TMPEN TO SAVE POWER IN NORMAL MODE.

PLACED IN CONBLK
PLACED IN TMBLK

United Memories Inc. Project: 128D14		
Title TIN DRIVERS <0,7,10:11>		
Size A	Document Number TINDRV	REV A
Date: October 12, 2001	Sheet 1 of 1	



IN REDUCED PAD TEST MODE

A11 A10 OPERATION

X 1 INCREMENT X-ADDRESS COUNTERS
(DONE IN ROWCON WITH REFB)

1 X INCREMENT BANK ROW COUNTERS

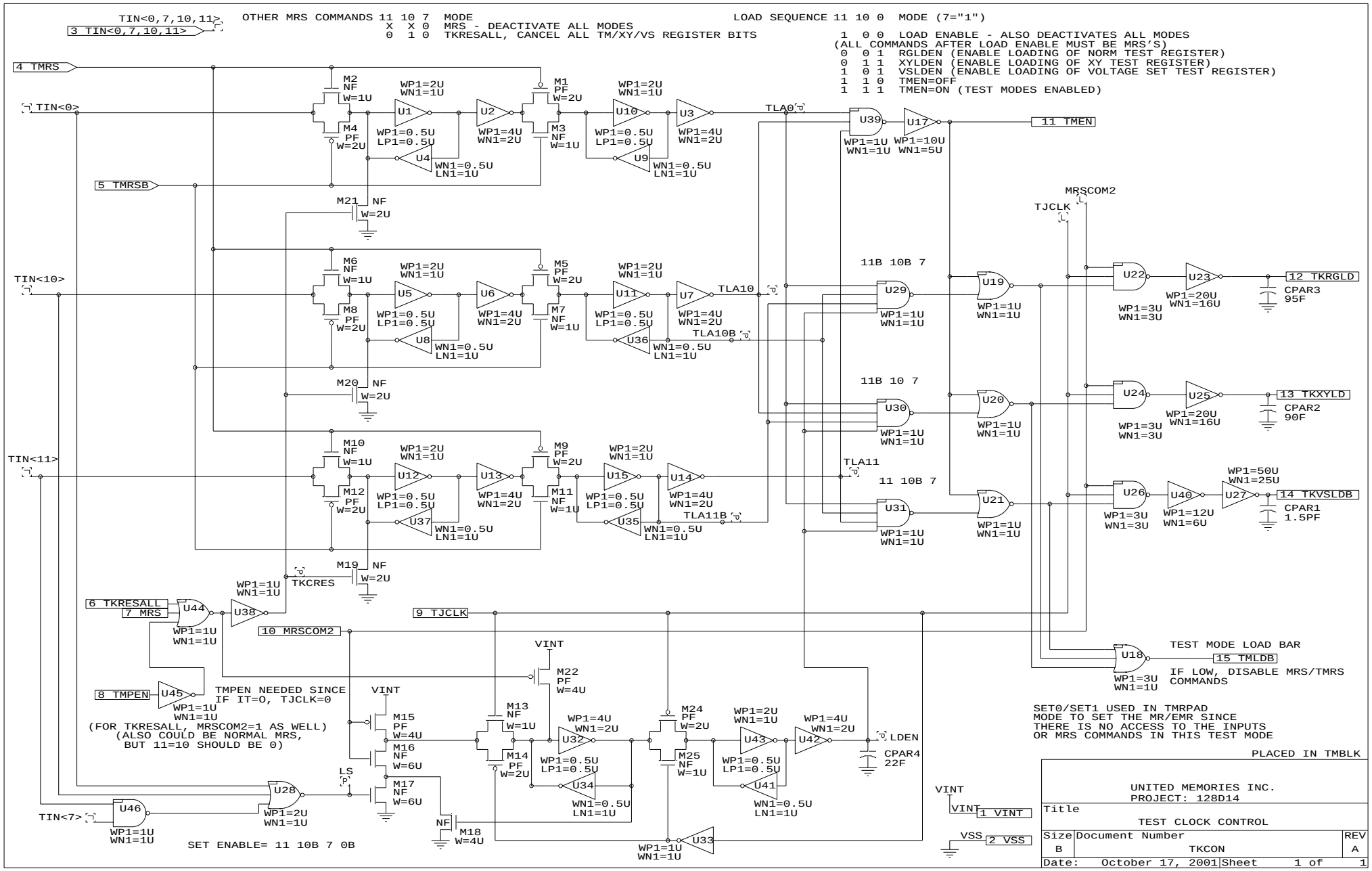
(BOTH, OR ANY COMBINATION THERE OF,
CAN BE EXECUTED SIMULTANEOUSLY)

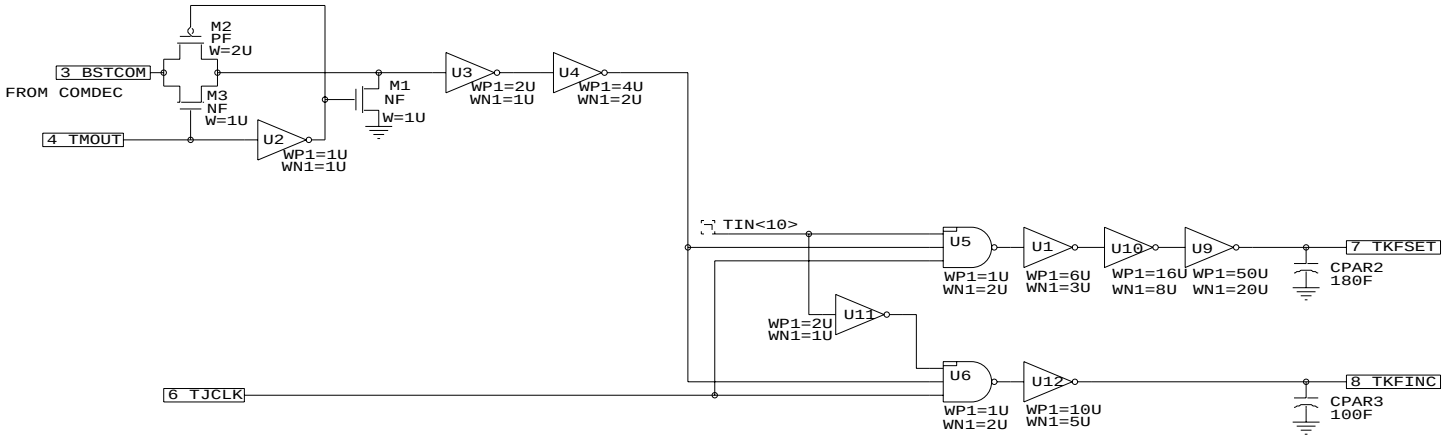
NEW FOR 128D14

VINT
VINT 1 VINT
VSS 2 VSS

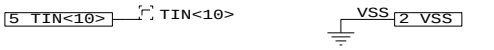
PLACED IN CONBLK

United Memories, Inc. PROJECT: 128D14		
Title TEST MODE -ACTIVE, XINC, AND BKXINC		
Size A	Document Number TKACT	REV A
Date: December 10, 2001	Sheet 1 of 1	


TIN<0,7,10,11>
3 TIN<0,7,10,11>
OTHER MRS COMMANDS 11 10 7 MODE
X X 0 MRS - DEACTIVATE ALL MODES
0 1 0 TKRESALL, CANCEL ALL TM/XY/VS REGISTER BITS
LOAD SEQUENCE 11 10 0 MODE (7="1")
1 0 0 LOAD ENABLE - ALSO DEACTIVATES ALL MODES
(ALL COMMANDS AFTER LOAD ENABLE MUST BE MRS'S)
0 0 1 RGLDEN (ENABLE LOADING OF NORM TEST REGISTER)
0 1 1 XYLDEN (ENABLE LOADING OF XY TEST REGISTER)
1 0 1 VSLDEN (ENABLE LOADING OF VOLTAGE SET TEST REGISTER)
1 1 0 TMEN=OFF
1 1 1 TMEN=ON (TEST MODES ENABLED)
4 TMRS
TIN<0>
5 TMRSB
TIN<10>
TIN<11>
6 TKRESALL
7 MRS
8 TMPEN
9 TJCLK
10 MRSCOM2
TIN<7>
11 TMEN
12 TKRGLD
13 TKXYLD
14 TKVSLDB
15 TMLDB
TLA0
TLA10
TLA10B
TLA11
TLA11B
11B 10B 7
11B 10 7
11 10B 7
MRSCOM2
TJCLK
TKCRES
LS
LDEN
VINT
VSS
1 VINT
2 VSS
CPAR3 95F
CPAR2 90F
CPAR1 1.5PF
CPAR4 22F
TEST MODE LOAD BAR
IF LOW, DISABLE MRS/TMRS COMMANDS
TMPEN NEEDED SINCE IF IT=0, TJCLK=0
(FOR TKRESALL, MRSCOM2=1 AS WELL)
(ALSO COULD BE NORMAL MRS, BUT 11=10 SHOULD BE 0)
SET ENABLE= 11 10B 7 0B
SET0/SET1 USED IN TMRPAD MODE TO SET THE MR/EMR SINCE THERE IS NO ACCESS TO THE INPUTS OR MRS COMMANDS IN THIS TEST MODE
PLACED IN TMBLK
UNITED MEMORIES INC.
PROJECT: 128D14
Title
TEST CLOCK CONTROL
Size B
Document Number TKCON
REV A
Date: October 17, 2001
Sheet 1 of 1



BSTCOM	TIN<10>	TMOUT	TJCLK	TKFSET	TKFINC
1	1	1	1	1	0
	0	1	1	0	1



PLACED IN TMBLK

United Memories, Inc.

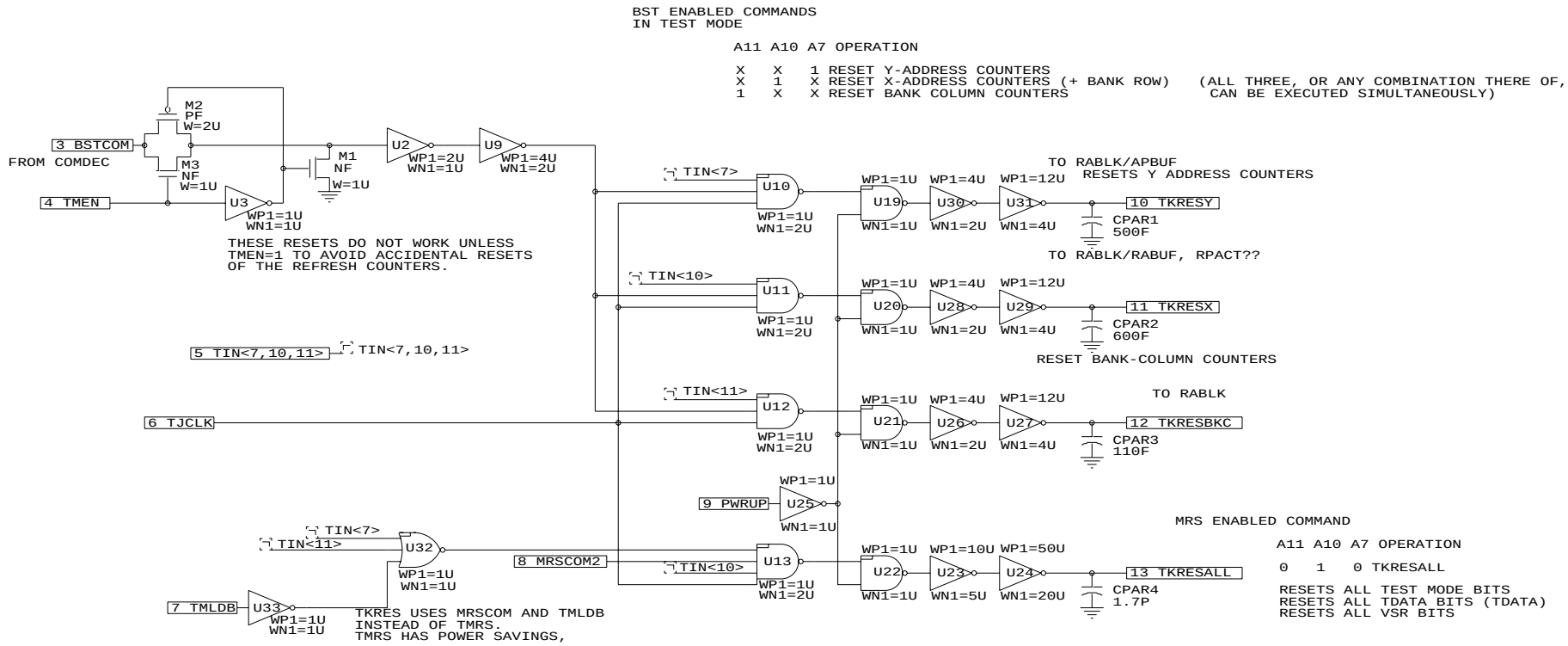
PROJECT: 128D14

Title

TEST MODE RESET - FUSE ID SET/SHIFT

Size	Document Number	REV
B	TKFS	A

Date: October 12, 2001 Sheet 1 of 1



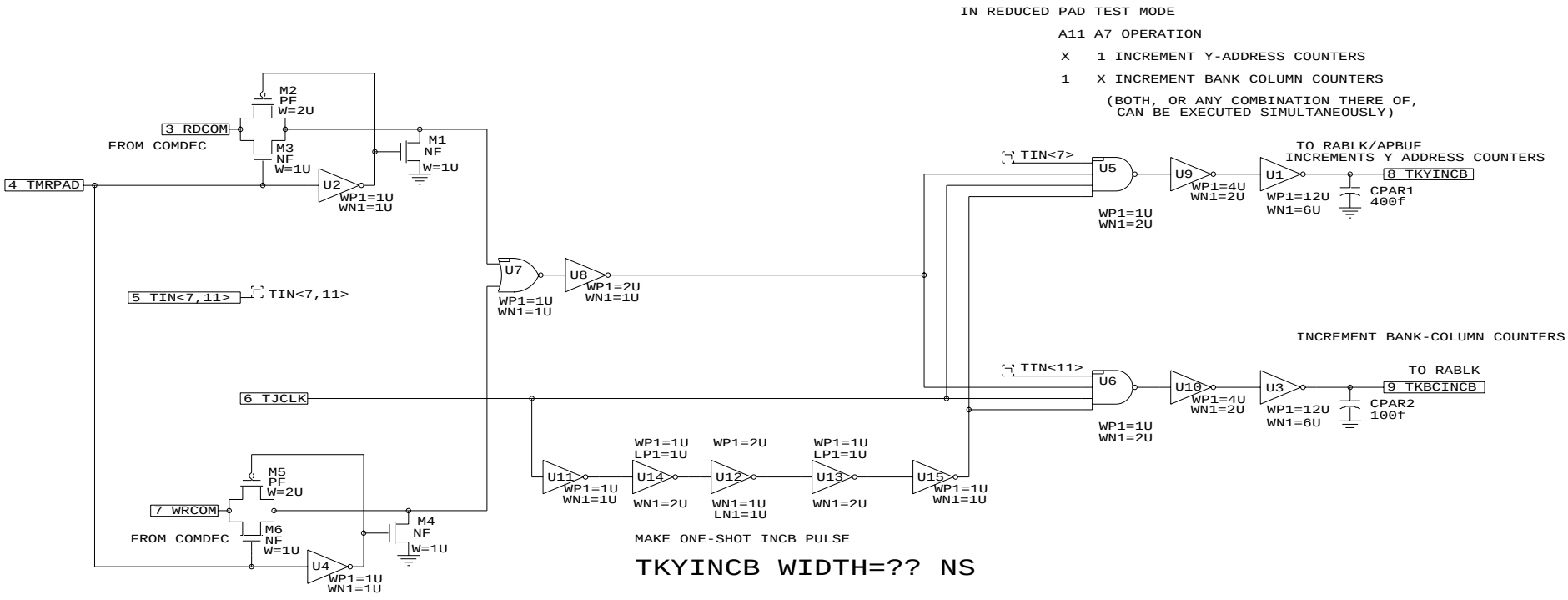
THE TMEN BIT CAN BE DISABLED BY ANY MRS
OR TMRS COMMAND WITH A7/A10/A11 NOT ALL=1.

TIN<7,10,11>,MRSCOM2,TJLK=0
UNLESS TMPEN (EMR<6>)=1
OR REDPAD=1

PLACED IN TMBLK

VINT
VINT 1 VINT
VSS 2 VSS

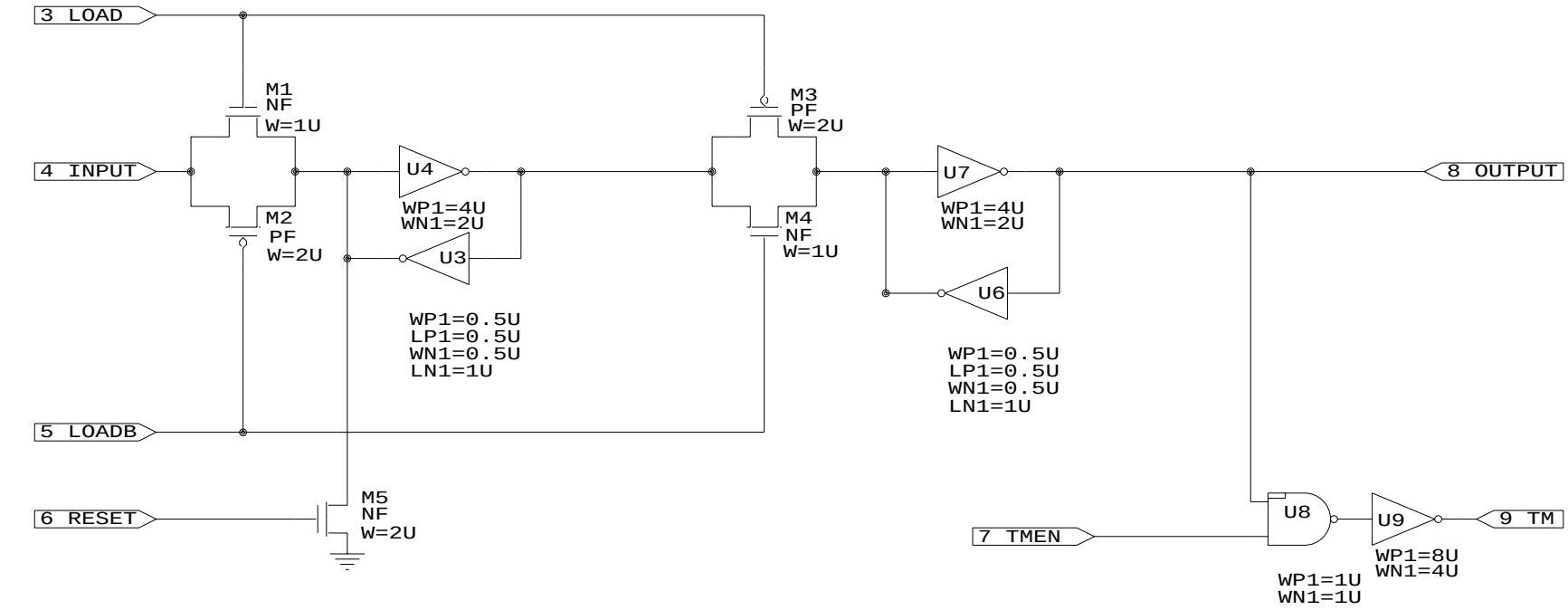
United Memories, Inc.		
PROJECT: 128D14		
Title TEST MODE RESET - X,Y,BKC,ALL		
Size B	Document Number TKRES	REV A
Date: October 12, 2001	Sheet 1 of 1	



PLACED IN TMBLK

VINT
VINT 1 VINT
VSS 2 VSS

United Memories, Inc.	
PROJECT: 128D14	
Title	
TEST MODE Y AND BANK-COL INCREMENT CONTROL	
Size B	Document Number TKYINCB REV A
Date: October 12, 2001	Sheet 1 of 1



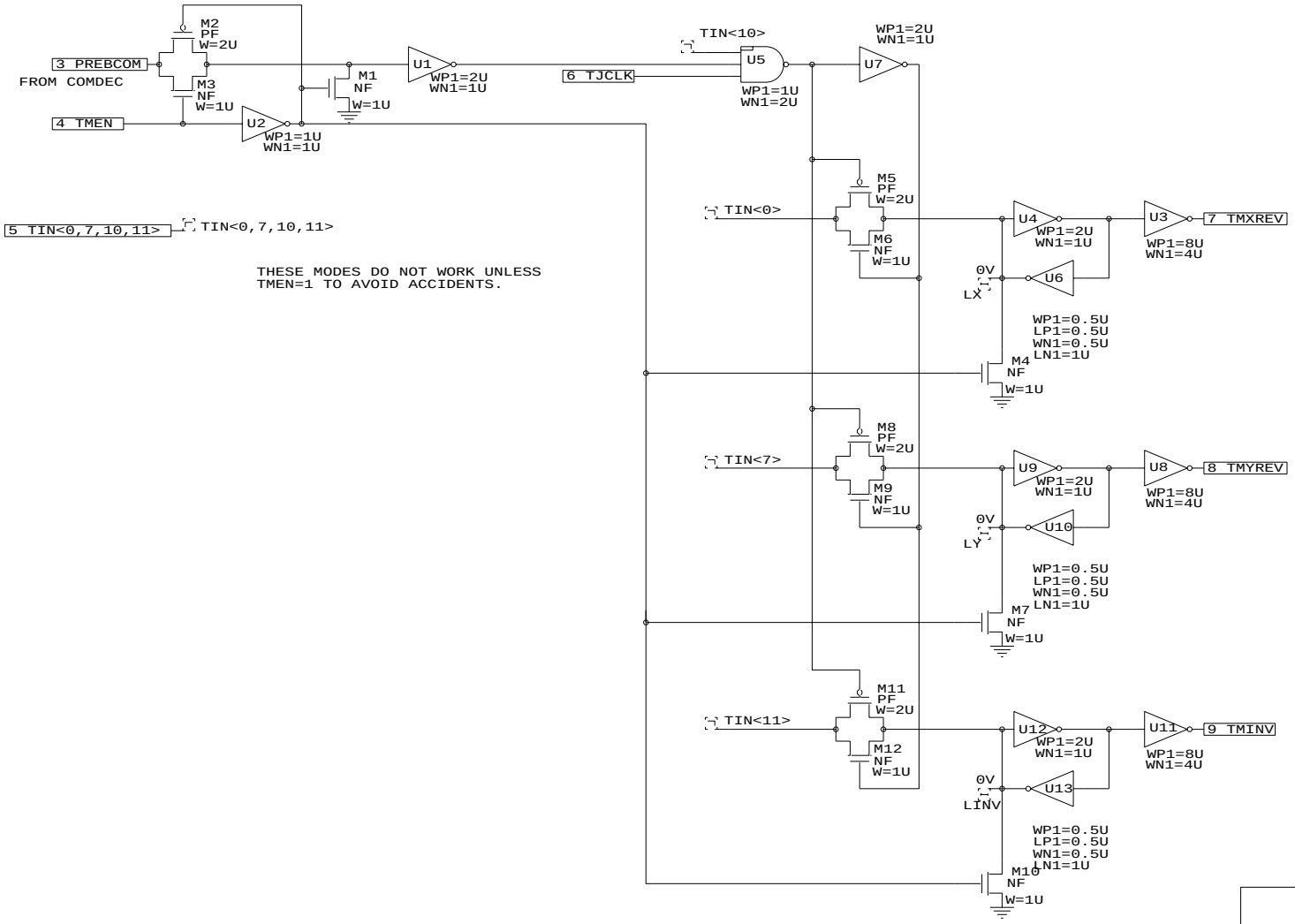
PLACED IN TMBLK

UNITED MEMORIES INC.
PROJECT: 128D14

Title		
	Test Mode Bit	
Size A	Document Number TMBIT	REV A
Date: August 24, 2001	Sheet 1 of 1	

PRE-ALL ENABLED COMMANDS (A10=1)
(NO CHANGES FOR A10=0, SINGLE BANK PRECHARGE

(ALL THREE, OR ANY COMBINATION THERE OF,
CAN BE EXECUTED SIMULTANEOUSLY)



THESE MODES DO NOT WORK UNLESS
TMEN=1 TO AVOID ACCIDENTS.

A10	A0	OPERATION
0	X	NO CHANGE
1	0	TMXREV=0
1	1	TMXREV=1 FOR REVERSE COUNTING OF X-COUNTERS

A10	A7	OPERATION
0	X	NO CHANGE
1	0	TMYREV=0
1	1	TMYREV=1 FOR REVERSE COUNTING OF Y-COUNTERS

A10	A11	OPERATION
0	X	NO CHANGE
1	0	TMINV=0
1	1	TMINV=1 FOR FAST INVERSION OF COMPRESSION PATTERNS

NEW FOR 128D14

PLACED IN CONBLK
PLACED IN TMBLK

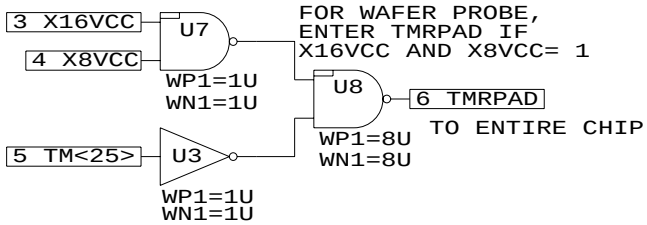
United Memories, Inc.

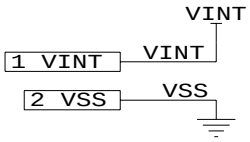
PROJECT: 128D14

Title
TMINV / TMXREV / TMYREV SELECT

Size	Document Number	REV
B	TMINVREV	A

Date: August 14, 2001 | Sheet 1 of 1

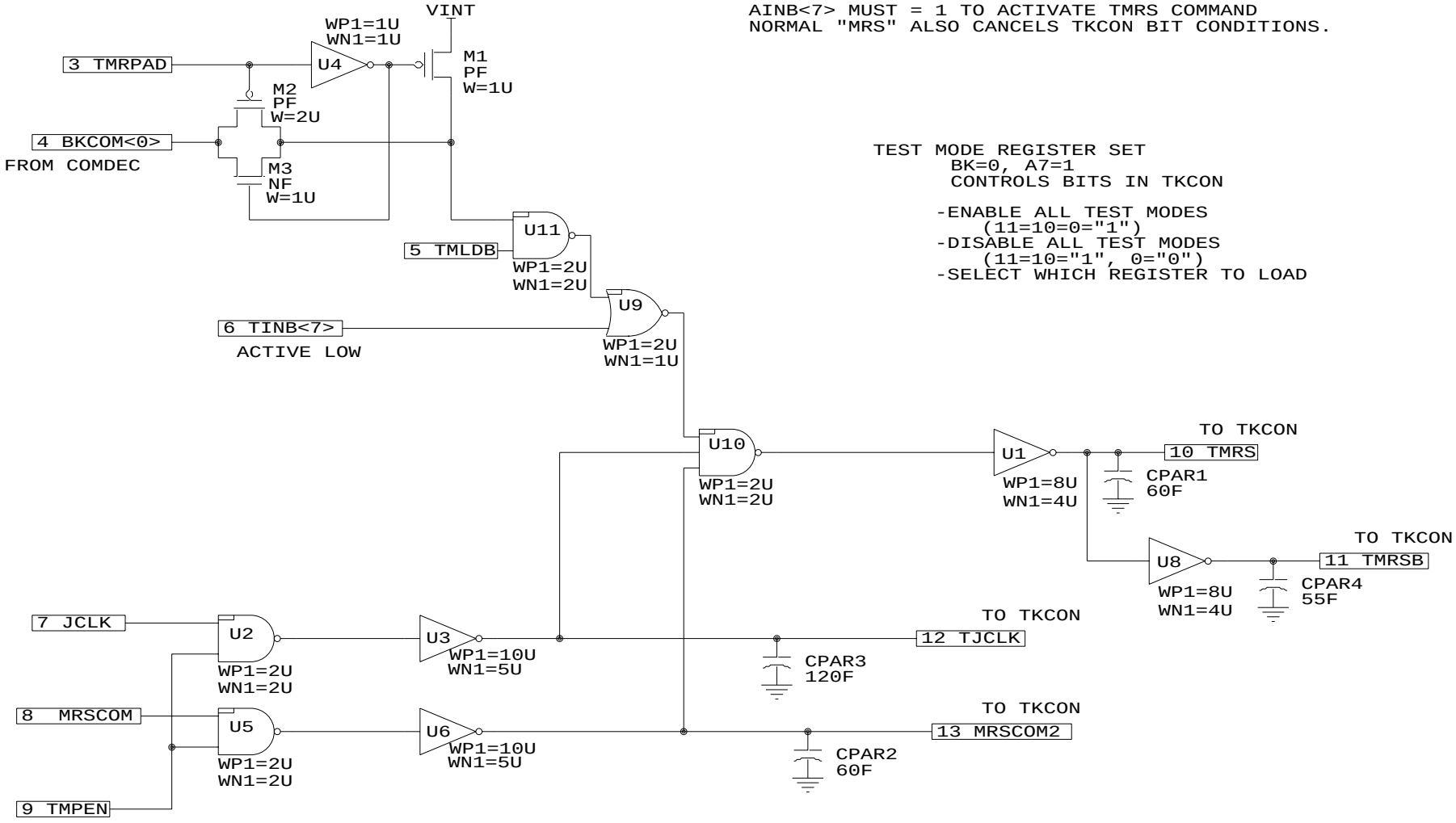




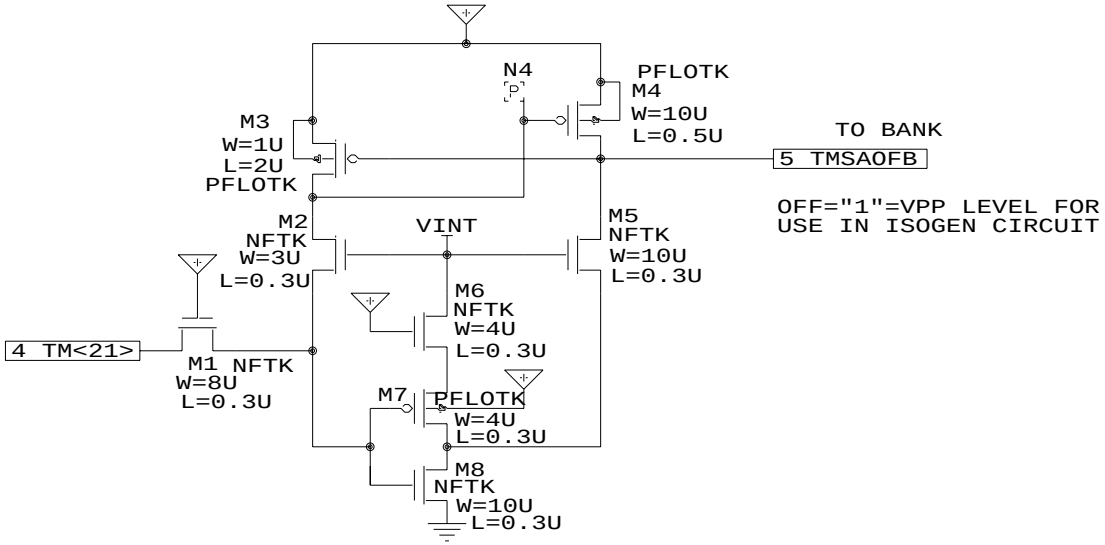
MISCELLANEOUS TEST BLOCK LOGIC

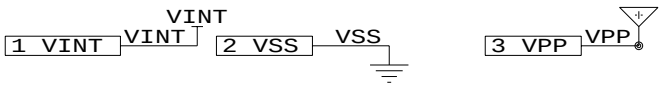
PLACED IN CONBLK
PLACED IN TMBLK

United Memories Inc. Project: 128D14			
Title GENERATE TMRPAD			
Size A	Document Number TMRPAD		REV A
Date: May 31, 2001		Sheet 1 of 1	



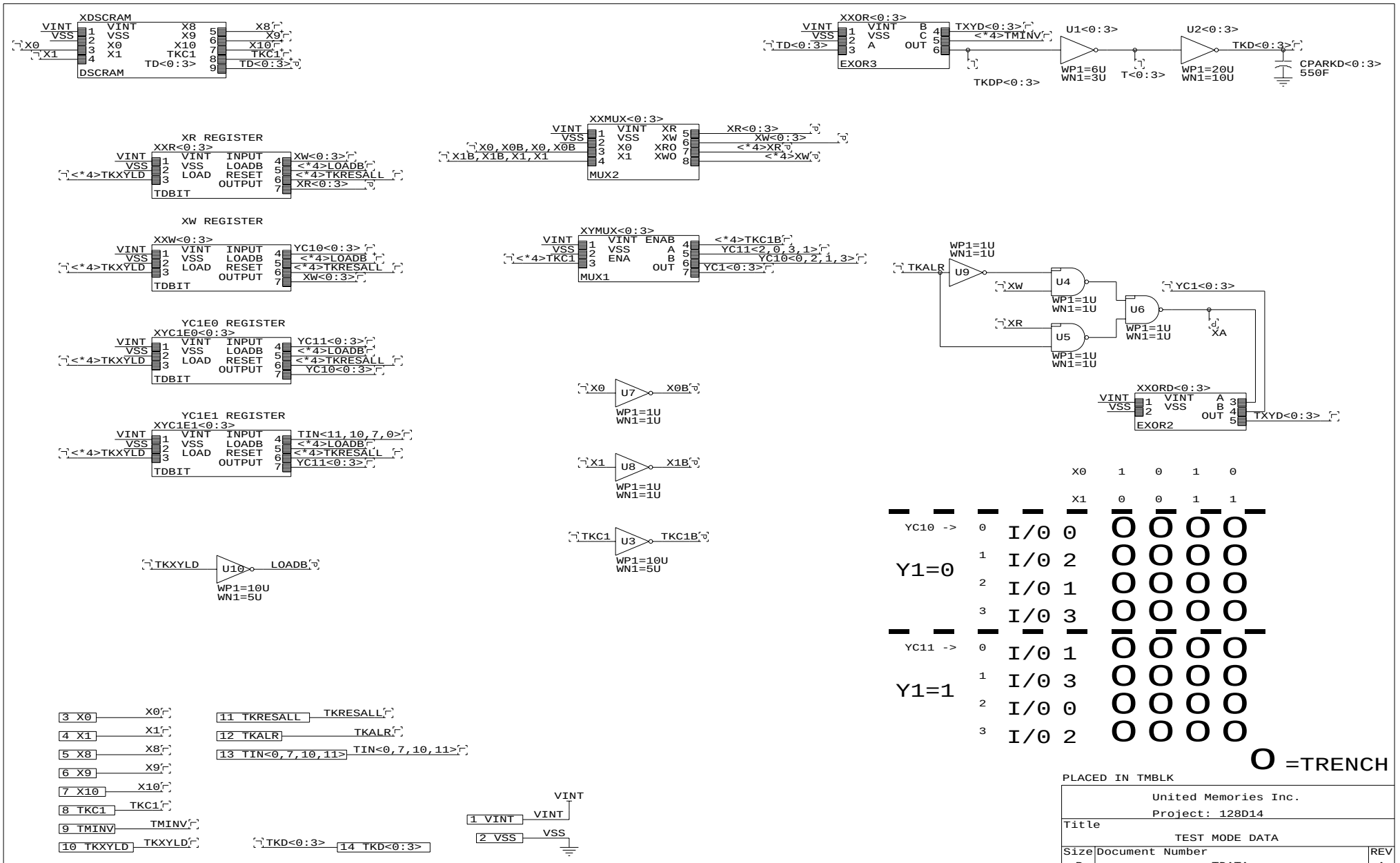
United Memories, Inc.		
PROJECT: 128D14		
Title		
TMRS GENERATION		
Size	Document Number	REV
A	TMRSCLK	A
Date: October 17, 2001	Sheet 1 of 1	





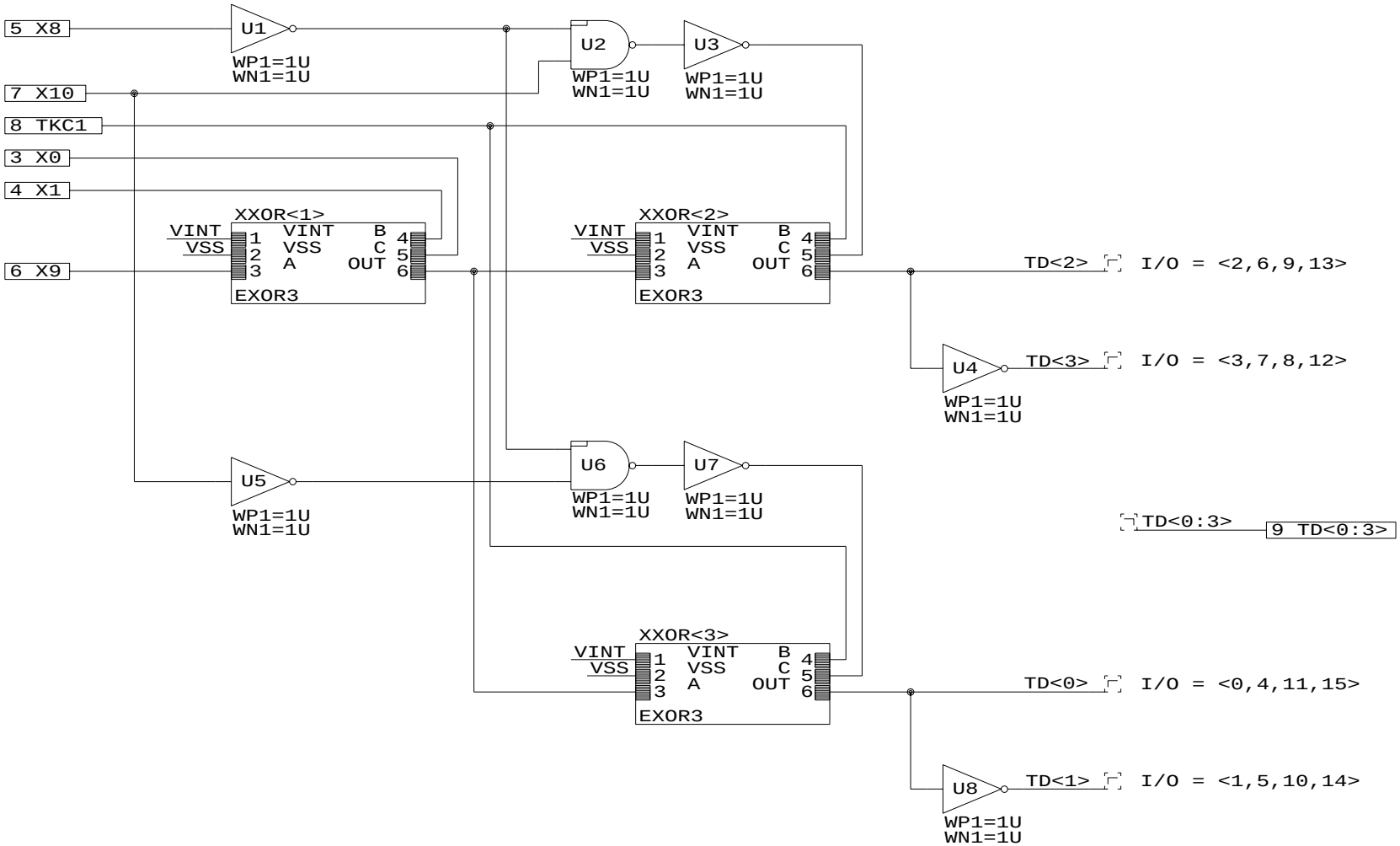
PLACED IN TMBLK

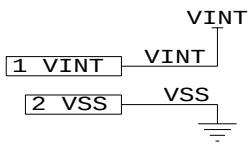
United Memories Inc. Project: 128D14		
Title TEST MODE - SENSE AMP OFF BAR (VPP LEVEL)		
Size A	Document Number TMSAOFB	REV A
Date: May 31, 2001	Sheet 1 of 1	



PLACED IN TMBLK

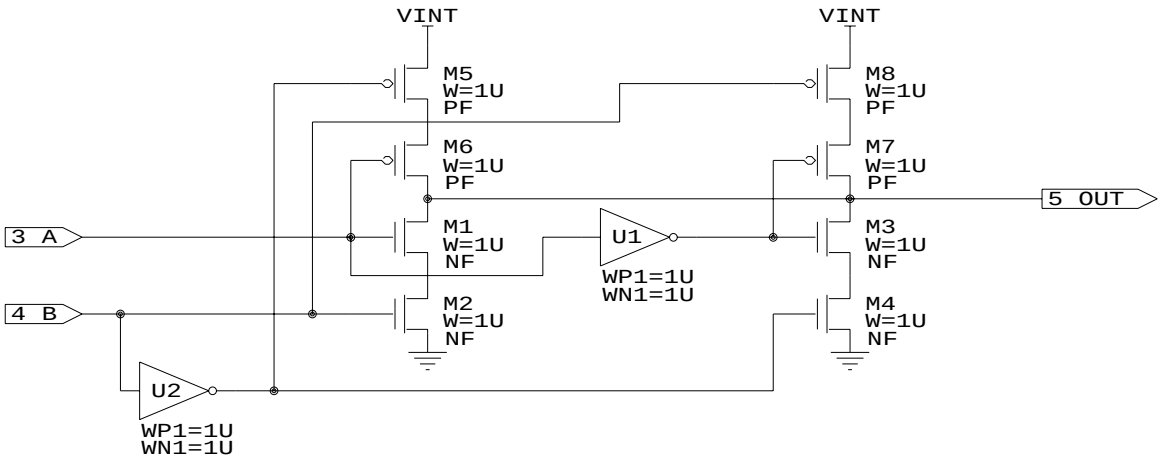
United Memories Inc.		
Project: 128D14		
Title		
TEST MODE DATA		
Size B	Document Number TDATA	REV A
Date: October 12, 2001	Sheet 1 of 1	

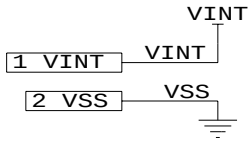




PLACED IN TDATA

United Memories Inc. Project: 128D14		
Title TEST DATA SCRAMBLE		
Size A	Document Number DSCRAM	REV A
Date: August 24, 2001	Sheet 1 of 1	

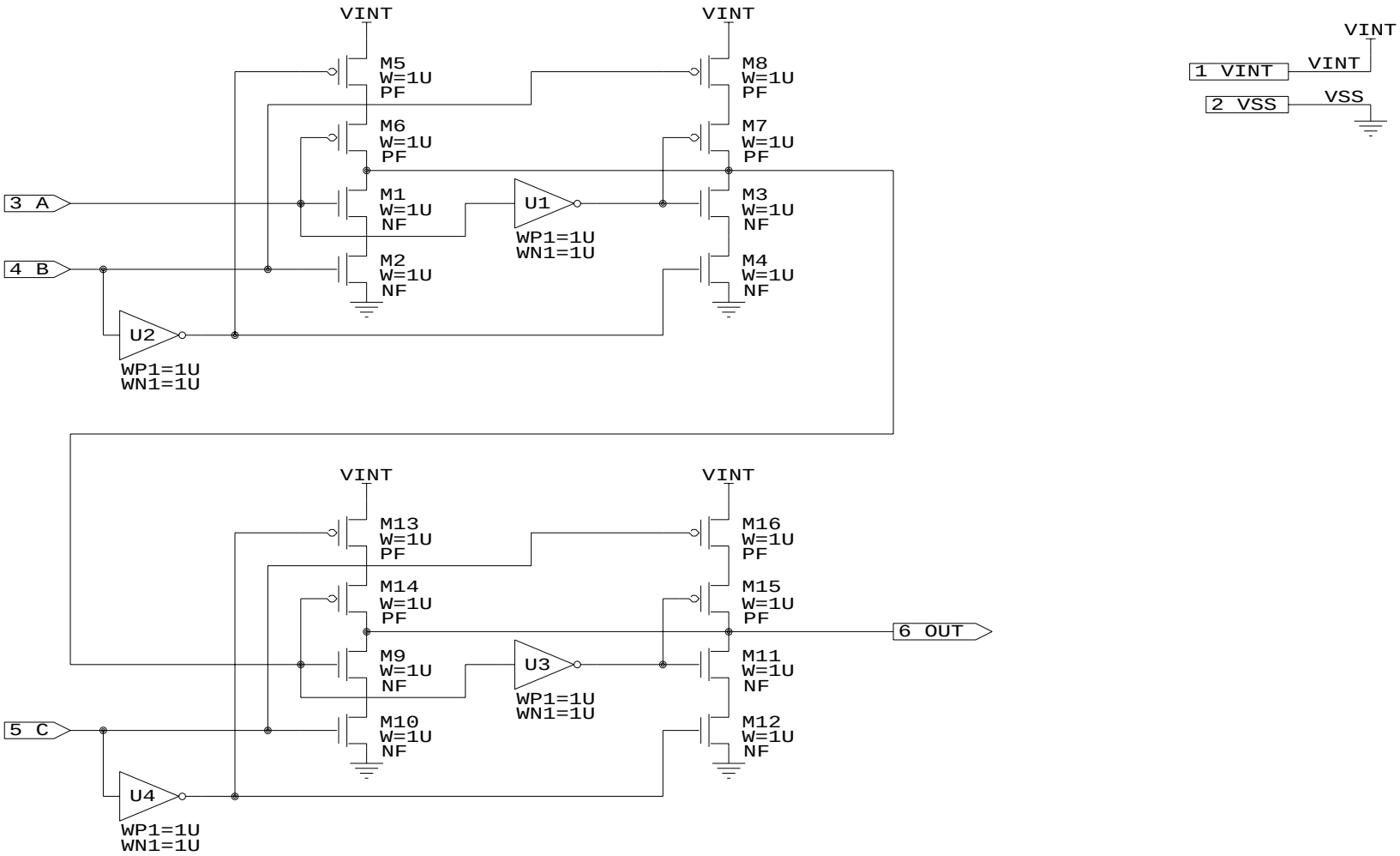




PLACED IN TDATA

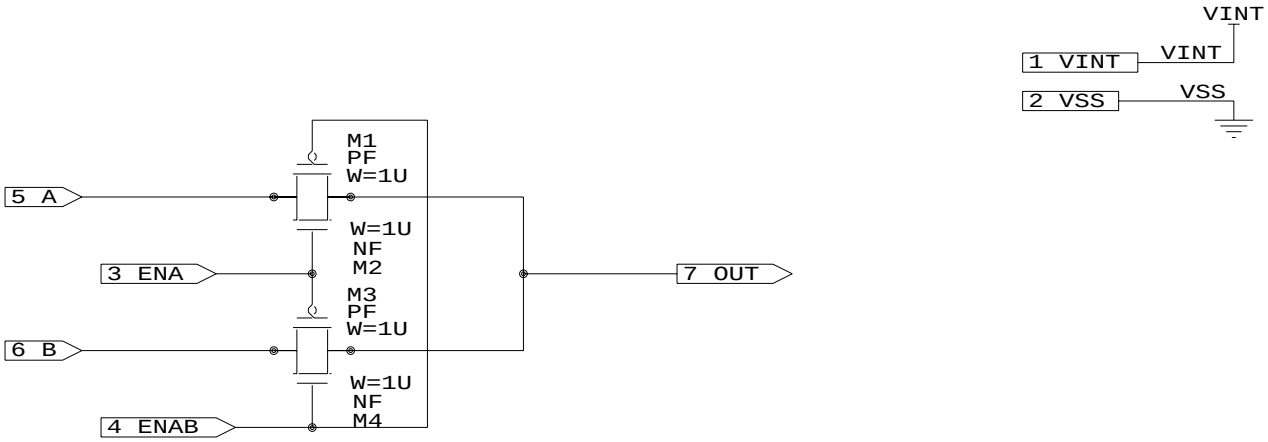
ALSO PLACED IN DPATH/CTMDAT

United Memories Inc. Project: 128D14		
Title 2 INPUT EXOR		
Size A	Document Number EXOR2	REV A
Date: August 24, 2001	Sheet 1 of 1	



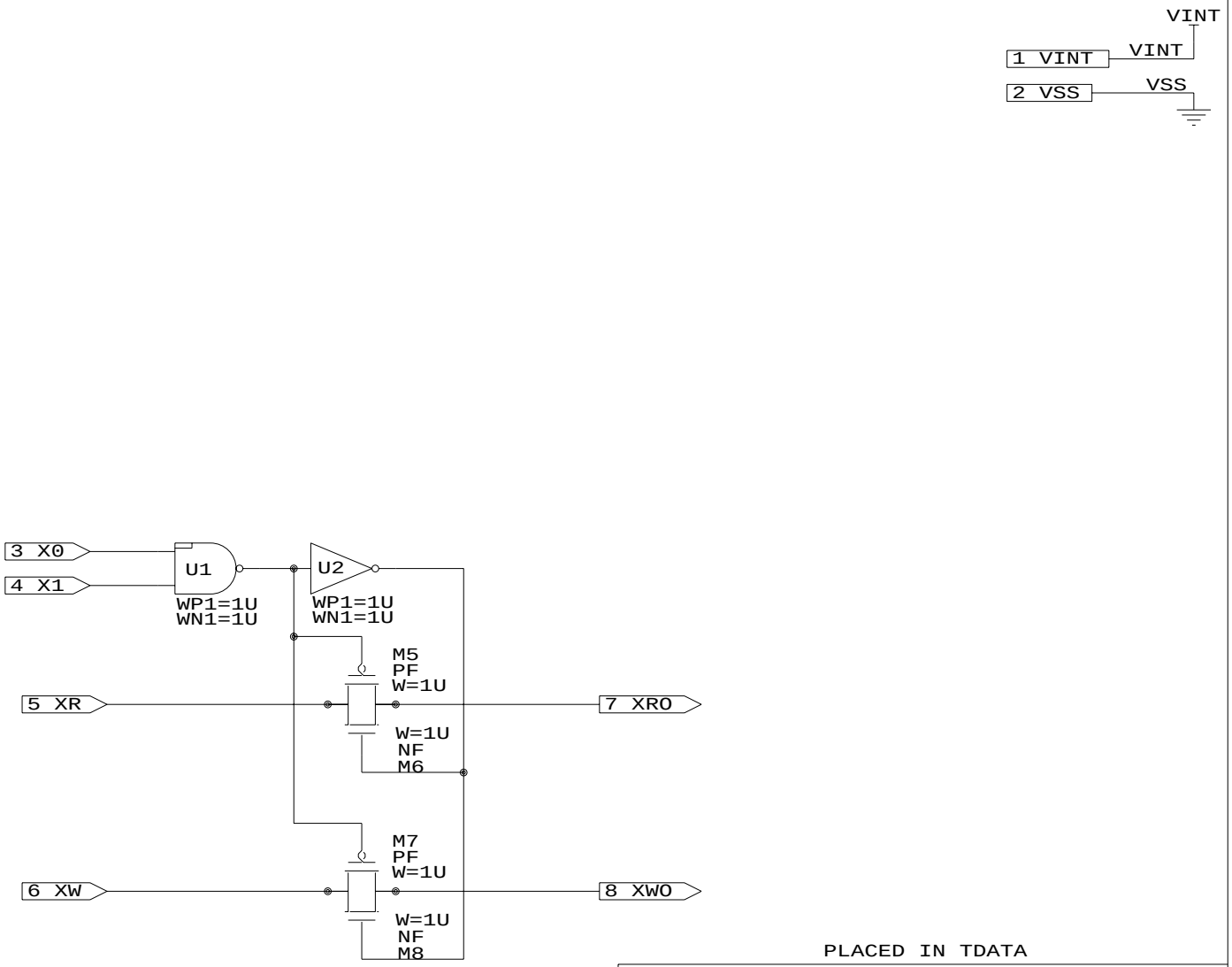
PLACED IN TDATA
PLACED IN TDATA\DSCRAM

United Memories Inc. Project: 128D14		
Title 3 INPUT EXOR		
Size A	Document Number EXOR3	REV A
Date: August 24, 2001	Sheet 1 of 1	



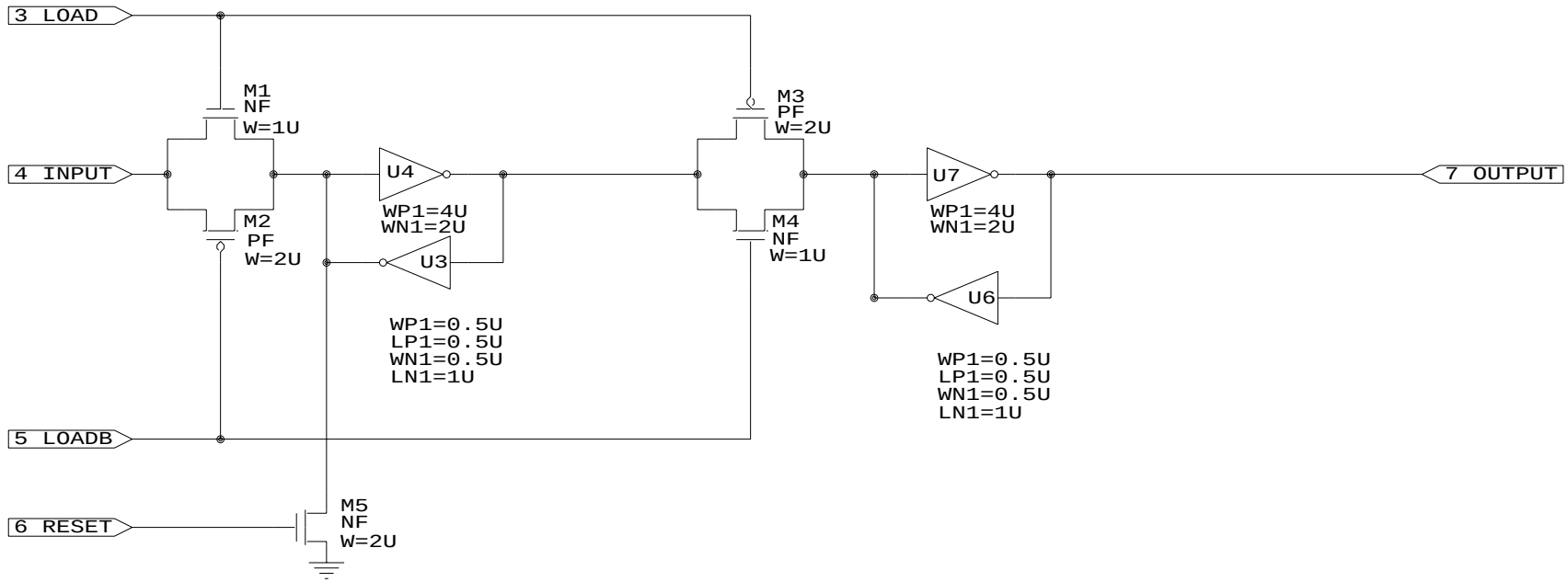
PLACED IN TDATA

United Memories Inc. Project: 128D14		
Title 2 TO 1 MUX - TRANSFER		
Size A	Document Number MUX1	REV A
Date: August 24, 2001	Sheet 1 of 1	



PLACED IN TDATA

United Memories Inc. Project: 128D14		
Title 2 TO 1 MUX - TRANSFER WITH DECODE		
Size A	Document Number MUX2	REV A
Date: August 24, 2001	Sheet 1 of 1	



PLACED IN TDATA

UNITED MEMORIES INC.
PROJECT: 128D14

Title		
	Tdata-Bit	
Size A	Document Number TDBIT	REV A
Date: August 24, 2001	Sheet 1 of 1	

REVISION HISTORY

NOTE: The revision numbers on this .pdf document do not necessarily bear any relation to the revision numbers in the database.

DATE	REVISION	MODIFICATIONS
01/20/02	128D14_SCH_A0	Original document
02/14/02	128D14_SCH_1	Revised shematics: d14chip, damp and chlf.